Low-Power and Robust Level-Shifter with Contention Mitigation for Memory and Standalone Applications

Kenneth M. Ramclam

University of South Florida, kennethramclam@gmail.com

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Low-Power and Robust Level-Shifter with Contention Mitigation for Memory and Standalone Applications

by

Kenneth M. Ramclam

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Computer Engineering
Department of Computer Science and Engineering
College of Engineering
University of South Florida

Major Professor: Swaroop Ghosh, Ph.D. Srinivas Katkoori, Ph.D. Hao Zheng, Ph.D. Jaydeep Kulkarni, Ph.D.

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DEDICATION

This is to my parents, Emelio Mena and Cherry Cadle, to my wife, Amira Shriteh Ramclam, and to the rest of my family, Joshua and Madonna Mena. Their belief in my capabilities and constant motivation helped to make everything possible.
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ABSTRACT

The scaling down of transistor sizes has imposed significant challenges in today’s technology. Memories such as eDRAM, are experiencing poor retention time because of challenges such as reference voltage variation, high transistor leakage, and low cell capacitance. It can be seen that we must consider not only the first order effects, but also the second order effects to ensure we keep up with current technology trends such as Moore’s law. In this thesis we explore various circuit level techniques on level shifters in order to achieve better retention time. With our research, we have addressed important design challenges and propose techniques that can be utilized in current and emerging technologies.

Level shifters (LS) are crucial components in low-power design where the die is segregated in multiple voltage domains. LS are used at the voltage domain interfaces to mitigate sneak path current. A less-known but very important application of LS is in high voltage drivers for designs where voltage boosting is needed for performance and functionality. We first study LS in eDRAM where LS is employed in the wordline path. Our investigation reveals that leakage power of LS can pose a serious threat by lowering the wordline voltage and subsequently affecting the speed and retention time of the eDRAM. It can also be noted that the delay of the LS under worse case process corners can cause significant functional discrepancies. We propose low-power pulsed-LS with supply gating to circumvent these issues. Our analysis indicate that pulsed-LS design can improve the worst case speed from 2.7%-43%. We extended this concept to design generic self-collapsible LSs that can be used for other applications such as voltage interfaces. The self-
collapsed design in both applications improved the worst case speed from 6%–24% and 89% in some cases.
CHAPTER 1

INTRODUCTION

The number of transistors on a chip has increased exponentially in accordance with Moore’s Law [20]. This has provided significant benefit in all applications across the technology spectrum. The number of transistor in today’s technology can easily exceed billions because of continuous scaling down of transistor size. Even though this has been extremely beneficial, it has also brought formidable problems that are only becoming worse. One of the biggest problems that arises from our advances in transistor technology is related to high transistor leakage and power dissipation. This has placed a limitation in scaling down of the transistor sizes and efficient solutions to handle these challenges are being explored every day in order to keep the semiconductor industry from experiencing a deadlock.

What can we consider effective solutions to these problems? One possible solution could be using stacked pMOS in the feedback section of a level shifter to help minimize static current. Some of the major challenges embedded dynamic random access memory (eDRAM) experience today are caused from the process variation and the leakage experienced in the level shifter. Current memories such as SRAM and DRAM are reaching their limitations because of these major design challenges.

\footnote{Portions of this chapter were previously published in [18]. Permission is included in Appendix A.}
Energy efficient circuit systems is becoming one of the most compelling design approaches in today’s community. Advances in design automation and power management has helped bring us into a new era of low-power. Features such as putting a memory bank to sleep when it is not being accessed, can significantly reduce the transistor leakage and lower its power consumption. The memory architecture described in this thesis will utilize some of these ideas and new techniques never seen before.

1.1 Embedded Dynamic Random Access Memory

Embedded dynamic random access memory (eDRAM) is a promising candidate for last level caches or replacing the off-chip DRAM to meet high bandwidth requirements of graphic processors [19]. Fig 1.1 shows the simplified column structure of the eDRAM which includes the bitline (BL), the reference bitline (rBL), 1T1C, senseamp, precharge, column select, write driver, and halfvcc generator. Some important and unique characteristics about the eDRAM are: a)
senseamp is placed on per-column basis (instead of per-global column) in order to restore the bits associated with unselected columns during the read/write operation; b) senseamp is fired by enabling both the header and footer transistors (instead of footer transistor firing) in order to prevent static current due to halfvcc bitline precharge; c) the precharge and equalization circuit consists of full CMOS gates due to halfvcc precharge (instead of NMOS only pass transistor); and the wordline is boosted to $V_{pp} \approx V_{cc} + V_{tn}$ in order to write a full “1” through the nMOS access transistor [21].

The figure shows that a pMOS type is used as column select to ensure a full “1” is written through the write driver. To write a “0”, the rBL will first write a full “1” while the BL stays close to $V_{tp}$ (threshold voltage of pMOS transistor) and then using the senseamp. When the senseamp turns ON, it will pull the BL to a full “0”.

Leakage and power dissipation of large eDRAM caches can have a significant effect on the retention time. First order effects such as low cell capacitance and high transistor leakage have been the major contributors to this problem but its only part of the case. Second-order effects such as supply voltage variation can prevent a full “1” writeback and significantly reduce the retention time of the bitcell. It can be said that the major design issues of eDRAM comes down to its sense margin and retention time [21]. It is crucial that designers model and understand the factors that affect the retention time of eDRAM.

1.2 Level Shifters for eDRAM

Supply voltage scaling is an effective knob to reduce the power consumption and has been exploited extensively on various parts of micro-processors to control both dynamic and leakage power consumption [1]. Since the optimal voltage for each part could be different, the
die is segregated into several voltage domains. For example, cache voltage is typically higher than core voltage. Level shifters (LS) are needed whenever the voltage domain is crossed. Although this application of LS is important, the number of level shifters in the die is limited to few thousands. Therefore power and performance of LS does not pose a significant threat.

Another application of LS is in embedded memory where the number of these components could be in the order of 4-5 sigma. Embedded Dynamic Random Access Memory (eDRAM) [2] employs high voltage (HV) on the gate (i.e., the wordline) of access transistor to write a full logical ‘1’ on the storage element. Therefore the wordline (WL) driver is operated on the high voltage supply ($V_{DDH}$). Dedicated charge pumps are employed to support the high voltage circuitries. The WL predecoder employs LS to convert nominal voltage ($V_{DD}$) to high voltage. The emerging memories such as Spin-Transfer Torque Random Access Memory (STTRAM) also employ HV on the access transistor to reduce the write failure while maintaining small bitcell footprint for improved memory density. The HV is typically generated

![Diagram](image_url)

Figure 1.2 Level shifters in the wordline driver path.
by using a dedicated charge pump (CP) [3]. Fig. 1.2 shows the simplified diagram of WL path for memory arrays where LSs are employed in both WL predecoder (typically located in the row driver) and WL enable (typically located in the timer). The detailed structure of the WL path is explained in chapter 2.

The prime complexity involved in designing the LS for embedded memory is due to the fact that $V_{DDH}$ can vary depending on PVT and load current [3]. This can be understood from the cartoon in Fig. 1.3 that shows CP output vs. load current behavior and the impact of PVT variations. Both CP output and load current can vary due PVT fluctuation and has a cumulative impact on $V_{DDH}$ variation. This is on top of access dependent load current variation (explained in chapter 2). Therefore, the functionality of LS has to be guaranteed for a wide range of $V_{DDH}$.

Other challenge with LS design involves (a) tight area budget as the LS should fit within the array with minimum area overhead, (b) the LS transistors should be protected to avoid reliability issues.

![Figure 1.3 $V_{DDH}$ Variation due to PVT variation in charge pump and load current.](image-url)
degradation due to NBTI, PBTI and HCI [4] and (c) reducing the leakage of the LS to alleviate the burden from charge pump and save standby power.

1.3 Related Work

Level shifters are well studied circuits and numerous design approaches have been proposed in literature to improve its robustness, area and power consumption. A contention mitigated LS (CMLS) is proposed in [5] that uses stacked PMOS transistors to mitigate the contention from PMOS in conventional DCVS (differential cascade voltage switch) LS [6]. A pass transistor based LS (LSpg) and several flavors to mitigate the contention to improve delay and reduce power has been described [7]. Another work [8] proposed a 2-step LS to reduce the load from charge pump during LS toggling. A new approach to embed the LS in flip-flops (FF) is introduced in [9]. By using LS FF, the area overhead can be minimized and interfacing between two different voltage levels can be made seamless. In order to address the issue of interfacing between high voltage IO and logic operating at subthreshold voltages, new LS topology is presented in [10]. Although the above techniques are low-overhead, low-power and robust they are not designed to operate at wide range of supply voltages. An error correcting LS is described in [11] to convert very low voltage to very high voltage. A novel technique to mitigate the contention in conventional DCVS LS and enable wide range of operation is introduced in [12] and [17] is based on a current mirror circuit. The work proposed by [16], which is also low-power, utilizes the classic model LS with an extra inverter at both input and output. Although effective the large area overhead with these techniques would prevent its application in eDRAM wordline selection. The LS from [15] also experiences a large area overhead due to the initial LS design choice and would prevent its use for eDRAM. A wide operating LS with shared droop circuit for embedded memory application is proposed in [18]
however the design is not suitable for standalone level shifting due to area overhead of the droop circuitry.

This thesis provides an in-depth analysis of the design issues related to LS for application in embedded memory, wordline boosting, and standalone circuit. In summary, we make following contributions in this thesis,

- We provide comprehensive analysis of LS operating conditions (in terms of leakage and performance) for wordline application.
- Our study shows that delay and power of LS can affect the functionality and retention time when coupled with eDRAM.
- We propose and evaluate a novel wide-operating pulsed LS to solve the above challenges in eDRAM by mitigating contention in LS. We also propose a power gating technique for robustness and low-power.
- We provide a system level analysis of eDRAM outlining the need for low-power peripheral to maintain high performance and retention.
- We propose embedded self-collapsing mechanism for contention mitigation that is suitable for standalone application in voltage boundaries.
- We show that the concept of self-collapsing is universal and could be employed in any existing LS topology. An example is illustrated by modifying the 2-Step LS [8] and embedded the self-collapsing mechanism.

The rest of the paper is organized as follows. In Chapter 2, we describe the memory architecture and operating conditions of LS. We look at the impact of $V_{DDH}$ on leakage and functionality of
LS. The low-power and wide-operating pulsed LS design and the system level analysis is also described in this chapter. The self-collapsing technique for 2-Step LS and passgate LS is presented in chapter 3 respectively. Finally, conclusions are drawn in chapter 4.
In this chapter we first present the memory architecture (including bank and subarray level design) to describe the wordline driver design. This is followed by CP modeling and analysis.

2.1 Wordline Driver Design

Fig. 2.1 shows the 32MB eDRAM array that contains 128 banks each with 256KB capacity. Each bank consists of 8 subarrays. Each subarray contains 256 rows and 1024 columns.

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2 Portions of this chapter were previously published in [18]. Permissions is included in Appendix A.
The detailed subarray and 128KB eDRAM bank architecture [13] for NOR style WL driver is also illustrated. The raw address is predecoded into high, mid and low outside array and shipped to the subarrays for further decoding. The addressing structure for the bank is shown in figure 2.1. The wordline selection is done based on predecoded address, wordline enable and subarray select. The wordline decoding is done in following manner:

\[
\text{for}(i = 0; i < \text{length}(addrh); i + +)\{
\quad \text{for}(j = 0; j < \text{length}(addrm); j + +)\{
\quad \quad \text{for}(k = 0; k < \text{length}(addrl); k + +)\{
\quad \quad \quad \text{WL}[2^7 \times \text{sectorsel} + 2^5 \times i + 2^3 \times j + k]
\quad \quad \quad = \text{Subarraysel}&\text{Wlen}&\text{Addh}[i]&\text{Addm}[j]&\text{Addl}[k]
\quad \quad \}\}
\}\}
\]

The LS are present in WL driver after predecoding stage as well as in timer. The total number of LS per bank is 544 (i.e., ((256/4)+4)x8). For the 32MB array, the total number of LS is 69632

Figure 2.2 Access modes of the memory die.
(i.e., 544x128). The HV circuitries including WL driver and LS are supported by a dedicated charge pump. The charge pump load contains the leakage power of idle banks and active power of selected banks. For this study, we consider 4 types of access patterns: (a) 1 bank access (1B or 1X), (b) 2 bank access (2B or 2X), (c) 4 bank access (4B or 4X) and (d) 8 bank access (8B or 8X). The details of these modes are shown in Fig. 2.2. Note that the access modes are bandwidth dependent. 1B is suitable for low bandwidth while 8B is suitable for high bandwidth. Furthermore, the bank accesses can be interleaved to avoid supply droop. The \( V_{\text{DDH}} \) load current is given by the summation of dynamic current drawn by the HV circuitries of active banks and leakage power of inactive banks. For 1B mode, leakage power dominates the total load whereas in 8B mode, dynamic power also becomes significant.

2.2 Charge Pump Modeling

For accurate estimation of \( V_{\text{DDH}} \) and low-power design of LS it is important to model and integrate CP in the analysis. In this work, we perform curve fitting of silicon data for the
voltage doubler design [3] to model CP. If the number of CPs per 32MB memory array is \( N \) and supply voltage is \( V_{DD} \) then the output voltage is given by

\[
V_{DDH} = 2V_{DD} - \left( \frac{I_{load}}{N} \right) \left( \frac{\Delta}{5.2 \times 10^{-3}} \right)
\]  

(1)

where \( \Delta = 0.5 \) (1.2) for \( f/2 \) (\( f/8 \)). Fig. 2.3 shows that above model closely matches silicon data. It can be observed that \( V_{DDH} \) droops significantly due to increase in load current. In our analysis we employ multiple CPs to compensate for larger load (Fig. 2.4). Note that the downside of employing multiple CP (increasing \( N \)) is two-fold: (a) area overhead and (b) possibility of very high voltage (closer to \( 2V_{DD} \)) at the HV circuits which may experience reliability degradation.

2.3 Impact of \( V_{DDH} \) Variation on Retention Time

Read operation in eDRAM is destructive due to charge sharing between bitcell and bitline and writeback is essential to maintain the functional integrity. The writeback voltage depends on WL voltage (since NMOS access transistor cannot pass a full high signal) which in

![Figure 2.4 Mitigating VDDH droop by increasing the number of CPs](image-url)
turn depends on $V_{DDH}$. Degradation in writeback voltage is manifested as poor retention time (i.e., the maximum amount of time before which the bitcell can be read correctly). This issue is further illustrated in Fig. 2.5.

2.4 Level Shifter for eDRAM

In this section, we describe the LS designs and analyze them in terms of power and delay. The primary challenge of designing LS is to ensure its robustness across all $V_{DDH}$, process skews and random variations. For example, the design requirements for $V_{DDH} = V_{DDH}(\text{min})$ may conflict with the design for $V_{DDH} = V_{DDH}(\text{max})$. Similarly, the designs for FS and SF corners could conflict with each other. These challenges are further elaborated in Section 2.5.

The simulations are carried out with predictive 22nm HP models [ref] using the Hspice simulation tool. Fast (slow) corner is modeled by reducing (adding) 150mV in the transistor
threshold voltage \( V_{TH} \). We have simulated at five process corners namely TT (typical nmos and pmos), FS (fast nmos, slow pmos), SF (fast nmos, slow pmos), SS (slow nmos, slow pmos) and FF (fast nmos, fast pmos). The random variations are modeled by adding \( V_{TH} \) with \((\mu, \sigma) = (0, 50\text{mV})\). Since there are 69K LS present in the memory system, 4.5 sigma analysis is performed in these corners to ensure the functionality of the LS. For analysis of LS stability \( V_{DH} \) is varied between \( V_{DH}(\text{min}) \) and \( V_{DH}(\text{max}) \). The \( V_{DH}(\text{min})=V_{DL}=1\text{V} \) and \( V_{DH}(\text{max})=1.8\text{V} \). Hot

![Figure 2.6 DCVS LS.](image)

![Figure 2.7 Passgate LS.](image)
temperature (90°C) is used for delay and leakage estimations. A total of 20 charge pumplets have been assumed for leakage simulations.

### 2.5 Analysis of Baseline Level Shifter

Fig. 2.6 and 2.7 depict two common LS designs [6] [7] - LSnom and LSpg. The LSpg from Fig. 2.7 contains two more transistors than the classical LSpg [7]. PMOS {P1} is used to disconnect N0 from P0 during a (1 → 0) transition so that N0 can pull the output down without contention from P0 which is weakly ON (Vgs=V_{DDH}-V_{DDL}). PMOS {P3} is added to weaken the feedback path so that it can only keep the P0 OFF after 1→0 transition and enable easy flipping (due to minimal contention with {N1, N2}) during 0→1 transition.

The pros of LSnom lie in its simplicity and symmetrical nature whereas the con is its area overhead. Due to symmetry, LSnom experiences contention in both directions. Since V_{DDH}

![LSnom Chart](image)

**Figure 2.8** DCVS LS plot showing (μ+4.5σ) delay under process variations.
can vary from low to high voltages the PMOS is kept small. The NMOS is sized such that it is strong enough to win the contention with PMOS under all VDDH and process skews. In our simulation the NMOS is sized 5X than PMOS to ensure robustness under 4.5sigma at all process skews. The LS is sized to drive FO4 load. Fig. 2.8 plots the $(\mu+4.5\sigma)$ rise and fall delay points obtained using Monte Carlo for all process skews. It can be observed that the rise delay is worse when VDDH is low and the PMOS transistor is slow (SS and FS corners). At higher voltages (and SF corner), the fall delay gets worse due to stronger PMOS transistor. Furthermore, the plot also reveals the challenge in designing LS that can operate at wide range of voltages without impacting the propagation delay.

LSpg is low overhead and preferable for area constrained applications. The sizing of LSpg is done to mitigate the stability and robustness under all process and voltage conditions. Compared to LSnom, this structure experiences contention in only one direction. Fig. 2.7 shows...
the contention between \{P2, P3\} and \{N1, N2\} at SF corner when $V_{\text{DDH}}$ is $V_{\text{DDH}}(\text{max})$. The sizing should be done so that \{N1, N2\} wins the fight with \{P2, P3\} and node ‘fb’ is pulled down to turn \{P0, P1\} ON (for fast rise delay). The same sizing conflicts when $V_{\text{DDH}}=V_{\text{DDH}}(\text{min})$ and \{P2, P3\} is too weak to pull node ‘fb’ to turn \{P0, P1\} OFF. This results in contention between \{P0, P1\} and N0 as both are ON simultaneously (slow fall delay). We consider these conflicting requirements for sizing the LS. Fig. 2.9 shows the path delay simulated at room temperature. It can be observed that rise delay is worse at low $V_{\text{DDH}}$ whereas fall delay is worse at high $V_{\text{DDH}}$ (@SS corner). This is an outcome of weak NMOS and relatively strong PMOS due to very good $V_{\text{GS}}$ at high $V_{\text{DDH}}$(@SS corner).

The leakage vs. $V_{\text{DDH}}$ applied is depicted in Fig. 2.10. The corresponding droop in $V_{\text{DDH}}$ (due to LS leakage) is also plotted in Fig. 2.11. It can be observed that the LS leakage can
Figure 2.11 Corresponding values of actual voltage received from CP at different corners.

Figure 2.12 Plot showing that VDDH can be boosted by increasing the number of CPs (FF corner is used for this simulation).
significantly affect the CP output voltage. Therefore the LS and WL drivers receives less than required $V_{DDH}$ degrading the writeback voltage of bitcell and degrading the retention time. We have simulated a single eDRAM bitcell and the results are depicted in Fig. 2.5. For this simulation we have used the bitcell capacitance to be 20fF and bitline capacitance to be 50fF. The circuit simulations are carried out at FF corner and 90C. It can be noted that the retention time reduces with lower $V_{DDH}$ values. This can be attributed to incomplete writeback during read/write access since the NMOS access transistor cannot pass a full logic ‘1’ and the bit is restored to a value much lower than 1V. For the simulations we define the retention time to be the time by which the bitcell loses so much charge that it is unable to develop 100mV differential. From the plot it is evident that retention time can be reduced to 0us due to droop in $V_{DDH}$. These results outline the need for designing low-power LS.

One possible alternative to avoid the $V_{DDH}$ droop is to increase the number of CPs that can supply the leakage and maintain high $V_{DDH}$. Fig. 2.12 shows that the number of CP can be increased to 30 in order to regain the voltage lost due to leakage. However, increasing the CP is associated with extra power consumption.

### 2.6 Robust and Fast Pulsed Level Shifter Design

It can be noted from previous Section that the delay associated with LSpg can be attributed to the contention between P0 and \{N1, N2\} at high voltages. We propose a pulsed-LSpg (pLSpg) to mitigate this contention. The pLSpg design splits the supply of feedback and pull-up PMOS transistors and droops the supply of feedback transistor \{P2, P3\} during up-conversion (0→1 transition). The weakening of feedback PMOS reduces the contention on the node ‘fb’ and assist easy flipping. We have implemented the pLSpg design with the described voltage drooping mechanism as shown in Fig. 2.13. The delay is very sensitive to the amount of
Figure 2.13  Schematic of pLSpg design. The split path for feedback transistor that is controlled by droop circuit is shown in insert.

Figure 2.14  Worst case delay vs. pulse width for different amounts of droop in pLSpg.
droop but the pulsewidth shows a strong impact as well. Both the amount and duration of $V_{DDH}$ droop determines the propagation delay of LS as shown in Fig. 2.14. A narrow pulse doesn’t improve delay significantly because the droop time is insufficient to fully mitigate the contention. Fig. 2.14 also illustrates the rise delay vs. pulse duration for different amount of droop. It can be noticed that the benefit of droop saturates after 40%. This is due to the fact that the contention is already mitigated and extra drooping doesn’t help. Similar argument holds true for pulsewidth more than 50-100ps. The regions dominated by contention and PMOS pull-up are also indicated. The waveforms of feedback node (fb) obtained through circuit simulation is illustrated in Fig. 2.15 for 40% and 60% droop. The waveform without droop is also shown for reference. The reduction in contention at ‘fb’ is evident from this result.

In order to estimate benefit of pLSpg under process variation, we simulated 5000 Monte Carlo points with 60% droop and $\Delta$=100ps for all process corners and $V_{DDH}$ values. The choice
of Δ is based on all corner simulation. The worst case rise delays for SF and SS (which are worst case corners in terms of rise delay) are shown in Fig. 2.16 and 2.17. For the sake of comparison, the worst case of LSpg is also plotted. It can be observed that as much as 30% reduction in worst case rise delay is possible at $V_{DDH}=1.8V@SS$ with the proposed pLSpg. This is very beneficial because the best retention time can be seen when $V_{DDH}=1.8V$. The benefit of feedback weakening is least at $V_{DDH}=1V$ due to absence of contention. Fig. 2.18 and 2.19 shows the histogram of delay distribution with pLSpg for SF and SS corners. The distribution of LSpg is also illustrated for the sake of comparison.

The salient feature of the droop circuit is that it fully operates on $V_{DDL}$ rail eliminating the need of level conversion for control signals. There are two components of the circuit, (a) programmable pulse generator that can modulate the width of pulse duration adaptively and, (b) droop circuit to disconnect the supply from LS and pull it down. The pulse generator senses the rise transition on input and generates a pulse which is in sync with the input. The pulse is fed to PMOS transistor $P_d0$ to disconnect LS from $V_{DDH}$. Note that $P_d0$ will be weakly ON since the pulse input is on $V_{DDL}$ rail. Nevertheless, it will reduce DC current between $V_{DDH}$ and ground when NMOS transistors $N_d0$, $N_d1$ and $N_d2$ start to the pull-down node $V_{droop}$. It is possible to fully disconnect $V_{DDH}$ in order to enable fast droop and eliminate DC current however that would require pulse $n_p$ to be level shifted to $V_{DDH}$ rail (which will create timing complexities). In order to avoid the area and delay overhead we keep the droop circuitry on $V_{DDL}$ rail. Pull-down NMOS transistors $N_d1$ and $N_d2$ are diode connected to clamp the droop to $2V_{TN}$ above ground. This is done to ensure fast pull-back and lower static power.

Note that the proposed circuit provides ~60% droop however multiple droop legs could be added or sizing of $N_d2$ could be dynamically changed to control the magnitude of droop. The
Figure 2.16 PLSpg worst case delay points for a voltage range of 1V to 1.8V at SF corner.

Figure 2.17 PLSpg Worst case delay points for a voltage range of 1V to 1.8V at SS corner.
Figure 2.18  Delay distribution for worst case delay points SF corner

Figure 2.19  Delay distribution for worst case delay points SS corner.
pulse generator and the droop circuit are shared among 64 LS (i.e., per subarray) to minimize the area overhead. The area overhead of the droop circuit is <1% since it is shared by 64 LS present in the subarray. The power overhead is 56uW which is <1%. Note that pLSpg requires pulsing the supply only during rising transition. This is due to the fact the worst case delay is dominated by rise delay. Furthermore, pulsing does not help fall transition due to absence of contention in the falling edge. However, the proposed technique provides opportunity to make trade-off between rise and fall delay. This can be achieved by upsizing the feedback PMOS transistors P2 and P3 which turn-off P0 quickly so that N0 can pull-down easily. The corresponding effect on rise time is minimal since the contention is fully eliminated through pulsing. Fig. 2.20 illustrates the rise and fall delay with upsizing of feedback transistors. It can be observed that the fall delay improvement is minimal since P1 already makes weakens pull-up strength.

![Feedback Size Vs. Delay](image)

Figure 2.20 Plot showing the trade-off between rise and fall delay by feedback transistor upsizing.
2.6.1 Design for Low-Power

From section 2.4.1 it is evident that leakage power of LS poses a threat to functionality and retention time of eDRAM design. We propose a power gated LS to sleep the inactive decoders in order to mitigate the leakage. Fig. 2.21 shows the comparison of leakage with supply and ground gating for different applied $V_{DDH}$. It can be observed that supply gating provides better leakage saving (8X) at high $V_{DDH}$ compared to ground gating (which shows slightly better results for low $V_{DDH}$). Therefore we select supply gating as the enabling leakage saving mechanism for pLSpg.

Note that sleep transistor sizing is non-trivial because the leakage saving and the wakeup time have conflicting sizing requirement. In order to determine the reasonable size we sweep the

Figure 2.21  Leakage vs. $V_{DDH}$ for header and footer transistor (TT corner).
Figure 2.22 Impact of transistor size on leakage in sleep mode.

Figure 2.23 Impact of transistor size on leakage during wake up time. Leakage is simulated at FF corner. The sleep transistor is chosen to ensure wake-up time of 1 cycle (250ps).
transistor width and compare the leakage and wake-up delay (Fig. 2.22 and 2.23). Based on the result obtained we choose 9um to be the sleep transistor size where the wake-up delay is minimized. The sleep signal is controlled by early subarrayselect. When the subarray is activated the LS is woken up. If the LS wakes up late, the wordline driver will be weak and the access latency will go down. For hiding the wakeup latency we require subarrayselect to arrive 1 cycle early (assuming 2GHz operating frequency). Fig. 2.24 shows the $V_{DDH}$ obtained and $V_{DDH}$ applied at WC leakage corner (FF). It can be noted that gated pLSpg can improve the CP output voltage by 34% due to lower leakage. This increases the retention time to 120us (from 0us). The latency is impacted by 1 clock cycle that can be hided.

Figure 2.24 Simulation showing 34%-37% improvement in $V_{DDH}$ by using the sleep transistor.
In the previous section we presented analysis of passgate LS and design of a novel low-power and robust pulsed-LS. In this section, we present system level analysis of the eDRAM memory for various access modes as introduced in Section 2.1. Fig. 2.25 shows the system model that is used for simulation. The LSs are divided into three sections- awake, active and sleep. The number of sleep, awake and active LS is determined by the access mode. For example, 1X mode will wake up 64 LS (since they share a common sleep transistor) with 1 LS being active. The remaining LS will remain in sleep mode (total number of LS=69K). Similarly, 2X will wake up 128 LS with 2 LS being active and so forth. The equations describing number of active, awake and sleeping LS as well as PMOS power-gating sizes for each of the sections can be seen in Fig. 2.25. Note that the leakage of the waked up LSs is higher than that of sleep mode.

2.7 System Level Analysis

Figure 2.25  Simulation model showing sleeping, awake and active LS and corresponding droop circuitries. The size of PMOS sleep transistor and total number of instantiations of sleep, active and awake LSs (i.e., N1, N2, N3, M1, M2 and M3) are also depicted.

\[ N1 = X \times (69k - (N2 + N3)) \]
\[ N2 = X \times (64 - 1) \]
\[ N3 = X \]
\[ X: \text{Mode of Operation (1x, 2x, ... 8x)} \]
\[ M0 = 9\mu m \]
\[ M1 = 1024 - X \]
\[ M2 = (9/64) \times N1 \]
\[ M3 = (9/64) \times (N3 + N2) \]
LSs and therefore they will present extra load to the CP. Apart from that the LS which is fired will draw dynamic current. For the sake of accurate estimation of $V_{DDH}$ due to leakage the CP model is also included in the simulation.

The plot of $V_{DDH}$ obtained for different operating modes are drawn for different $V_{DDH}$ applied in Fig. 2.26. The simulation is performed at 90C and FF corner for worst case leakage. A total of 10 CPs are assumed in this simulation. It can be observed that $V_{DDH}$ obtained from CP decreases as the access mode increases (i.e., for 8X and 16X). Similarly, the actual $V_{DDH}$ observed is lower than the intended value because of leakage experienced by the system. The access time is assumed to be 3ns meaning that the active bank cannot be accessed for at least 3ns (which is equivalent to 12 cycles@4GHz). This access period is determined by the sense, writeback and precharge time. In our simulation, sense time is 1 cycle, precharge time is 1 cycle and remaining 10 cycles are allocated for writeback. The bandwidth vs. retention time is plotted

![Figure 2.26](attachment:image.png)

Figure 2.26 Plot indicating the $V_{DDH}$ obtained vs. access mode for different $V_{DDH}$ applied.
in Fig. 2.27. It can be observed from Fig. 2.26 that 8X mode results in maximum droop in $V_{DDH}$. This corresponds to poor retention time however the bandwidth obtained is maximum in this case. 1X mode improves the retention time due to less droop in $V_{DDH}$ but the corresponding bandwidth is also low. This indicate that higher bandwidth from the memory can be sustained by lowering the retention time which translates to higher refresh power. This trend is shown in Fig. 2.27. Note that the present model of the system does not account for loading due to wordline driver which is a crucial component of leakage and active power. Nevertheless the conclusions drawn remain same. Future model will be improved to comprehend wordline driver leakage for better accuracy and estimation.

Figure 2.27  Bandwidth vs. retention. A higher bandwidth corresponds to lower retention due to $V_{DDH}$ droop and incomplete writeback.
CHAPTER 3

SELF-COLLAPSING LEVEL SHIFTER

The wide-operating pulsed LS for embedded memory is prohibitive for standalone LS due to droop circuit overhead. In this chapter, we show that the concept of pulsing the supply for contention mitigation can be extended to standalone LS as well. This is achieved by embedding the self-collapsing mechanism in the LS itself (scLSpg). The pulse generator and droop circuit from chapter 2 has been reconsidered in order to maintain efficiency. We analyze it in terms of

![Figure 3.1 Generic structure of LS and modifications required.](image-url)

VDDH

LEV

EL

ER

LEVEL SHIFTER

Feedback Section

Driver Section

Delay and Isolation Logic

LS Input

LS Output

S1

S2

Figure 3.1 Generic structure of LS and modifications required.
delay and robustness, and, compare with respect to LSpg and pLSpg. The simulation setup is the same as described in Section 2.4.

3.1 Generic Structure of Self-Collapsing LS

Fig. 3.1 shows the generic structure of LS and modifications required to embed self-collapsing technique. Two switches are required to enable the self-collapsing of feedback path. Switch S1 will disconnect the power supply from feedback while S2 will collapse it to relieve contention. The switches will be controlled based on the LS input. In some cases, a delay and isolation logic might be needed to control the droop duration and enable contention-free collapse.

3.2 Robust and Fast Self-Collapsing Passgate Level-Shifter

As noted before, level shifters are especially needed at voltage domain interfaces to prevent sneak path current from occurring. It can be seen that the pulse generator and droop circuit require more area overhead than the LSpg and this can pose a significant problem since

![Figure 3.2 Schematic of self-collapsing LS (scLSpg).](image)
the LS at each domain is minimal. In order to remove the extra area overhead, we propose self-collapsing pulsed LS which embeds a low-overhead drooping mechanism in the LS eliminating the need of drooping circuit. Note that the proposed circuit may not be suitable for memory application due to extra overhead per LS.

The drooping is achieved by grounding the drain terminal of the feedback PMOS \( P2 \) during an up conversion \( (0 \rightarrow 1) \). Fig. 3.2 illustrates the schematic of the proposed scLSpg. When the input transitions from low to high \( (0 \rightarrow 1) \), PMOS \( \{P2\} \) partially turns OFF and NMOS \( \{N3\} \) turns ON. This provides the collapsing node (\( V_{\text{droop}} \)) with a direct connection to ground allowing very minimal contention during operation. Note that PMOS \( \{P2\} \) is weakly ON due to partial \( V_{\text{gs}} (=V_{\text{DDH}}-V_{\text{DDL}}) \) however, it still reduces contention from \( V_{\text{DDH}} \) and helps in

![Waveform of feedback node (fb) showing the contention mitigation with self-collapsing mechanism.](image)

| Waveform of feedback node (fb) showing the contention mitigation with self-collapsing mechanism. | 34 |
creating the droop. When the input transitions from high to low (1 → 0), PMOS \{P2\} turns ON and NMOS \{N3\} turns OFF. The waveform of feedback node (fb) and \(V_{\text{droop}}\) node obtained through circuit simulation is illustrated in Fig. 3.3 and 3.4.

The scLSpg design is compared with LSpg and pLSpg models by simulating 5000 Monte Carlo points under process variation at worst case conditions. The LSpg and pLSpg were found to experience its worst case rise delay from the SF and SS corner. Therefore, scLSpg was also simulated at the same worst case delay. The SS and SF worst case corner can be seen in Fig. 3.5 and 3.6. The worst case of the LSpg and pLSpg is also plotted for the sake of comparison.

Compared to LSpg, the proposed scLSpg experiences as much as 6%-24% reduction in its worst case rise delay at \(V_{\text{DDH}}=1.0\text{V}-1.8\text{V}@\text{SS}\). It had been noted that the benefit is least at \(V_{\text{DDH}}=1\text{V}\) due to the absence of contention. It can be observed from Fig. 3.6 that scLSpg benefit

Figure 3.4 Circuit simulations illustrating the functionality of self-collapsing mechanism.

![Diagram showing 60% Droop and Self-Collapsing Node]

35
Figure 3.5  Worst case rise delay points for 5000 MC simulations at SS corner with scLSp.

Figure 3.6  Worst case rise delay points for 5000 MC simulations at SF corner with scLSp.
gets saturated from 1.2V $\rightarrow$ 1.8V. This is because PMOS \{P2\} is no longer connected as a feedback from the output of the LS as in Fig. 2.7. It is observed that the scLSpg can experience 24% reduction in its worst case rise delay at $V_{DDH}$=1.8V@SF. Fig. 3.7 and 3.8 shows the histogram of the rise delay distribution with scLSpg for SS and SF corners. The distribution of LSpg and pLSpg are also illustrated for the sake of comparison.

To ensure that the falling transition (1 $\rightarrow$ 0) is not affected by the proposed self-collapsing mechanism, we also performed a worst case analysis for the fall delay. The scLSpg is found to have a worst case fall delay at SS corner. When the driving PMOS \{P4\} experiences high threshold voltage, it can cause the inverter to provide a very slow rising transition to the LS. The slow rising transition can create heavy contention on the feedback node (fb) during a down conversion (1 $\rightarrow$ 0). This contention can be seen by LSpg in Fig 3.9. To mitigate this contention, we propose to employ low threshold voltage on PMOS \{P0\}. It can be observed (Fig 3.9) that

![Image](image-url)

**Figure 3.7** Corresponding delay distribution of scLSpg is shown. The delay of LSpg and pLSpg are also plotted for comparison.
the low threshold voltage can mitigate the contention significantly. We also compared the fall delay of the scLSpg by simulating 5000 Monte Carlo points under process variation with worst case conditions. The SS corner with worst case fall delay points can be noted in Fig 3.10. For the sake of comparison, the worst case fall delay of LSpg and pLSpg are also plotted. It can be seen that as much as 66% reduction in fall delay is possible at V_{DDH}=1.8V@SS with the proposed threshold voltage reduction. Fig 3.11 shows the histogram of the fall delay distribution with scLSpg for SS corner. The distribution of LSpg and pLSpg are also displayed for the sake of comparison. The scLSpg does not pose a significant area overhead. In comparison to the LSpg, there is <0.1% extra area overhead because the scLSpg only requires one extra transistor. The total power consumed is 326uW, which is 18% power overhead compared to LSpg. We reduce this power by proposing a low-power flavor (scLSpg lp).
Figure 3.9 Waveform of feedback node.

Figure 3.10 Worst case fall delay points for 5000 MC simulations simulated at SS corner with scLSpg-lp.
3.2.1 Design for Low-Power

From section 3.2 it can be observed that scLSpg experiences static power consumption between P2 and N3 (Fig. 3.12) when N3 is ON. To prevent the static current generated, we propose (scLSpg-lp) which allows the node \(V_{\text{droop}}\) to be collapsed only for a brief period of time after which N3 is turned OFF. A low overhead pulsing circuit is shown in Fig. 3.12. It consists of an isolation mux to disconnect input from droop transistor N3. Two inverter chains control the mux. During \(0 \rightarrow 1\) transition, PMOS \{P2\} and NMOS \{N3\} receives the input signal from the LS through mux until the delayed signal turns it OFF and turns NMOS N4 ON. This ensures that P2 and N3 are turned OFF. The delay circuit fully operates on \(V_{\text{DDL}}\) rail and does not need level conversion. Note that the inverters in delay chain are stacked to increase the droop duration of \(V_{\text{droop}}\) node. Low threshold voltage is employed on the mux to minimize propagation delay. The collapse time achieved by the scLSpg-lp is demonstrated in Fig. 3.13.

![Figure 3.11](image)

Figure 3.11 The histogram of the fall delay distribution with scLSpg for SS corner.
Figure 3.12 Low-power self-collapse LS (scLSpg-lp) schematic.

Figure 3.13 Collapse time achieved by scLSpg-lp in comparison to the collapse time of scLSpg.
We compared the benefits of scLSpg-lp through the Monte Carlo points collected from scLSpg. The SS worst case rise and fall delay can be seen in Fig. 3.14 and 3.15. The worst case points of LSpg and scLSpg are also plotted for comparison. It can be seen that no delay overhead is experienced by scLSpg-lp for all simulated points. The leakage experienced through NMOS \{N3\} by scLSpg-lp is also plotted in Fig. 3.16. The leakage of scLSpg is also plotted for the sake of comparison. It can be seen that the leakage consumed by scLSpg-lp is 95% less than scLSpg when $V_{DDH} = 1.8V@SS$ corner. The area overhead of scLSpg-lp compared to LSpg is ~50% due to addition of isolation mux and extra inverters. Trade-off between area and delay can be made for area constrained designs.

3.3 Analysis of 2-Step Level-shifter

Section 3.2 described an embedded self-collapsing LS for contention mitigation in standalone LS application. In this section, we show that the self-collapsing technique generic and
Figure 3.15  Worst case fall delay points for 5000 MC simulations simulated at SS corner with scLSpg-lp.

Figure 3.16  Leakage experienced through NMOS {N3} by scLSpg-lp compared to scLSpg.
can be embedded in any LS topology. We take an example of 2-Step LS [8] and employ self-collapsing mechanism (sc-2SLS) to improve its performance. We then analyze it in terms of delay and robustness. The 2-Step Level-Shifter (2SLS) is designed to increase the performance and efficiency for wordline boosting in 8T SRAM (figure omitted for brevity). The 2SLS receives a ‘0’ input and can select between $V_{DDL}$ and $V_{DDH}$ as the output to the wordline. The selection of the output is determined by the state of the enable signal and the input signal from the wordline decoder. The 2SLS performs its transition from (0 → $V_{DDH}$) in 2 steps. When a level shifting is needed, the 2SLS transitions from (0 → $V_{DDL}$) at the output which is then used to drive the output from ($V_{DDL}$ → $V_{DDH}$). Even though the LS is done in 2 steps, the design still experiences significant contention at the feedback node (fb).

Figure 3.17  Self-collapse 2-Step LS (sc-2SLS) schematic.
The proposed 2SLS with the self-collapsing mechanism (sc-2SLS) is depicted in Fig. 3.17. The added transistors to enable self-collapsing (shaded in Fig. 3.17) are very similar to transistor \{P2, N3\} of Fig. 3.2. When the input transitions from \(0 \rightarrow 1\), PMOS \{P6\} is turned ON. PMOS \{P6\} then turns NMOS \{N2\} ON which allows the feedback node (fb) to be pulled to ground by NMOS \{N0\}. This becomes a problem because PMOS \{P5\} is still supplying \(V_{DDH}\) to the feedback node (fb) during this transition. This contention continues until PMOS \{P6\} partially turns OFF PMOS \{P5\} and NMOS \{N0\} overcomes the sneak path current. Fig. 3.19 plots the \((\mu+4.5\sigma)\) rise delay points obtained using Monte Carlo for all process skews. It can be observed that the rise delay is worse when the \(V_{DDH}\) is low and at the (FS and SS) corner. The (SS) corner could not be plotted because 95% of the Monte Carlo simulation failed due to significant contention. The contention at the feedback node (fb) can be seen in Fig. 3.18. In the

3.4 Robust and Fast Self-Collapsing 2-Step Level-Shifter

Figure 3.18 Waveform of feedback node (fb) showing contention mitigation with self-collapsing mechanism.
Figure 3.19  Plot showing $(\mu+4.5\sigma)$ rise delay under process-variations.

Figure 3.20  Worst case rise delay points for 5000 MC simulations simulated at SS and FS corner with sc-2SLS.
worst case corner (FS), 2SLS takes 1ns to complete a full transition due to this contention. It can also be observed that it never completes due to contention in worst case (SS) corner.

The proposed sc-2SLS relieves this contention during the (0 → 1) transition. During a (0 → 1) transition, NMOS {N4} is turned ON and PMOS {P7} is partially turned OFF. This disconnects PMOS {P5} from the feedback node (fb) and NMOS {N4} provides a direct path to ground for all sneak path current. The feedback node (fb) experiences minimal contention when PMOS {P8} turns ON. PMOS {P8} provides $V_{DDH}$ to the output and allows PMOS {P5} to fully turn OFF allowing PMOS {P7} to slowly turn OFF as well. This removes all sneak path current experienced through NMOS {N4}. It can be observed in Fig. 3.18 that the feedback node (fb) of sc-2SLS at the (SS) corner is able to transition significantly faster than the 2SLS at (SF and SS) worst case corner. The worst case rise delays for FS and SS (which are worst case corners in terms of rise delay) are shown in Fig. 3.20. For the sake of comparison, the worst case delay of

Figure 3.21  Showing leakage experienced by sc-2SLS. The 2SLS is also plotted for comparison.
2SLS is also plotted. It can be noted that as much as 89% reduction in worst case rise delay is possible at $V_{DDH}=1.8V@FS$ with the proposed sc-2SLS. This is very beneficial because the best retention time can be seen at $V_{DDH}=1.8V$.

ScLSpg design experiences sneak path current through NMOS {N3} because PMOS {P2} remain partially ON. This can create significant amount of leakage because the scLSpg can remain in that state for long periods of time. The sc-2SLS doesn’t experience this leakage because it receives protection from the transmission gate consisting of PMOS {P4, P5}. When PMOS {P8} is turned ON, it eliminates the sneak path current generated from PMOS {P5} because it is fully turned OFF. Fig. 3.21 shows that the total leakage in the worst case (FS) corner remains same for sc-2SLS. This is because the sneak path current experienced by sc-2SLS is less than or equal to the amount of leakage experienced by the contention at the feedback node (fb) of 2SLS. The total amount of area overhead required for sc-2SLS is $<3.5\%$. 
CHAPTER 4

CONCLUSION

EDRAM is known to experience design issues that can detrimental to its functionality. We studied level-shifters for application in eDRAM and voltage domain interfaces to explore these issues. Our investigation for eDRAM revealed that leakage power of the LS circuitries could play an important role in determining the retention time and functionality. It also indicated that conventionally designed LS may fail to meet the timing requirement due to wide CP voltage variation.

In chapter 2, we introduced the eDRAM array and a system level design on the level shifters. We then proposed a novel low-overhead power-gated pulsed LS to break the dependency of LS speed on CP output variation and enable fast level conversion and higher retention time. By focusing on the worst case corner delays, we were able to locate problematic areas of the level shifters and minimize power consumption in the design. Our system level simulation indicated the presence of an interesting trade-off between bandwidth, leakage power of LS and standby power of system that is governed by retention time.

In chapter 3, we introduced a generalized model that can be used to employ the self-collapsing technique on various level shifter topologies. We applied the model to the Passgate LS and the 2-Step LS and showed the performance improvement. It was seen that the self-collapsing LS allowed for significant contention mitigation and fast level conversion with a small power overhead in comparison to conventional LS.
CHAPTER 5

FUTURE WORKS

The future research will focus on exploring and introducing new series of wide operating and robust level shifters that utilize the proposed self-collapsing mechanism. With minimal overhead and fast conversion time, the proposed LS can be utilized in various applications. One significant benefit of the 2SLS is that it does not require a delay and isolation logic which makes it a promising candidate for area and power constrained applications. The future work will study sc-2SLS application in eDRAM for trade-off between leakage, retention time and bandwidth. A detailed comparison of the self-collapsing 2SLS with other 2-step LS will be carried out to quantify the benefit of the proposed technique.
REFERENCES


APPENDIX A

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