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Characterization and modeling of planar spiral inductors and pad stack parasitic effects

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Characterization and Modeling of Planar Spiral Inductors and Pad Stack Parasitic Effects

by

John Capwell

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering Department of Electrical Engineering College of Engineering University of South Florida

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Date of Approval:
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Keywords: passive components, measurements, inter-connects, capacitors, substrate scalable

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<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>W</td>
<td>Width of the input line</td>
</tr>
<tr>
<td>H</td>
<td>Thickness of the substrate</td>
</tr>
<tr>
<td>c</td>
<td>Speed of light</td>
</tr>
<tr>
<td>C</td>
<td>Capacitance</td>
</tr>
<tr>
<td>$\varepsilon_{\text{eff}}$</td>
<td>Effective dielectric constant</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>Relative dielectric constant</td>
</tr>
<tr>
<td>dB</td>
<td>Decibels</td>
</tr>
<tr>
<td>GSG</td>
<td>Ground signal ground</td>
</tr>
<tr>
<td>L</td>
<td>Inductance</td>
</tr>
<tr>
<td>MCROSS</td>
<td>Microstrip cross-junction</td>
</tr>
<tr>
<td>MLEF</td>
<td>Microstrip line open-end effect</td>
</tr>
<tr>
<td>MLIN</td>
<td>Microstrip line</td>
</tr>
<tr>
<td>MSTEP</td>
<td>Microstrip step in width</td>
</tr>
<tr>
<td>MTEE</td>
<td>Microstrip T-junction</td>
</tr>
<tr>
<td>$\Omega$</td>
<td>Ohms, resistance units</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>R</td>
<td>Resistance</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>Conductivity</td>
</tr>
<tr>
<td>SOLR</td>
<td>Short-Open-Load-Reciprocal Thru</td>
</tr>
<tr>
<td>T</td>
<td>Metal thickness</td>
</tr>
<tr>
<td>TRL</td>
<td>Thru-reflect-line</td>
</tr>
<tr>
<td>X</td>
<td>Reactance</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector network analyzer</td>
</tr>
<tr>
<td>$Z_{0_9.9}$</td>
<td>Characteristic impedance of the pad if the dielectric constant is 9.9</td>
</tr>
<tr>
<td>$Z_0$</td>
<td>Characteristic impedance of the pad with the dielectric constant of the substrate</td>
</tr>
<tr>
<td>$\varepsilon_{\text{eff_9.9}}$</td>
<td>Effective dielectric constant of the substrate if the dielectric constant is 9.9</td>
</tr>
<tr>
<td>$\varepsilon_{\text{eff}}$</td>
<td>Effective dielectric constant of the substrate</td>
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</table>
Characterization and Modeling of Planar Spiral Inductors and Pad Stack Parasitic Effects

John Capwell

ABSTRACT

This thesis concentrates on RF/microwave characterization and modeling of planar spiral inductors and pad stack parasitics. The inductors varied in size from 1.9 to 15.3 nH. Several approaches were examined for modeling the planar spiral inductors. The approach developed herein is built around an existing composite model (available in commercial computer-aided design software), with added series and shunt impedances at both the input and output of the existing composite model. Artificial neural network (ANN) software was used to determine the correction impedance values. Another approach investigated was to model the S-parameters of the inductor using a space-mapping model of the input parameters for the existing model. The correction impedance modeling approach was theoretically sound but the level of accuracy need for the ANN model was not obtainable. The space mapping approach had merit but a substrate and parameter scalable model could not be achieved.

A pad stack is a section of microstrip line that a surface mounted element is affixed to; these pad stacks are standardized for specific element sizes, so for example any 0805 (80 mils by 50 mils) element may have the same pad stack whether it is a capacitor, inductor or resistor. The pad stack models were necessary because a capacitor model originally developed at the University of South Florida did not include parasitic effects for different input connections. The pad stack parasitic models can be broken
down into three types: dual-input, tri-input, and quad-input. Each of the dual- and tri-input models have input angles of either 0°, 45°, or 90°. The models were developed using a combination of microstrip and lumped elements.
Chapter 1

Introduction

1.1 Overview

When designing RF/microwave circuits, it is important to take into account both the parasitic effects of the interconnections to the elements (such as chip capacitors and inductors) as well as the parasitic effects of the elements themselves. In modern Computer Aided Engineering (CAE), the goal is to design a circuit virtually on a computer (using software such as Agilent’s Advanced Design System™) and then manufacture it to produce the same response as the simulated design. The use of “ideal” elements (eg. perfect inductors and capacitors) in a circuit schematic can give an accurate response at low frequencies, but accounting for parasitic effects becomes increasingly important as the frequency is increased. In order to avoid manual tuning of the hardware, accurate models need to be used that account for the parasitics at RF/microwave frequencies for not only the circuit elements, but for the interconnections as well.

This thesis will examine two main topics: planar spiral inductor modeling and pad stack parasitic modeling. The pad stack parasitic models were created for different input connections to desired circuit elements. The planar spiral inductor models were developed for inductors with varying geometries and substrate heights. The pad stack parasitic models and planar spiral inductor models are designed to be accurate from .05 to 10 GHz.
The second chapter covers the process of modeling planar spiral inductors. The models include the following input parameters: the number of turns of the inductor, the line width, the spacing between the lines, the dielectric constant of the substrate, and the height of the substrate. The models are intended to be used in Agilent’s Advanced Design System (ADS).

The third chapter will cover pad stack parasitic effects. Pad stacks are the transmission line elements that surface mounted components are affixed to, for example an 0805 capacitor has pad stack dimensions of 50mil (length) by 40mil (width) with 30mil spacing between the pads. The pad stack parasitics result from the discontinuities caused by the connections to the pad stack configuration. A step in width and an angled input offset are examples of these types of discontinuities. The pad stack configuration can be broken down into three different types: single-input, dual-input, and tri-input connections. Due to the use of a two-port VNA, the single-input models were developed from series measurements, but the multi-input models were developed from shunt measurements. The three-input models were developed with one of the inputs terminated by a 50Ω load. All the models are comprised of either a combination of lumped elements and microstrip elements, or just microstrip elements.

The contributions of this thesis include an investigation of two planar spiral inductor modeling approaches and new pad stack parasitic models for surface mount capacitors and inductors. Two methods were investigated for the planar spiral inductor models: correction factor modeling using an existing planar spiral inductor models and a space mapping models for the inputs of the existing planar spiral inductor model. Even though both methods investigated did not produce a usable spiral inductor model, they
can be a good starting point for further research. The pad stack models were designed to increase the versatility of the existing capacitor models, by expanding the range of the layout configurations in which they can be accurately used.
Chapter 2

Planar Spiral Inductors

Figure 1 – Example of a Planar Spiral Inductor. Legend: S: Spacing, R: Radius, and W: width of line.

2.1 Overview

Planar spiral inductors are popular design elements in RF/microwave circuitry. These elements can replace surface mounted components that have to be attached to the Printed Circuit Board (PCB) by a solder or epoxy process. The planar inductor can be manufactured along with the transmission lines; hence the manufacturer saves the cost of a surface mounted component and process to affix the component to the PCB.

In order to use these types of inductors an accurate model is needed. A preliminary model was designed using a pre-existing model from Agilent’s ADS. This model gives an accurate response on some substrate heights (see Figure 5), but fails on others. An alternative approach is to incorporate the existing model as the core of a new model, and build in correction terms to enhance its accuracy. Artificial neural network
software (NueroModeler (1)) was used to generate equations that express the correction factors as a function inductor geometry and frequency.

2.2 Previous Models

Previous planar spiral inductor models have been developed using physics based equations (2), and are accurate at low frequencies, but are lacking at higher frequencies. Agilent’s Advanced Design Systems (ADS) has models for the planar spiral inductor (MSIND) that are frequency, geometry, and substrate dependent. These models give an accurate prediction of the response of most inductors used in this work on 14 mil and 31mil FR4 substrates, but are not accurate for any of the inductors on 5 mil thick substrates. As an example, the return loss for an inductor with 5mil line width, 5mil spacing, and radius of 62mil (see figure 1 for spiral geometry) can be seen in Figures 2 through 4. There are obvious differences between measured and simulated results on the 5mil boards, but reasonable accuracy is achieved on the other two substrates.
Figure 2 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Existing ADS Model to Measured Data for Inductor with 5mil Line Width, 5mil Spacing, and Outer Radius of 62mil on 5mil Thick Substrate.

Figure 3 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Existing ADS Model to Measured Data for Inductor with 5mil Line Width, 5mil Spacing, and Outer Radius of 62mil on 14mil Thick Substrate.
2.3 Design Specifications

The planar inductors were designed on FR4 using 3 substrate heights: 5mil, 14mil, and 31mil. The geometry of the inductors vary with the width of the line, the line spacing, the outside radius of the inductor, and the number of turns of the inductor. For each combination of line width and line spacing the outer radius was varied to get approximate inductance values that can be seen in Table 1 (See Appendix A for inductance equations). The minimum inductance value is based on the smallest obtainable radius using the limitations of the printed circuit board (PCB) technology.
Table 1 – The Design Parameters for the Inductors Used in this Study (N=number of turns).

<table>
<thead>
<tr>
<th>N</th>
<th>Width (mils)</th>
<th>Spacing (mils)</th>
<th>Radius (mils)</th>
<th>Inductance (nH)</th>
<th>N</th>
<th>Width (mils)</th>
<th>Spacing (mils)</th>
<th>Radius (mils)</th>
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2.4 Characterization

Measurements were performed on an HP8719B Vector Network Analyzer (VNA) and JMicro probe station using 650 µm pitch GGB ground-signal-ground (GSG) probes. Cascade’s WinCal 2.1 software was used to perform a Thru-Reflect-Line (TRL) calibration (3) and measure the S-parameters. The measurements were performed from .05~10 GHz. The TRL calibration was performed on the back-side of the multi-layer PCB board (see Figure 5), setting up measurement reference planes at the edge of the
pads for the “live” vias. The calibration substrate thickness was maintained at 14mil, while the inductor substrate thickness was varied between 5, 14, 31mil.

The inductors were printed on one side of a multi-layer PCB board. This PCB board consisted of a metal layer (inductor layer), a substrate, a buried metal layer (ground plane), another substrate, and then another metal layer (calibration layer); see Figure 5 for a graphical representation of the cross-section of the test fixture board. The inductors are on one metal layer and the calibration is performed on the other metal layer. “Live” vias were used to connect the inductor metal layer to the lower metal layer. In order to use live vias to connect the two metal layers, metal was removed from the ground plane where the “live” vias were located. The term “live” via refers to a via used to pass the RF signal to another layer; this is in contrast to a ground via that connects a metal layer to a ground plane.

![Figure 5](image_url)

Figure 5 – Cross-Sectional View of Multi-layer PCB Used to Measure Inductors.

2.5 Model Extraction Techniques

Two techniques are investigated in this section; impedance correction model extraction and space-mapping extraction. Each method uses the existing ADS model as the foundation for the model development.
2.5.1 Impedance Parameter Model Extraction

The impedance parameter model extraction process can be broken down into three main steps. The first step is to theoretically derive expressions for correction impedances. The second step is to calculate the correction impedances from the measured data, making the impedances dependent on the number of turns of the inductor (N), the width of the line (W), the spacing between the lines (S), the outer radius of the inductor (Ro), the substrate height (H), and the frequency (freq). The third step is to develop a suitable set of equations to predict the correction impedances, which are essentially multidimensional fits to the calculated values.

The correction impedances were derived using ABCD parameter, admittance parameters and impedance parameter network theory (4). Through a sequence of network analysis manipulations the correction impedances were found as a function of the entire network ABCD parameters and the existing ADS inductor model parameters. The entire network ABCD parameters are the ABCD parameters derived from inductor measurements.

The first step in the derivation is to represent the existing inductor model as an equivalent pi network (4). The combined network of the correction impedances and admittances, and the ADS model’s equivalent pi network, was simplified into two cascaded “Tee” junction networks (see Figure 6). Each of the remaining “Tee” junction networks were then represented by impedance parameter matrices. The impedance parameter matrices were then converted into ABCD parameter matrices. The reason for converting into ABCD parameter matrices is because they are easily combined when cascaded.
Once these conversions are completed it is possible to solve for the series and shunt impedances ($Z_1$, $Z_2$, $Z_L$, and $Z_R$ from Figure 6b). The final correction factor equations are:

$$Z_R = \frac{2 \cdot B}{(B \cdot C - 1 + A \cdot D)} \quad (1),$$

$$Z_L = \frac{(Z_R + Z_C)}{(1 - Z_R \cdot C)} \quad (2),$$

$$Y_1 = \frac{1}{Z_L} + Y_a \quad (3),$$

$$Y_2 = Y_1 - Y_b \quad (4),$$

$$Z_i = \frac{Z_R \cdot (A - 1 - Z_C)}{(2 - Z_R \cdot C)} \quad (5),$$

$$Z_2 = \frac{(Z_R \cdot (D - 1 + Z_C \cdot C) + Z_C \cdot (D - 2))}{(Z_R + Z_C) \cdot (2 - Z_R \cdot C)} \quad (6).$$

Where $A = -\frac{Y_{11}}{Y_{21}}$, $B = -\frac{1}{Y_{21}}$, $C = -\frac{(Y_{11} \cdot Y_{22} - Y_{12} \cdot Y_{21})}{Y_{21}}$, and $D = -\frac{Y_{11}}{Y_{21}}$. $Y_{11}$, $Y_{21}$, $Y_{12}$, and $Y_{22}$ are the impedance.
parameters for the measured data (4). These equations make it possible to calculate exact values for the correction factors from ABCD parameters derived from measurements of physical inductors, and the equivalent pi network parameters of the existing inductor model. The correction factors are calculated at each of the desired frequency points.

Calculating the correction factors can be done using software such as MathCAD, spreadsheet software such as EXCEL, or simulation software such as ADS. ADS was chosen for this work because the existing inductor models were already simulated for a comparison study, and only the measured data and correction factor equations need to be added to calculate the correction impedances. ADS also has the ability to simulate over different desired frequency ranges. The necessary equations were created in the MeasEqn feature in ADS, making it possible to simulate, automatically display and check the agreement to the simulated response. The correction factors were exported into a series of ASCII files and then imported and manipulated into one file for inputting into the artificial neural network (ANN) software.

Once the data was ready for ANN software the neural network is trained and tested. Training the network is a type of optimization in the ANN software, and different optimization techniques can be used (e. g. Quasi-Newton, gradient, random, etc). While training it is useful options is to observe how the ANN model outputs change as a function of each of the input variables. Also a good rule to follow while training is to use every other data point, as the complete data set can later be used during the testing process. The training process fits the ANN model to the data, and the testing process compares the model to another set of data.
Three different formats were used to input the data into the ANN software: impedances, admittances and the reflection coefficient ($\Gamma$) with respect to 50 $\Omega$ (5). It was determined to input the original configurations of the series impedances ($Z_1$ and $Z_2$ from Figure 6a) and the shunt admittances ($Y_1$ and $Y_2$ from Figure 6a). The four parameters were then separated into their real and imaginary parts. Using the eight separate factors, i.e. the real and imaginary parts for $Z_1$, $Z_2$, $Y_1$, and $Y_2$, a spreadsheet was generated for each, and then converted into space delimited format for inputting into the ANN software.

2.5.1.1 Comparison

Three different responses are compared in this study: the ABCD parameters of the measurements and the ABCD parameters of the new inductor model, the derived correction factor values and the values generated by the ANN equation, and the S-parameters of the measurements verse the S-parameters of the new inductor model using the ANN correction factor equations.

Comparisons of the ABCD parameters of the measurements to the new inductor model were used as a check of the equation derivation process. Ideally this is an exact match as the values for the correction factors for the new model are derived from a closed form expression. Table 2 through Table 5 show comparisons between measured data and derived data of the A, B, C, and D parameters, respectively. These tables show a nearly exact match between measurements and the new inductor model.
Table 2 – A-Parameter Comparison for Measured to Derived Correction Factor Model.

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Table 3 – B-Parameter Comparison for Measured to Derived Correction Factor Model.

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<th>Ro (mil)</th>
<th>H (mil)</th>
<th>Freq. (GHz)</th>
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<th>Calculated B-Parameter</th>
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Table 5 – D- Parameter Comparison for Measured to Derived Correction Factor Model.

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Comparisons of the ANN generated correction factors to the derived correction factors can be seen in Figure 7 – 10. These comparisons are for an ANN model that is generated for a one turn spiral inductor with 5mil line width, 5mil line spacing, 35mil outer radius, on a 5mil substrate. This ANN model was generated for just this one inductor on a single substrate only. The results of an ANN model based on three inductors and three substrates (“3x3 model”) are shown in Figures 11 – 14. The 3x3 ANN was tested and obtained a worst case percent error of 5.5%.
Figure 7 – Z1 Comparison Between Calculated and ANN Generated Data for Planar Spiral Inductor with 5mil Line Width, 5mil Spacing, and 35mil Radius on 5mil FR4 Substrate.

Figure 8 – Z2 Comparison Between Calculated and ANN Generated Data for Planar Spiral Inductor with 5mil Line Width, 5mil Spacing, and 35mil Radius on 5mil FR4 Substrate.
Figure 9 – Y1 Comparison Between Calculated and ANN Generated Data for Planar Spiral Inductor with 5mil Line Width, 5mil Spacing, and 35mil Radius on 5mil FR4 Substrate.

Figure 10 – Y2 Comparison Between Calculated and ANN Generated Data for Planar Spiral Inductor with 5mil Line Width, 5mil Spacing, and 35mil Radius on 5mil FR4 Substrate.
Figure 11 – S11 Comparison Between the 3x3 ANN Model and Measurement for Planar Spiral Inductor with 5mil Line Width, 5mil Spacing, and 35mil Radius on 31mil FR4 Substrate.
Figure 12 – S21 Comparison Between the 3x3 ANN Model and Measurement for Planar Spiral Inductor with 5mil Line Width, 5mil Spacing, and 35mil Radius on 31mil FR4 Substrate.

Figure 13 – S22 Comparison Between the 3x3 ANN Model and Measurement for Planar Spiral Inductor with 5mil Line Width, 5mil Spacing, and 35mil Radius on 31mil FR4 Substrate.
2.5.1.2 Summary

The method for deriving the correction factors is a unique solution and works in theory, but it requires a level of accuracy for the impedance and admittance correction factors that cannot be directly obtained with existing curve fitting methods (i.e. ANN, polynomial, etc). The 3x3 ANN model had a worse case error of 5.5%. It can be seen from figures 11-13 that a 5.5% error has a drastic effect on the response. It was due to this limitation that another method of inductor modeling was investigated.

2.5.2 Space Mapping Model Extraction

Space mapping is another approach of using an existing model as the fundamental part of a new model. In this case, the input parameters to the existing model are modified from the “nominal” (or physical) values in order to obtain the proper response. Then the modified input parameters are mapped to the physical parameters of the inductors. The resulting space map can then be used in reverse to transform the input parameters (the number of turn of the inductor (N), the width of the line (W), the spacing between the lines (S), the outer radius of the inductor (Ro), the substrate height (H), dielectric constant (Er), and frequency (freq)) to the modified inputs that are used with the existing model. In theory the existing model with the modified inputs will be able to output the response for the inductor. A graphical representation of this process can be seen in figure 14.
The modified input parameters were calculated by optimizing the input parameters of the existing model until the s-parameter outputs matched the measured s-parameters.

Some example of these modified input parameters can be seen in Table 6.

**Table 6 – Optimized Results for a Sample of Inductor Space Mapping Coefficients.**

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<thead>
<tr>
<th>Inductor Input Parameters</th>
<th>Modified Input Parameter</th>
</tr>
</thead>
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<tr>
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2.5.2.1 Comparison

Some examples of the modified input parameters can be seen in Table 6. These parameters were then inputted back into the existing ADS model; the results of the space mapping approach can be seen in Figure 15 through Figure 20. These results show that the 14 mil and 31 mil data is an acceptable match but the 5mil data is not an acceptable match.

Figure 15 – S11 Comparison Between the Space Mapping Model and Measurement for Planar Spiral Inductor with 5mil Line Width, 10mil Spacing, and 35mil Radius on 5mil FR4 Substrate.
Figure 16 – S21 Comparison Between the Space Mapping Model and Measurement for Planar Spiral Inductor with 5mil Line Width, 10mil Spacing, and 35mil Radius on 5mil FR4 Substrate.

Figure 17 – S11 Comparison Between the Space Mapping Model and Measurement for Planar Spiral Inductor with 5mil Line Width, 10mil Spacing, and 35mil Radius on 14mil FR4 Substrate.
Figure 18 – S21 Comparison Between the Space Mapping Model and Measurement for Planar Spiral Inductor with 5mil Line Width, 10mil Spacing, and 35mil Radius on 14mil FR4 Substrate.

Figure 19 – S11 Comparison Between the Space Mapping Model and Measurement for Planar Spiral Inductor with 5mil Line Width, 10mil Spacing, and 35mil Radius on 31mil FR4 Substrate.
2.5.2.2 Summary

As with the ANN model extraction approach described in Section 2.5.1, an acceptable match between measurements and models developed using the space-mapping method could only be obtained for the 14 and 31 mil substrates, but not the 5 mil substrate. A method for curve fitting the relationships between the modified inductor inputs among the multiple substrates was not determined.

2.6 Other Modeling Methods

Two other model extraction methods were also investigated - a lumped element model and a coupled line model. Like the previously described methods, the results were acceptable on the 14mil and 31mil thick substrates, but the 5mil model did not agree with
the measured data. These additional studies confirmed a potential issue with the accuracy of the 5mil measured data.

2.7 Summary

One uncertainly involved with the examined model extraction study was the related to the measurement technique used. In this work the measurement reference plane was located on the opposite side of the PCB from the inductors, thus there are live vias between the measurement reference plane and the inductors. These vias could contribute parasitic effects that are not easily accounted for in the models. If the calibration had been performed on the same side of the PCB board as the inductors, it would remove uncertainties related to the vias. In a next iteration it would be advisable of perform this adjustment in the measurement and calibration setup of the PCB design.
Chapter 3

Pad Stack Parasitics

3.1 Overview

The purpose of the pad stack study was to develop models that can be used with high frequency capacitor models to allow more versatility in the way the capacitors are configured on a circuit schematic layout. In this case, the baseline capacitor models were developed at the University of South Florida (USF) and assume 2-port series interconnects in which the input and output lines are parallel to each other. Using the pad stack models, new types of interconnects that can be used range from angled single inputs to multiple inputs of two and three lines. In practice, the different types of inputs are used to minimize the area of a PCB layout, and the models developed herein are representative of the types of component connections used in a realistic PCB. One challenge in developing the new pad stack models is that the USF capacitor model has the effect of the straight, series, 2-port pad stack incorporated into the model. It was desired to leave the original model in tact, and allow alternative pad stack models to be used; therefore the pad stack models first compensate for the built-in effects of a straight 2-port interconnect and then account for the parasitic effects of the actual interconnect being used.

An example of a capacitor pad stack can be seen in Figure 26. This figure also shows that the USF capacitor model reference plane is external to the existing model topology. The USF capacitor model was developed using a microstrip taper as the transition between the capacitor pad stack width and the input microstrip line width, the
latter always being adjusted to achieve a 50 Ω characteristic impedance for the particular substrate.

In this study 5mil, 14mil and 31mil substrates heights were used. On the 14mil and 31mil substrates two different input line widths (connected directly to the pad stacks without the tapers mentioned above) were used to develop the models. The models were developed using an 0805 chip capacitor with a model number 2113740A10(2pF), then verified on capacitor 2113740A49(56pF) and 2113730A66 (300pF). It will be shown that using a combination of microstrip elements and lumped elements, the various interconnections can be accurately modeled from through 9GHz.

3.2 Motivation

Prior to this work, no pad stack parasitic models were available for use with the USF capacitor models. More generally, this is the first known attempt to develop models that accurately negate built-in pad stack effects for one interconnect configuration (i.e. the configuration used to develop the original models) while introducing circuit elements representative of a new configuration. In order to demonstrate the need for such models, two comparisons are shown between measured data for a given pad stack configuration, compared to simulated data using only the USF capacitor model. Figure 14 shows the reflection coefficient measurement of the dual-input 45° pad stack (see Set #3, section 3.3) compared to the original USF capacitor model. Figure 21 shows the reflection coefficient measurement of the dual-input series 90° pad stack (see Set #2, section 3.3) compared to the USF capacitor model. These two figures show that when the input and output configurations are modified the USF capacitor model does not give an accurate response across the band. For frequencies below 1 GHz, the USF capacitor model by
itself gives an accurate response, but as the frequency is increased deviations from the measurements are observed. This occurs due to more pronounced parasitic effects at higher frequencies.

Figure 21– Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated USF Capacitor Model 2113740A10 to Measured Data for 2113740A10 Capacitor with Input Rotated 45° on a 31mil FR4 Substrate.
3.3 Design Specifications

Three different types of connections were investigated: dual-input series connections, tri-input connections, and quad-input connections (the number of inputs includes the interconnect lines plus the connection to the capacitor). The dual-input connections consist of input line connections at input angles of $0^\circ$, $45^\circ$, and $90^\circ$. The tri-input connections have inputs on two sides with input angles of: $0^\circ$ and $90^\circ$, $45^\circ$ and $135^\circ$, and $0^\circ$ and $180^\circ$. Due to the use of two-port measurement equipment, the tri-input structures had to be measured in a shunt configuration. The quad-input connections have one input on each of the unused pad stack sides, but due to the use of two-port measurement equipment one of the inputs had to be terminated in a $50\Omega$ load. Like the
tri-input configuration, all the quad-input configurations were measured in a shunt configuration. All of the different connection sets can be seen in Table 7.

The pad stack parasitic models have been developed for 0805 USF capacitor models. The specific part numbers used were: 2113740A10, 2113740A49, and 2113740A66. The 0805 pad stack has a length of 40mils, a width of 50mils, and a pad spacing of 30mils. The pad stack models have been developed using input line width of 8.5mils and 25.6mils on the 14mil and 31mil substrates; only the 8.5mil input line width was used on the 5mil thick boards. All the models are scalable versus on substrate parameters such as dielectric constants and substrate height, as well as input line widths.
Table 7 – Pad Stack Parasitic Set Description.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Set Number</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Set #1 Diagram" /></td>
<td>Set #1</td>
<td>2 Input Series Connection with 0° Offset</td>
</tr>
<tr>
<td><img src="image2.png" alt="Set #2 Diagram" /></td>
<td>Set #2</td>
<td>2 Input Series Connection with 90° Offset</td>
</tr>
<tr>
<td><img src="image3.png" alt="Set #3 Diagram" /></td>
<td>Set #3</td>
<td>2 Input Series Connection with 45° Offset</td>
</tr>
<tr>
<td><img src="image4.png" alt="Set #4 Diagram" /></td>
<td>Set #4</td>
<td>3 Input Shunt Connection with 0° Offset</td>
</tr>
<tr>
<td><img src="image5.png" alt="Set #5 Diagram" /></td>
<td>Set #5</td>
<td>3 Input Shunt Connection with 45° Offset</td>
</tr>
<tr>
<td><img src="image6.png" alt="Set #6 and #7 Diagram" /></td>
<td>Set #6 and Set #7</td>
<td>3 Input Shunt Connection with 0° &amp; 90° Offset</td>
</tr>
<tr>
<td><img src="image7.png" alt="Set #8 Diagram" /></td>
<td>Set #8</td>
<td>4 Input Shunt Connection with 1-0° &amp; 2-90° Offsets. The 0° Offset is terminated with a 50 Ω Load.</td>
</tr>
<tr>
<td><img src="image8.png" alt="Set #9 and #10 Diagram" /></td>
<td>Set #9 and Set #10</td>
<td>4 Input Shunt Connection with 1-0° &amp; 2-90° Offsets. The one of the 90° Offsets is terminated with a 50 Ω Load.</td>
</tr>
</tbody>
</table>
3.4 Characterization

The measurements used for model extraction were taken on the same equipment and software specified in Chapter 2.4. However, unlike the planar spiral inductor characterization, the TRL calibration was not the only calibration used. An SOLR (short-open-load-reflect) calibration (6) was used on two pad stack configurations. The reason for choosing the SOLR calibration was the ability to perform measurements with the microwave probes positioned at right angles. The SOLR calibration and measurements were performed using WinCal 2.1. The SOLR calibration was used for Set #7 and Set #10 (see Table 7).

3.5 Model Extraction and Comparison

3.5.1 Dual Input Series Connections

There are three dual-input series connections being examined, as seen in Table 7. Set #1 is the same configuration as that used by B. Lakshminarayanan (7) except the tapers used in that work to connect between feed lines and capacitor pad stack were replaced by steps in width. In Set #2 the capacitor is rotated 90° so the connections are
on the length side of the pad stack, instead of the width side. In Set #3 the capacitor is rotated $45^\circ$ so the connections are on the corner of the pad stack.

3.5.1.1 Set #1

Set #1 is a series two-port connection with input lines on the pad width side of the pad stack. The transition between the bond pad and the input line width is a microstrip step element (MSTEP in Series IV and ADS). This structure shows how well a step in width can replace a taper in the original capacitor model. The model for this connection is just a microstrip step in width. Figure 24 shows both the structure and the model. Figures 25 and 26 show the return loss and insertion loss comparisons between the model and measured data.

![Figure 24 – a) Set #1 Layout, b) Set #1 Schematic.](image-url)
Figure 25 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #1 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.

Figure 26 – Insertion Loss (S21) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #1 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.
3.5.1.2 Set #2

Set #2 is a series 2-port connection with the inputs to the bond pad on the pad length side of the pad stack. For this connection the capacitor was rotated 90° and the inputs are on the bond pad length side. It was first attempted to model this connection using a microstrip corner, but the size of the bond pad violated the allowed parameters of the corner element as defined in Series IV and ADS. Instead, a “tee” junction was used and the unused side of the junction was open circuited (see Figure 27b). Because the original capacitor model incorporates the bond pad effects, a microstrip line was added to the side of the junction connected to the capacitor model, with a negative line length equal to the bond pad length. A step in width is added at the input to account for the impedance step between the input line and the bond pad length width. A schematic can be seen in Figure 27b. The USF capacitor is represented in the schematic by the capacitor element labeled “Capacitor_Model”. Figures 28 and 29 show the return loss and insertion loss comparisons between the model and measured data.
Figure 27 – a) Set #2 Layout, b) Set #2 Schematic.
Figure 28 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #2 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.

Figure 29 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #2 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.
3.5.1.3 Set #3

Set #3 is a series 2-port connection with inputs on the corner of the bond pad at an angle of 45°. The 45° connection is modeled with a series inductor and a shunt capacitor to ground (see Figure 30a). The model reference plane is at the tip on the corner; (Figure 30b), where the dashed lines designate the reference plane. The equation for the series inductance (L1) in nH and shunt capacitance (C1) in pF (8) can be seen below. Figures 31 and 32 show the return loss and insertion loss comparisons between the model and measured data.

\[
C1 = 0.3579C*(-0.0506+0.7206*\ln(\frac{1+H}{W}))
\]

\[
L1 = 2*10^{-3}\left[2.8372\ln\left(\frac{5.6744}{W+t}\right) + 0.2871 + 0.0333\left(\frac{W+t}{2.8372}\right)\right]*\left[13.0096 - 2.0459*\ln\left(\frac{1+W}{H}\right)\right]
\]

Where \( C = \frac{\sqrt{\varepsilon_{\text{eff}}}}{c*Z_0} \), \( W \) = width of the input line in mm, \( H \) = thickness of the substrate in mm, \( \varepsilon_{\text{eff}} \) = effective dielectric constant, \( Z_0 \) = Characteristic impedance, \( c \) = speed of light, \( t \) = metal thickness in mm.
Figure 30 – a) Set #3 Layout, b) Set #3 Schematic.
Figure 31 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #3 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.

Figure 32 – Insertion Loss (S21) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #3 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.
3.5.2 Tri Input Shunt Connections Sets

The tri input shunt connections pad stacks are sets 4-7. For these connections the “Tee” junction element (MTEE in Series IV and MTEEO in ADS) and output series inductance at the input to the pad stack structures are used to model this effect. The difference between the sets will be discussed in the corresponding sections below. The via data used in the models are measured for the corresponding substrate thickness.

3.5.2.1 Set #4

Set #4 is a shunt tri-input connection with the input line connections on the pad length sides of the bond pad (see Figure 33a). The input to this model has a step in width at the input to the “Tee” junction, and on the output of the “Tee” junction there is a microstrip line element with a negative line length and series inductance. The inductance was added to compensate for negating the “Tee” junction element by using a negative length of microstrip line. The equation for the series output inductance (L1) (9) in nH can be seen in equation 9; this value was determined via circuit optimization. Figures 34 and 35 show the return loss and insertion loss comparisons between the model and measured data, respectively.

\[
L_1 = 2 \times 10^{-3} \left[ 3.5837 \left[ \ln \left( \frac{7.1674}{W+t} \right) + 0.4056 + 0.0386 \left( \frac{W+t}{3.5837} \right) \right] \right] \times \left[ 6.5551 - 1.6552 \ln \left( \frac{1+W}{H} \right) \right] \tag{9}
\]

Where W= width of the input line in mm, H= thickness of the substrate in mm, t= metal thickness in mm.
Figure 33 – a) Set #4 Layout, b) Set #4 Schematic.

Figure 34 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #4 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.
Set #5

Set #5 is a shunt tri-input connection with the input line connections on the corner of the bond pad at an angle of 45°. It was found that no combination of microstrip elements could model this connection, so a lumped element equivalent circuit was designed. The lumped element circuit for this connection is a series inductance at the input and output of the “Tee” junction element. The equations for these inductances (L1 and L2) (9) in nH can be seen below; these inductance values were determined using circuit optimization. Figures 37 and 38 show the return loss and insertion loss comparisons between the model and measured data, respectively.

\[
L_1 = 2 \times 10^{-3} \left[ 3.3093 \ln \left( \frac{6.6186}{W + t} \right) + 1.5559 + .0649 \left( \frac{W + t}{3.3093} \right) \right] * \left[ 18.052 - 4.5592 \ln \left( \frac{1 + W}{H} \right) \right]
\]
\[ L_2 = 2 \times 10^{-3} \left[ 1.625 \ln \left( \frac{3.25}{W + t} \right) + 0.2941 + 0.0571 \left( \frac{W + t}{1.625} \right) \right] \times \left[ 2.4545 + 0.2607 \ln \left( \frac{1 + W}{H} \right) \right] \] (11)

Where W = width of the input line in mm, H = thickness of the substrate in mm, t = metal thickness in mm.

Figure 36 – a) Set #5 Layout, b) Set #5 Schematic.
Figure 37 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #5 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.

Figure 38 – Insertion Loss (S21) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #5 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.
3.5.2.3 Set #6 and Set #7

Set #6 and Set #7 are shunt tri-input connections with one input line on the width side of the bond pad and the other input line on the length side (see Figure 37a). The input of this model has a step in width at the input to the “Tee” junction and on the output of the “Tee” junction there is a microstrip line element with a negative line length and series inductance. The equation for the series inductance \( L_1 \) (9) in nH can be seen below; these values were optimized to measured data. Figures 40 and 41 show the return loss and insertion loss comparisons between the model and measured data, respectively.

\[
L_1 = 2 \times 10^{-3} \left[ 3.5837 \left( \ln \left( \frac{7.1674}{W + t} \right) + 0.4056 + 0.0586 \left( \frac{W + t}{3.5837} \right) \right) \right] * \left[ 6.5551 - 1.6552 * \ln \left( \frac{1 + W}{H} \right) \right] (12)
\]

Where \( W \) = width of the input line in mm, \( H \) = thickness of the substrate in mm, \( t \) = metal thickness in mm.

Figure 39 – a) Set #6 and Set #7 Layout, b) Set #6 and Set #7 Schematic.
Figure 40 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #6 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.

Figure 41 – Insertion Loss (S21) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #6 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.
3.5.3 Quad Input Shunt Connections

The four input shunt connection pad stacks are sets 8, 9 and 10. Set #10 is the same structure as set #9 except it is set up for an SOLR calibration. All the four-input connections can be modeled with a cross-junction element (MCROS in Series IV and MCROSO in ADS) or cross-junction lumped element equivalent circuit. The cross junction element gives an accurate response but the 0805 pad dimensions violate the Series IV and ADS element parameters on the 5mil and 14mil substrate thicknesses, and an error is reported during simulations. Due to this error a lumped element equivalent circuit was developed (see Figure 42). The lumped element equivalent circuit consists of shunt capacitors \( (C1) \) and series inductances parameters \( (L1, L2 \text{ and } L3) \) - these values are derived from the dimensions of the pad stack (8) and are listed below. Since the pad dimension is rectangular, the inductance and capacitance of the two pad width sides and two pad length sides are equal. Like the “Tee” junction model, a microstrip line element with the width of the bond pad and a length the negative length of the bond pad is placed between the cross junction and the capacitor model to negate the effects of the bond pad that was integrated into the original capacitor model. The via data and load data used in the model were measured for the corresponding substrate thickness.

\[
C1 = \frac{C \left( \frac{Z_{0.99}}{Z_0} \right) \sqrt{\frac{\varepsilon_{\text{eff}}}{\varepsilon_{\text{eff}.9.9}}} \right)}{4}
\]

\[
C = \begin{bmatrix}
\log \left( \frac{W1}{H} \right) \ast \left[ 86.6 \ast \frac{W2}{H} - 30.9 \sqrt{\frac{W2}{H} + 367} \right] \\
\ast \left( \frac{W2}{H} \right)^3 + 74 \left( \frac{W2}{H} \right)^2 + 130
\end{bmatrix} + \frac{1}{1000} W1 (14)
\]

\[
C = \begin{bmatrix}
\log \left( \frac{W1}{H} \right) \ast \left[ 86.6 \ast \frac{W2}{H} - 30.9 \sqrt{\frac{W2}{H} + 367} \right] \\
\ast \left( \frac{W2}{H} \right)^3 + 74 \left( \frac{W2}{H} \right)^2 + 130
\end{bmatrix} + \frac{1}{1000} W1 (14)
\]

\[
C = \begin{bmatrix}
\log \left( \frac{W1}{H} \right) \ast \left[ 86.6 \ast \frac{W2}{H} - 30.9 \sqrt{\frac{W2}{H} + 367} \right] \\
\ast \left( \frac{W2}{H} \right)^3 + 74 \left( \frac{W2}{H} \right)^2 + 130
\end{bmatrix} + \frac{1}{1000} W1 (14)
\]
\[ L1 = \left[ \frac{W1}{H} \right] 165.6 \cdot \frac{W2}{H} + 31.2 \cdot \sqrt{\frac{W2}{H}} - 11.8 \cdot \left( \frac{W2}{H} \right)^2 - 32 \cdot \frac{W2}{H} + 3 \cdot \left( \frac{W1}{H} \right)^\frac{3}{2} \cdot \frac{H}{1000} \] (15)

\[ L2 = \left[ \frac{W2}{H} \right] 165.6 \cdot \frac{W1}{H} + 31.2 \cdot \sqrt{\frac{W1}{H}} - 11.8 \cdot \left( \frac{W1}{H} \right)^2 - 32 \cdot \frac{W1}{H} + 3 \cdot \left( \frac{W2}{H} \right)^\frac{3}{2} \cdot \frac{H}{1000} \] (16)

\[ L3 = 337.5 + \left( 1 + \frac{7}{W1} \right) \cdot \frac{1}{W2} - 5 \cdot \frac{W2}{H} \cos \left( \frac{\pi}{2} \left( 1.5 - \frac{W1}{H} \right) \right) \cdot \frac{H}{1000} \] (17)

Figure 42 – Set #6 and Set #7 Layout.
3.5.3.1 Set #8

Set #8 is a shunt four-input connection with inputs on all four sides. A 50 Ohm load was connected on a “width” side of the pad (see Figure 44a). Figures 45 and 46 show the return loss and insertion loss comparisons between the model and measured data, respectively.
Figure 44 – a) Set #8 Layout, b) Set #8 Schematic.
Figure 45 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #8 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.

Figure 46 – Insertion Loss (S21) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #8 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.
3.5.3.2  Set #9 and Set #10

Set #9 and Set #10 are shunt four-input shunt connection with inputs on all four sides, but in this case a load is attached to a pad “length” side. (Figure 47). Figures 48 and 49 show the return loss and insertion loss comparisons between the model and measured data, respectively.

Figure 47 – a) Set #6 and Set #7 Layout, b) Set #6 and Set #7 Schematic.
Figure 48 – Return Loss (S11) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #9 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.

Figure 49 – Insertion Loss (S21) Magnitude (dB) and Phase (deg) Comparison of Simulated Set #10 Pad Stack Model with USF Capacitor 2113740A10 to Measured Data on 31mil FR4 Substrate.
3.6 Conclusions

This study shows how pad stack configurations can be modeled. These models consist primarily of microstrip elements, but when such elements were not available or inadequate, equivalent lumped element designs were developed. It was demonstrated that the models give an accurate response from 0.05-9GHz.
Chapter 4

Conclusions and Recommendations

The planar spiral inductor modeling and pad stack parasitic modeling studies are good starting points for further research. The planar spiral modeling techniques did not work as anticipated but that theory is sound and could benefit some other types of component modeling. One recommendation for the planar spiral inductor modeling is to have the measurement reference plane on the same substrate was the inductor. Not having the reference plane on the second substrate will add extra measurement time, but it should clear up some of the measurement ambiguity. The pad stack parasitic models have been developed for 0805 capacitor models. Further studies using different pad stack sizes (such as 0201, 0402, 0603 and 1206) and different surface mounted elements (resistors and inductors) could be done.
References


Appendices
Appendix A: Equations for Calculating Inductance of a Planar Spiral Inductor

The equations and formulas were used to calculate the approximant inductances seen in Table 1. The inductance values were solved for in MathCAD software. These equations were obtained from a paper by G. Burkett (2), but were modified for the calculating the inductance from the outer radius instead of the inner radius. So the input went from the inner radius, the number of turns, the line width, and the line spacing to the outer radius, the number of turns, the line width, and the line spacing.

\[ ro = ri + n(S + W) + W \]  

(18)

Was replace with:

\[ ri = ro - (n(S + W) + W) \]

(19)

\[ a = \frac{ro + ri}{2} \]

(20)

\[ c = ro - ri \]

\[ Ind = \frac{0.8n^2\cdot a^2}{6.0a + 10\cdot c} \]

(21)

Where \( ri \) is the inner radius, \( ro \) is the outer radius, \( W \) is the width of the line, \( S \) is the line spacing, \( N \) is the number of turns, and the inductance \( (\text{Ind}) \) is in nH. All the dimensions are in mils.