Stability studies of CdTe/CdS thin film solar cells

Bhaskar Reddy Tetali

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Stability Studies Of CdTe/CdS Thin Film Solar Cells

by

Bhaskar Reddy Tetali

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy
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Keywords: II-VI devices, illumination, thermal, lightsoak, stress, degradation, solar

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DEDICATION

This dissertation is dedicated to my parents and brother for their immense love and support in all my endeavors and to my dear wife for the help and motivation towards the end.
ACKNOWLEDGEMENTS

I am greatly indebted to my major professor, Dr. Chris Ferekides. His invaluable support and guidance during the course of this research and during some tough personal times is very much appreciated. I would also like to express my gratitude to Dr. Don Morel for his advice and support during my involvement in the compound semiconductor lab. I would like to thank my committee members Dr. Y.L. Chiou, Dr. Richard Gilbert and Dr. A.N.V. Rao for agreeing to be a part of the committee in evaluating my research.

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STABILITY STUDIES OF CdTe/CdS THIN FILM SOLAR CELLS

Bhaskar Reddy Tetali

ABSTRACT

CdTe/CdS solar cells have shown great potential for terrestrial solar power applications. To be commercially viable they need to operate efficiently for about 30 years. CdS/CdTe solar cells fabricated at USF have shown record efficiencies up to 16.5% [46]. This research involves the study of thermal stress (TS) and light soaking (LS) on the stability of high efficiency (>10%) solar cells. The change in key electrical parameters $V_{oc}$, FF, $J_{sc}$, A and $J_o$ are quantified for more than 2000 hours of stressing.

The device degradation was found to increase with stress temperature for TS. Below 100°C, the changes were due to collection and recombination losses. Above 100°C, “shunting” mechanisms were found to start affecting the device performance. A fast drop in performance within the first 500 hours was observed. It is believed to be due to an increase in deep-level Cu-related defects that increase with stress temperature. Diffusion of Cu$^{+}$ ions from the back contact along CdTe grain boundaries had been previously reported [16]. An increase in light/dark J-V crossover and bulk $R_s$ with stress time and temperature was observed. A slow degradation component attributed to Cu-related substitutional defect [23] formation/diffusion to the junction and CdS is proposed. This should compensate the CdS over time and increase its photoconductivity/resistivity.
An improvement in the current collection and FF within 100 hours of LS was observed. This is possibly due to the enhancement of Cu$_{i}^{+}$ diffusion into the junction and CdS during LS as previously reported [16]. A reduction in light/dark J-V crossover was observed, possibly due to an increase in CdS doping and reduction in the CdS/SnO$_2$ front contact barrier. However, a fast decrease in $V_{oc}$ and increase in recombination current was also observed in the first 1000 hours of LS. This is possibly due to the existence of higher concentration of Cu-related deep level defects at the junction. A larger decrease in $V_{oc}$ was found for LS than TS at the same operating temperature.

A continuous drop in performance over time is observed for both TS and LS. The existence of a slow degradation component involving the formation/diffusion of Cu-related substitutional defects at the junction and CdS is proposed. The concentration of this defect is probably not high enough in CdS for LS samples to affect their photoconductivity and cause light/dark J-V crossover in 2000 hours.
CHAPTER 1
INTRODUCTION

In a continuing quest to find alternate energy sources to fossil fuels, mankind has tapped into various other natural sources like solar-thermal, ocean-thermal, wind, nuclear, biomass, solar-photovoltaic etc.

A photovoltaic phenomenon is the conversion of light energy to electricity, exhibited by some semiconductor materials. Devices exhibiting this property are called solar cells. The commercial viability of solar cells depend on the following:

(1) cell efficiency,
(2) manufacturing cost, and
(3) operating lifetime.

To be economically competitive with conventional fossil fuels for terrestrial applications, solar arrays with conversion efficiencies in excess of 15% are required [34].

Semiconductors with bandgaps of around 1.5eV are optimum in terms of solar cell efficiency. This led to the study of materials with bandgaps between 1.1-2.0eV like Si, InP, GaAs, CdSe, CdTe, CIS, CIGS etc. for solar cell applications. Various device structures are used as solar cells, the most common being a p-n homojunction. Heterojunction devices, metal-semiconductor junctions (schottky diodes), metal-insulator semiconductor (MIS) structure etc. are other structures in use. Single crystalline silicon has a low absorption coefficient requiring a relatively large thickness to absorb light. High purity silicon is necessary for high efficiency cells but sophisticated processing technology has made the production costs too high. Direct gap thin
film semiconductors have high absorption coefficients. This means that a thin layer of a few microns (µm) of these films is sufficient to absorb the same amount of light, as it would take about a hundred microns (µm) of silicon. Thus, only a fraction of these materials is necessary compared to Si solar cells. Materials like amorphous Si, CdTe, CIS, CdSe etc. are direct gap semiconductors. Various low cost processing techniques such as close-spaced sublimation (CSS), evaporation, sputtering etc. are used to deposit these thin films in the polycrystalline form. They can also be deposited on various substrates (polymers, steel, glass, metal foils etc.) that are low cost and flexible leading to innovative new applications such as folding solar cell panels on satellites, solar cell blinds in homes etc. The low cost processing techniques and low material costs have made thin film technology lucrative. Study of these thin film materials is necessary to continue photovoltaic technology development.

Cadmium Telluride (CdTe) is one of the promising thin film materials identified for solar cell fabrication because of its high absorption coefficient and its near ideal bandgap of 1.45 eV, giving it high theoretical photovoltaic conversion efficiency. Cadmium Sulfide (CdS), with a wide bandgap of 2.42eV, has been found to be the most successful heterojunction partner as a n-type window layer material to date.

The fabrication of CdTe solar cells involves low-cost processing techniques. CdS/CdTe thin film solar cells with world record efficiencies > 15% have been obtained on high purity borosilicate glass (7059) substrates with solution grown CdS and CSS-deposited CdTe films [1,46] and large area module efficiencies > 10% have been demonstrated [46]. For the financial viability, it is necessary that thin film solar cells are stable and have a field lifetime of > 30 years. Outdoor testing of CdS/CdTe solar cell modules had shown great promise [38]. Thus, commercialization of CdS/CdTe thin film solar cells has shifted focus of the research community from efficiency to efficiency/stability. It is important to study the degradation rates of these devices so that we can predict and extend their lifetimes. Accelerated testing procedures must be
developed, as well as understanding mechanisms/processes that lead to degradation is essential to achieve this goal. The focus of this thesis is to contribute to these key aspects of CdS/CdTe technology i.e accelerated testing and degradation mechanisms.

A solar cell depends on sunlight for its operation. During this process there are two major factors influencing its operation. The primary factor is illumination. The secondary factor is the ambient temperature of the device. The device is expected to operate at temperatures over the ambient temperature due to heat dissipation. In this study the effects of the above two factors on device behavior and degradation are studied. The thesis is based on two key experiments (1) Temperature Stress (no light) (2) Light Soaking.
CHAPTER 2

SEMICONDUCTOR THEORY AND DEVICE PHYSICS

Semiconductors are materials with electronic properties in between metals and insulators. They can be elemental (Si, Ge), compound (ex: II-VI, III-V compounds i.e. CdS, CdTe, GaAs, InP etc.) or compounds (ex: Al$_x$Ga$_{1-x}$As, Hg$_{1-x}$Cd$_x$Te etc.). Semiconductor materials can be classified based on their structure and purity.

Materials are classified based on degree of atomic order as:

a) Amorphous (no recognizable order),

b) Polycrystalline, and

c) Crystalline (entire material is made up of atoms in an orderly array).

They can also be classified on purity as:

a) Intrinsic (pure material i.e no foreign atoms),

b) Extrinsic (impurity or dopant atoms present).

The extrinsic property of semiconductors is what makes them remarkable. It allows the modulation of electronic properties of these materials altering their conductivity useful for a wide range of applications. One key difference of semiconductors is that both electrons and holes act as current carrying species, unlike metals where only electrons exist for current transport. The dominant or majority carrier in the material determines whether a semiconductor is p-type (holes) or n-type (electrons).

“Doping” is the addition of impurity atoms to a semiconductor material to manipulate its electronic properties or current carriers. Silicon (Si) is a group IV element and in its intrinsic form
has four electrons contributing to its intrinsic carrier concentration \( (n_i \, \text{cm}^{-3}) \). Adding a group V element like Phosphorus (P – donor impurity) will cause an increase in electrons making the material n-type. A group III element like Boron (B – acceptor impurity) will cause a reduction in electrons i.e. increase in hole concentration of the material making it p-type. Thus, the conductivity of a semiconductor material can be controlled by the amount of dopant used. This remarkable discovery was instrumental in starting the “Digital Revolution”. Semiconductor materials and their compounds and alloys spurred the growth of electronic industry with applications like sensors, diodes, transistors to name a few.

The density of states (DOS), \( g(E) \) in a semiconductor shows how many states exist at a given energy \( E \). \( g_c(E) \) and \( g_v(E) \) define the number of available states in conduction and valence band.

A fermi function, \( f(E) \) specifies the probability that an available state at energy \( E \) is filled with an electron under equilibrium conditions.

\[
f(E) = \frac{1}{1 + e^{(E - E_f)/kT}}
\]

where \( E_f \) = Fermi energy or Fermi level, \( k = \) Boltzmann constant \((k = 8.62 \times 10^{-5} \, \text{eV/K})\), \( T = \) temperature in Kelvin (K).

The DOS, Fermi function and energy band diagram for an intrinsic semiconductor in equilibrium can be shown in figure 1. \( E_c \) is the conduction band, \( E_i \) is the intrinsic Fermi level and \( E_v \) is the valence band. The fermi level is present at the center of the bandgap with an equal number of electrons and holes being present.
Figure 1. DOS, Fermi Distribution, Carrier Density and Energy Band Diagram of an Intrinsic Semiconductor [38]

Figure 2. DOS, Fermi Distribution, Carrier Density and Energy Band Diagram of n-type Semiconductor [38]
For a n-type semiconductor the fermi level is close to the conduction band with the number of electrons higher than holes as shown in figure 2.

For a p-type semiconductor the fermi level is close to the valence band with the number of holes higher than electrons as shown in figure 3.

For a nondegenerate semiconductor i.e. \( E_v + 3kT < E_F < E_c - 3kT \), the carrier concentrations of electrons and holes are given by the expression,

\[
\begin{align*}
    n &= N_c e^{(E_F - E_c)/kT} \\
p &= N_v e^{(E_F - E_v)/kT}
\end{align*}
\]

where \( N_c \) and \( N_v \) are “effective” density of states in the conduction and valence band.

Highly doped semiconductors with \( E_F \) less than 3kT from the valence or conduction band are called degenerate semiconductors.

The above expressions for carrier concentrations in nondegenerate semiconductors can be modified as

\[
    n = n_i e^{(E_F - E_i)/kT}
\]
\[ p = n_i e^{(E_i - E_f)/kT} \]

where \(n_i\) is the intrinsic carrier concentration and \(E_i\) is the intrinsic energy level. Two other intrinsic carrier based expressions are

\[ n_i = \left( N_c N_v \right)^{1/2} e^{-E_g/2kT} \]

showing its relationship to temperature, where \(E_g\) is the bandgap of the semiconductor and

\[ np = n_i^2 \]

For doped semiconductors with \(N_D \sim N_A >> n_i\) or \(N_A - N_D >> n_i\) the expressions for carrier concentration simplifies to \(n \sim N_D\),

\[ n \approx n_i^2 / N_D \]

and \(n \sim N_A\),

\[ p \approx n_i^2 / N_A \]

It should be noted that all semiconductors at sufficiently high temperatures would become intrinsic as \(n_i >> (N_D - N_A)\).

### 2.1 Carrier Action

There are three types of carrier action occurring in semiconductors: (a) drift, (b) diffusion, and (c) recombination-generation. The carrier action will be discussed for electrons. The discussion can be extended to holes by analogy.

#### 2.1.1 Drift

Drift is defined as the motion of a charged particle in response to an electric field. When an electric field, \(E\) is applied to a semiconductor the force on the carriers accelerates the positively charged holes (+q) in the direction of the electric field and negatively charged electrons (-q) in the direction opposite to the electric field. The carrier in motion collides with ionized
impurities and thermally agitated lattice atoms causing scattering on a microscopic scale. However, a resultant motion occurs for each carrier type on a macroscopic level and is defined in terms of a constant drift velocity, $v_d$. It is defined by the expression,

$$ v_d = \mu_n E $$

where $\mu_n$ is the mobility of electrons. The electron current density, $J_{N|\text{drift}}$, is defined as

$$ J_{N|\text{drift}} = q\mu_n n E $$

The mobility of carriers can be influenced by three factors: (1) Thermally agitated lattice atom scattering or ionized impurity scattering can reduce carrier mobility, (2) Increased doping concentration monotonically can decrease mobility, and (3) Higher temperature can decrease the mobility for lower doped semiconductors but the sensitivity to temperature drops for higher doping levels.

Resistivity is defined as the inherent resistance of a material to current flow. It is shown as,

$$ E = \rho J $$

where $E$ is the electric field in the material, $J$ is the total current density and $\rho$ is the resistivity. In a nondegenerately doped n-type material, resistivity is shown as,

$$ \rho = \frac{1}{q\mu_n N_D} $$

### 2.1.2 Diffusion

Diffusion is a process where particles tend to redistribute from regions of high concentration to regions of low particle concentration due to their random thermal motion to obtain equilibrium by uniform distribution of particles in the system. Note that the diffusing species moves due to thermal motion and not due to interparticle repulsion and so do not have to be charged. The electron diffusion current density, $J_{N|\text{diff}}$, is

$$ J_{N|\text{diff}} = qD_n \nabla n $$
where $D_N$ is the electron diffusion coefficient and $Vn$ is the concentration gradient for electrons.

For similar concentration gradient of holes, the diffusion of holes occurs in the same direction but the current flow is opposite to the flow of electrons. As a result of electron or hole diffusion, a nonzero electric field exists inside a nonuniformly doped semiconductor under equilibrium conditions. However, the total carrier currents should be zero due to equilibrium conditions.

Thus,

$$J_{N_{\text{drift}}} + J_{N_{\text{diff}}} = 0$$

This can be simplified to,

$$D_N/\mu_n = kT/q$$

called the Einstein’s relationship for electron states.

Similar relationship can be generated for holes. Einstein’s relationship is deduced for equilibrium conditions but it can be extended to nonequilibrium conditions. It is not valid for degenerate semiconductors.

### 2.1.3 Recombination-Generation (R-G)

Generation occurs when charge carriers (electrons and holes) are created and recombination occurs when they are annihilated or destroyed. When light or heat energy greater than the bandgap of the semiconductor is absorbed, it excites an electron from the valence band into the conduction band generating an electron-hole pair called direct generation. The opposite effect of carrier annihilation is called direct recombination. This is however not the dominant mechanism in semiconductors. A second mechanism called indirect generation-recombination due to thermal excitation is the dominant process in semiconductors at all times. This occurs by the assistance of R-G centers present at energy levels between the valence and conduction bands.

Thus carrier generation is a two-step process of an electron exciting or trapped into an R-G center from the valence band before being excited into the conduction band. The opposite process
occurs for indirect recombination. R-G centers are physical impurity atoms or lattice defects present in the semiconductor material which form deep defects states close to mid-gap. It is desirable to keep R-G centers or traps to a minimum in functional devices. R-G processes are never-ending but to attain equilibrium the thermal recombination and generation rates balance each other.

Photo-generation process causes an equal number of electrons and holes to be created. The carriers generated are a function of distance the light has penetrated into the material and the wavelength of light.

Low-level injection in a semiconductor occurs when a perturbation like thermal excitation causes no significant change to the majority carrier concentration but increases the minority carrier concentration by many orders of magnitude. The change of minority carrier concentration (ex: electrons in p-type material) due to thermal R-G process is defined as

$$\frac{\partial n}{\partial t}|_{\text{thermalR-G}} = -\nabla n/\tau_n$$

where $\tau_n$ is the electron lifetime. This can be extended to holes in p-type materials. The minority carrier lifetime can be defined as the average time an excess minority carrier will live in a sea of majority carriers [39]. The average distance the minority carrier (ex: electron in a p-type material) can travel before recombination is defined as its diffusion length given by

$$L_N = (D_N \mu_n)^{1/2}$$

With the three main processes for carrier action introduced, it is relatively simple to put together each of these individual components to form the full set of continuity equations for carrier action in semiconductor materials. Further study of these continuity equations and the application of boundary conditions to individual cases of perturbation can be found in any semiconductor textbook [5].
2.2 p-n Junctions

When two oppositely doped semiconductors are brought in contact with each other, a p-n junction is formed. The p-type material has high concentration of holes and n-type material has a high concentration of electrons. When they are brought together, the diffusion of electrons from n to p-type material and holes from p to n-type material takes place. Thus diffusion current flows through the junction. But diffusing holes leave behind ionized acceptors and electrons leave behind ionized donors. The ionized acceptors and donors at the junction develop an electric field opposite to the diffusion current. The field initiates a drift current opposite to the diffusion current of each type of carriers. This continues until an equilibrium develops between the diffusion and drift current. The electric field exists in the region of uncompensated carriers called the depletion region or space charge region at the junction.

Figure 4. p-n Junction in Equilibrium [38]
Figure 4 shows p-n junction formed between a lowly doped p-type Si and a highly doped n-type Si. $x_p$ and $x_n$ are the depletion widths in the p and n side. The space charge region extends predominantly into p-type material due to its low doping to maintain charge neutrality. The direction of the electric field in the space charge region is from uncompensated donors in the n-region to uncompensated acceptors in the p-region. This results in a potential difference to exist between the two sides shown by built-in potential ($V_{bi}$). It can be calculated by the expression,

$$V_{bi} = kT/q \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

The band bending ensures the fermi level stays constant throughout the material as expected from a p-n junction in equilibrium.

2.2.1 p-n Junction Under Forward Bias (FB)

![Figure 5. p-n Junction Under FB](image)

When a p-n junction is forward biased (figure 5), the biasing potential causes majority carriers to flow towards the junction. This results in some donors and acceptors at the junction being compensated causing a reduction in depletion width. The built-in potential and band bending are also reduced causing an increase in minority carrier diffusion w.r.t the carriers in the
opposite direction. The non-equilibrium condition of bias causes the fermi-level to split into quasi fermi levels. The difference between fermi levels in n and p-type is equal to the applied voltage, \( V \). Thus, forward bias results in an increase in majority carrier transport across the junction, which increases the dc current in the diode.

### 2.2.2 p-n Junction Under Reverse Bias (RB)

When a p-n junction is reverse biased (figure 6), the biasing potential causes majority carriers to be pulled away from the junction. This results in more ionized dopants to be uncompensated in the space charge region. This increases the space charge region causing an increase in built-in potential and band bending at the junction. The majority carrier flow across the junction is minimal as shown and the difference in quasi-fermi levels is equal to the applied bias. The current present in the diode is the reverse saturation current of a reverse biased diode and is independent of applied bias.

Figure 6. p-n Junction Under RB [38]

When a p-n junction is reverse biased (figure 6), the biasing potential causes majority carriers to be pulled away from the junction. This results in more ionized dopants to be uncompensated in the space charge region. This increases the space charge region causing an increase in built-in potential and band bending at the junction. The majority carrier flow across the junction is minimal as shown and the difference in quasi-fermi levels is equal to the applied bias. The current present in the diode is the reverse saturation current of a reverse biased diode and is independent of applied bias.
2.3 Solar Cells

2.3.1 Introduction

The intensity of solar radiation in free space at the average distance of the earth from the sun is defined as the solar constant with a value of 1353 W/m². This is known as the AM0 condition which represents the solar spectrum outside earth’s atmosphere and is relevant for satellite and space-vehicle applications. Sunlight at its peak on the earth surface is represented by AM1 condition. AM1.5 condition (sun at 45° above the horizon), as shown in figure 7, is an energy weighted average for terrestrial applications, typically 1000 W/m². Spectral irradiance is the power per unit area per unit wavelength.

![Figure 7. Standard AM1.5 Solar Spectrum [5]](image)

When light is incident on a semiconductor, part of it is reflected and the rest is transmitted or absorbed. Light transmitted by a semiconductor follows the equation,

\[ I_t = I_o e^{-\alpha t} \]
where $I_0$ is the intensity of light incident on the semiconductor, $\alpha$ is the absorption coefficient of the semiconductor, $t$ is the depth of the semiconductor material from the surface of incidence and $I_t$ is light in the semiconductor at a depth, $t$, from the surface. The energy of incident light in terms of wavelength in the light spectrum can be obtained by the relationship,

$$\lambda = \frac{c}{\nu} = \frac{1.24 \mu m}{\hbar \nu}$$

where $\nu$ is the frequency in hertz, $h\nu$ is the photon energy in eV. If the energy of photons is less than the bandgap of the material, the light passes through the material. The photons are absorbed by the semiconductor if the energy is equal to or greater than the bandgap of the material. Energy, $E_g$ is sufficient in the creation of electron-hole pair and all the excess energy in the photon is dissipated as heat. The photon generated carriers are responsible for a rise in the photocurrent at the junction terminals.

2.3.2 Operation

One of the key applications of p-n junction diodes is solar cells. The photovoltaic effect is utilized for the operation of a solar cell. Under illumination, photo-generated minority carriers with sufficient lifetime travel towards the junction and get swept across the junction with its built-in field. These minority carriers reach the other side of the junction becoming the majority carriers. These excess majority carriers accumulate at the external contacts creating a voltage to build across the junction. This photo-generated voltage can be utilized to drive loads in various applications.

A solar cell operation is evaluated by its electrical performance characteristics described below.

Current-Voltage curves in the dark and light are shown in the figure 8.

The total current of an ideal solar cell is given by,
\[ I = I_L \left( e^{\frac{qV}{kT}} - 1 \right) - I_0 \]

where \( I_L \) is the light generated current or photocurrent. Short circuit current, \( I_{sc} \), is defined as the current flowing in the circuit with no voltage applied to the cell. The product of voltage and current in the fourth quadrant is negative signifying that this is the output power delivered by the solar cell.

![I-V Curves for a p-n Junction Diode in the Dark and Under Illumination](image)

**Figure 8. I-V Curves for a p-n Junction Diode in the Dark and Under Illumination**

Several parameters are involved in the characterization of a solar cell. The open-circuit voltage, \( V_{oc} \), is the voltage output at the device terminals with infinite load attached to it. This is physically equivalent to leaving the terminals of the device open or unconnected and measuring the voltage across it. \( V_{oc} \) is given by,

\[ V_{oc} = A_0 \left( \frac{kT}{q} \right) * \ln \left( \frac{I_{sc}}{I_0} + 1 \right) \]

where \( I_0 \) is the reverse saturation current or dark current at the junction and \( A_0 \) is the diode quality factor showing the “perfectness” of the junction. \( V_{oc} \) attains its highest value for a “perfect”
junction at $A_o = 1$ and it decreases as $A_o$ increases. This is because $A_o$ & $I_o$ are interdependent [7] and $I_o$ increases with increasing $A_o$, which results in lower $V_{oc}$.

$I_o$ should be as low as possible as can be seen in the expression. The bandgap of the material and temperature affect the dark current. $I_o$ can be decreased by increasing the bandgap or decreasing the temperature of the material thus increasing $V_{oc}$ [5]. This can be observed in the expression for $J_o (I_o/area$ of device) given below [7].

$$J_o = \frac{n_i WkT}{2(V_{bi} - V)\tau_e}$$

where $W$ is the width of depletion region, $k$ is boltzmann constant, $T$ is absolute temperature, and $\tau_e$ is the electron lifetime. Typical values of $J_o$ are $1.13e^{-11} \pm 1.6e^{-12}$ [7]. $J_o$ is influenced by two mechanisms: a) Recombination currents in the junction due to traps and deep level defects b) “shunting” leakage currents at the grain boundaries (GB) due to GB defects.

The diode quality factor, $A_o$, in the current equation, has also been found to be voltage dependent due to change in recombination center density. ‘$A_o$ vs Voltage’ for a theoretical homojunction is given in the figure 9.

![Figure 9. Diode Quality Factor, $A_o$ vs Voltage [7]](image-url)
The short circuit current, $I_{sc}$, is determined by the spectral response of the cell. A good spectral response over the entire visible spectrum signifies the generation of high currents. An ideal spectral response is a step function that equals zero for wavelengths $> E_g$ and unity for wavelengths $< E_g$ [8]. The material properties namely bandgap, absorption coefficient etc. directly influence the spectral response of a solar cell. It can be improved by increasing the diffusion length and reducing the surface recombination losses of charge carriers in the material.

In the figure 10 below, $I_{sc}$ & $V_{oc}$ are short-circuit current and open-circuit voltage of the cell and $I_m$ & $V_m$ are the current and voltage corresponding to the maximum power point. The maximum power point shows the maximum power that can be generated by a device. This power is the product, $I_m*V_m$. The fill factor, FF, is another important parameter of interest given by,

$$\text{FF} = \frac{V_m I_m}{V_{oc} I_{sc}}$$

Figure 10. Inverted Maximum Power Rectangle
The photovoltaic conversion efficiency ($\eta$) of a solar cell is a measure of light energy successfully converted to electrical energy.

$$\eta = \frac{P_m}{P_{in}} = FF \times I_{sc} \times \frac{V_{oc}}{P_m}$$

where $P_m$ is the area of the maximum power rectangle, $P_{in}$ is the incident power input to the solar cell.

Figure 11 below represents an equivalent circuit for a solar cell with series resistance, $R_s$ and shunt resistance, $R_{sh}$ acting on the device. For an ideal solar cell, $R_s \to 0$ and $R_{sh} \to \infty$. The series resistance depends on the ohmic losses in the front surface and the shunt resistance depends on the leakage currents.

![Equivalent Circuit of a Solar Cell with Series and Shunt Resistances](image)

Figure 11. Equivalent Circuit of a Solar Cell with Series and Shunt Resistances, $R_s$ & $R_{sh}$

Defects like pinholes in the solar cell are responsible for decrease in shunt resistance. $FF$ & $V_{oc}$ are the parameters directly affected by low $R_{sh}$. Low shunt resistance leads to current losses in the form of leakage current. Thus, $I_{sc}$ is also affected by $R_{sh}$. Series resistance is generally affected by contacts and resistance in the bulk of the device material. $FF$ & $I_{sc}$ decreases for high $R_s$ in a device.

Thus, the practical total current of a device is modified to
\[ I = I_0 \left( e^{\frac{q(V - IR_s)}{AT}} - 1 \right) + \frac{V - IR_s}{R_{sh}} - I_i \]

with the series and shunt resistance losses being applied to the ideal equation.

### 2.4 Heterojunction Solar Cells

The advantage of using a heterojunction (HJ) with a large band gap “window” material and a small band gap “absorber” material is to minimize the surface recombination losses that might otherwise dominate direct bandgap materials, enhance short wavelength response, and lower bulk series resistance (using thin-film materials). A “window” layer is a semiconductor material which is transparent to incident light with low absorption coefficient. An “absorber” layer is a semiconductor material with high absorption coefficient and capability to form a heterojunction with the window layer. The energy band diagram of an abrupt HJ and an HJ in equilibrium is shown in figure 12.

![Energy Band Diagram of Two Heterojunction Forming Materials](image)

Figure 12. Energy Band Diagram of Two Heterojunction Forming Materials
The two materials have different bandgaps, \( E_{g1} \) & \( E_{g2} \), different electron affinities, \( \chi_1 \) & \( \chi_2 \), different work functions, \( \Phi_{m1} \) & \( \Phi_{m2} \) and different permittivities \( \varepsilon_1 \) & \( \varepsilon_2 \). The energy required to remove an electron from the bottom of the conduction band, \( E_c \) is called electron affinity, \( \chi \) while the energy needed to remove an electron from the fermi level, \( E_f \) is called work function, \( \Phi_m \).
The basic model as a result of bringing two semiconductors together and lining up the fermi levels is shown in the figure 13. This model called the Anderson’s model assumes that no interface states are present and that current transport is via injection into the quasi-neutral region(QNR) or by recombination/generation in the depletion layer. The relation between various quantities is given by:

\[ \Delta E_c = (\chi_1 - \chi_2)q \]

\[ \Delta E_v = (\chi_2 - \chi_1)q + E_{g2} - E_{g1} \]

\[ qV_d = qV_{d1} + qV_{d2} = E_{g1} - n - p + \Delta E_c \]

The presence of discontinuities in the conduction band and valence band and possible interface dipole layers complicate the theory of HJs. The spike impedes the flow of minority carriers across the junction from the p-type to the n-type regions and the photocurrent will be reduced. The distribution of interface states may be electrically charged which further distorts the junction profile. Thus, the theory of HJs is not yet as firmly based as that for homojunctions.

The Anderson band profile is modified to include the effects of electrically charged interface states and dipoles. These changes, plus the introduction of various tunneling mechanisms bring the theory of HJ’s to follow experimental observations.

The carrier transport properties of HJs are dominated by phenomena in the interface region. The current transport in the depletion region is attributed to recombination, tunneling or to combination of both involving energy levels near the interface. The diffusion current has an exponential dependence on \( qV/kT \). The reverse saturation current \( J_o \propto n_i^2 \) meaning this mechanism is predominant in small bandgap materials with high \( n_i \) like silicon. \( J_o \) for recombination current is linearly dependent on \( n_i \) given by

\[ J_o = qn_iW/\tau_e \]

under the assumption that recombination occurs throughout the space charge region. The temperature dependence of \( J_o \) is given by
Tunneling current is given by

\[ J_t = B N_t \exp(-\alpha(V_{bi} + V)) \]

where \( N_t \) is the density of interface states, \( B \) & \( \alpha \) are constant with temperature, \( V_{bi} \) does not have a significant temperature dependence. Thus, tunneling current has weak temperature dependence.

2.4.1 Interface States

The effect of lattice mismatch between the two components of the HJ and impurities or defects introduced during fabrication result in extrinsic imperfection energy levels in the vicinity of the interface. These interface states may or may not be electrically active.

The lattice mismatch in HJs produces a periodic array of dangling bonds or edge dislocations. Such dangling bonds may be electrically active themselves or act as sites for impurity segregation. Interfaces can be efficient recombination centers because they introduce deep trap levels in the bandgap. They can also provide sites for quantum mechanical tunneling processes, which is important for current loss mechanisms across the junction. The interface traps degrade the performance of a solar cell and it becomes essential to produce HJs with low density of interface traps.

Electrically active interface states provide two mechanisms on HJs: a) \( Q_{ss} \), charge stored in the states distorts the band profile, raising or lowering the conduction band at the interface w.r.t. its equilibrium fermi level, b) The states provide a large density of recombination centers needed to explain the high \( J_o \) values observed. The effective interfacial recombination velocity \( S_1 \) quantifies the recombination behavior of the interface states. Both, \( Q_{ss} \) and \( S_1 \) vary with illumination and bias conditions.
2.4.2 Collection Function

In practical solar cells with lattice mismatch at the heterojunction, the quantum efficiency, $\eta_Q$ is decreased by forward bias, resulting in reduced fill factor and open circuit voltage. The analysis of these junctions is difficult due to lack of concrete information about the properties of the material in the depletion layer. The effect of bias and wavelength perturbation on the Q.E. expression is captured by a factor called collection function $H(\lambda, V)$ that multiplies the ideal cell current $J_L$, given by

$$J = J_o \exp\left(\frac{qV}{AKT}\right) - H(\lambda, V) J_{L_o}$$

where $J_{L_o}$ is the $H=1$ value of the light current. $J_{L_o}$ can be sometimes calculated by measurement at large reverse bias. The effect of $H<1$ is shown in figure 14, where the value of light generated current is reduced w.r.t. that generated in the absorber, especially in the forward bias. As a result $V_{oc}$ is reduced slightly and there is a considerable reduction in fill factor. The reduction in $J_{sc}$ is quite small in efficient cells.

![Figure 14. The Bias Dependence of Collection Function, H(V) [5]](image-url)
Collection function analysis of CdS/ CdTe cells was carried out by Mitchell et. al. (1977) [5] where major light absorption occurs in the CdTe layer of depletion region. No appreciable absorption takes place in the CdS window layer, and $J_o$ and $A$ are almost independent of light intensity. The collection function $H$ is a product of two factors: 1) $g(\lambda, V)$, representing absorption and recombination in the bulk, and 2) $h(V)$, showing the bias dependence of interfacial recombination loss.

The collection of photo-generated carriers from the thick quasi-neutral region (QNR) is given by:

$$g_1(\lambda, V) = \exp[-\alpha(\lambda) W_d(V)]/[1+1/\alpha(\lambda)L_n] \text{ for } x_p < x < \infty$$

The collection in the depletion layer of width $W_d(V)$, where the carriers are assumed to be swept by the junction field without suffering recombination losses is given by,

$$g_2(\lambda, V) = \{1- \exp[-\alpha(\lambda) W_d(V)]\} \text{ for } 0 < x < x_p,$$

where $x = 0$ is the interface and $g = g_1 + g_2$. The depletion width is almost in the CdTe layer due to heavy doping of CdS layer. Thus,

$$W_d(V) \approx \left[2\varepsilon_d(V_d - V)/qN\lambda\right]^{1/2} \approx x_p$$

The recombination of photo generated carriers at centers close to the disordered interface of the CdS/CdTe heterojunction was not found to be function of wavelength [5]. Mitchell et. al. used an approximate interfacial collection function, $h(V)$ given by,

$$h(V) = 1/[1+(S/\mu E)]$$

where the electric field at the interface is $E = 2(V_d - V)/ W_d(V)$, $S_i$ is the interfacial recombination velocity and $\mu$ is the local mobility.
Figure 15. Bias Dependent SR of a CdS/CdTe Heterojunction [5]

The SR in figure 15 showed that \( h(V) \) was constant with wavelength. The shape of the SR curve was wavelength dependent and voltage independent which means \( g = g(\lambda) \) and \( g \neq g(V) \). Thus, the change in \( H(\lambda,V) \) was observed to be from bias dependent interface recombination losses. Forward bias may influence the lifetime in the absorber QNR and alter the J-V characteristics.

2.4.3 The Effect of Illumination and Temperature on Cell Efficiency

The effect of illumination on the quasi-fermi levels of electrons and holes was illustrated by Fahrenbruch and Bube as shown in figure 16.
A forward biased heterojunction with a p-type absorber layer is shown. The depletion widths $x_p$ and $x_n$ are the depletion regions on the p and n side from the junction interface $x_i$. $E_{fp}$ represents the equilibrium Fermi level on the p-side and $E_{fn}$ is the equilibrium Fermi level on the n-side. Both should be at the same level at equilibrium but the offset shown indicates that the device is forward biased and is equal to the applied bias. $E_{fno}$ in the p-type material is the equilibrium fermi level of minority carrier electrons on the p-side. During illumination, energy is absorbed by the p-type absorber material and generates an equal number of electron-hole pairs. The majority carrier hole concentration is not significantly altered so the $E_{fp}$ remains unchanged. However, there is a significant increase in the minority carrier electrons which changes the electron Fermi level represented by the quasi-fermi level, $E_{fno}$ on the p-side.

Illumination level and/or wavelength have been found to vary the diode $J_o$ and $A$ of some heterojunctions, MIS cells and Cu$_x$S/CdS cells. This occurs when trapping centers at or near the
junction are not in good thermal communication with the conduction or valence bands and can have their occupancy and hence charge changed by illumination. Optical absorption by states at the interface, in the bulk material near the junction could cause the change in $J_o$ and $A$. This change in Cu$_x$S/CdS structure is due to the change in ionized donor or acceptor density on illumination.

The temperature dependence of the solar efficiency can be interpreted in terms of the individual temperature dependence of $J_{sc}$, $V_{oc}$ and FF. The primary dependence of $J_{sc}$ on temperature is through the minority carrier diffusion length: $L = (\mu kT \tau/q)^{1/2}$. A cell with high initial QE is not substantially affected by changes in $L$ with temperature. The changes in minority carrier lifetime with temperature depends on the relative location of the energy levels of the recombination centers and the quasi-Fermi levels along with the dependence of the recombination cross sections of the centers themselves.

The $V_{oc}$ and FF decrease with temperature primarily due to changes in $n_i$. $J_o$ increases exponentially with temperature causing $V_{oc}$ to drop almost linearly with increasing $T$.

$$J_o = BT^3(D/\tau)^{1/2}\exp[-E_g/kT]$$

$$V_{oc} = (E_g/q) - (kT/q)\ln[D/\tau]^{1/2}T^3B/J_{sc}$$

where $B$ is a temperature independent constant, $D$ is the debye length and $\tau$ is the minority carrier lifetime. FF decreases quite strongly with temperature. Contacts may become non-ohmic at low temperatures causing large losses in FF.
CHAPTER 3

REVIEW OF CdTe/CdS THIN FILM SOLAR CELLS

This chapter reviews the properties of all the materials in a CdS/CdTe heterojunction solar cell which are relevant to device performance and stability. The superstrate device structure (figure 17) used in this research consists of a front contact layer (SnO₂), n-type layer (CdS), p-type layer (CdTe) and a back contact layer (graphite paste doped with HgTe:Cu) on 7059 borosilicate glass substrate.

Figure 17. Superstrate Structure

3.1 Front Contact

The properties expected of a front contact material are high transmission, high conductivity, efficient transport of carriers collected from the p-n junction to the device terminals (i.e. no surface recombination losses) and chemical stability to subsequent processing conditions.
They are called transparent conducting oxides (TCO) and as the name suggests are typically made from highly doped oxides like fluorine doped Tin Oxide (SnO$_2$:F), Tin doped Indium Oxide (ITO), Fluorine doped Indium Oxide (INO), Cadmium Stannate (CTO). Routine high efficiency CdS/CdTe solar cells have been most successfully fabricated using SnO$_2$ as TCO [28]. Device with record efficiency of 16.5% was achieved using a CTO/ZTO layer [46]. A bilayer of low resistance SnO$_2$:F deposited on glass followed by high resistance SnO$_2$ is used in the current research. A typical film thickness of 0.7-1µm and sheet resistance of 8-10Ω was used. Typical doping concentrations of $10^{19}$-$10^{20} /\text{cm}^3$ are obtained making it a degenerate. SnO$_2$:F has been found to be chemically non-reactive at its interface to CdS and no interdiffusion was observed [28].

3.2 CdS Layer

The main function of a window layer in a superstrate structure is to be a good heterojunction partner to the p-type absorber layer with minimal lattice mismatch to minimize defects like interface states and dangling bonds at the metallurgical interface, and be transparent to incident light. Both these roles have been successfully played by cadmium sulfide resulting in fabrication of high efficiency thin-film CdTe/CdS solar cells. In spite of the 9.7% lattice mismatch between hexagonal CdS and cubic CdTe, high efficiency devices are made with this junction probably due to interdiffusion at the CdS/CdTe interface. The CdS$_x$Te$_{1-x}$ layer formed during this interdiffusion will be discussed in Section 3.4. The CdS layer thickness has to be optimized to make it as thin as possible to sustain the heterojunction. This is required to minimize the photocurrent losses due to absorption in CdS. Such interdiffusion is enhanced by the post-deposition CdCl$_2$ heat treatment [47]. It is thought to enhance CdTe grain growth, help grain recrystallization and improve p-doping (by creating a shallow acceptor complex, $V_{Cd} - Cl_{Te}$).
Cadmium Sulfide (CdS) gets its n-type conductivity due to the presence of sulfur vacancies (native defects formed during processing), which act as ionized donors. Typical donor concentrations of $10^{16}$-$10^{17}$/cm$^3$ are obtained. The doping concentration of this layer can be altered by acceptor type impurity and defect compensation. Intrinsically Cd$_i^{++}$ acts as a donor like defect and S$_i^{--}$ will exist as an acceptor like defect. The species of interest in this study are Cu, Cl and their defect complexes. Cu can exist in many forms in CdS. As an interstitial, Cu can exist as a neutral atom or as an ionized donor Cu$_i^{+}$. Copper is also known to occupy cadmium vacancies V$_{Cd}$, acting as an ionized acceptor like defect. Similarly Cl can exist as a neutral atom or a more stable Cl$_i^{--}$ as an acceptor. Cl also substitutes sulfur vacancies forming donor like defects. Several acceptor like defect complexes have also been identified to exist such as [Cu$_{Cd}$-Cl$_{Te}^{+}$], [V$_{Cd}^{2-}$-2Cl$_{Te}^-$], [Cu$_{Cd}$-$Cu_i^{+}$] etc. The increase in acceptor like defects in CdS will result in compensation effects that increase the CdS resistivity. This work as well as other research groups [21] have shown large accumulation of Cu and Cl at the junction interface and in CdS. This is possibly due to higher GB and lattice defects at the metallurgical interface and the fact that CdS grains are much smaller compared to CdTe resulting in a larger grain boundary area. Thus ionic dopant species like Cu and Cl and their complexes accumulate at these interfaces and GBs due to GB diffusion. CdS film resistivities of $10^6$Ω-cm as deposited and $10^2$-$10^3$Ω-cm after CdCl$_2$ anneal were observed [25].

### 3.3 CdS/TCO Interface

The front region of the CdS/CdTe solar cell has been studied extensively by Dan Oman [7] on USF samples. A light sensitive series resistance component was observed in the CdS layer. Using a 450nm band pass filter (primarily absorbed in CdS layer), samples were exposed to blue light varying in intensity from dark to 1 Sun. This showed $R_s$ variation from 1.85Ω in the dark to 1.45Ω at 1 Sun intensity. This behavior could not be repeated using a red light of 600nm or for
very thin CdS layers with >30% transmission at 450nm. Thus some excess CdS bulk beyond the metallurgical junction is essential for the light sensitivity to occur, meaning all CdS should not be utilized in the formation of the CdS$_x$Te$_{1-x}$ layer. Exposure to 10 times lower intensity of blue light than red light, had shown smaller J-V crossover for blue light due to its absorption in CdS. This shows the photoconductive nature of CdS and its sensitivity to blue light. A device was forward biased to 0.885V (the turn-on portion of light J-V) and exposed to equal intensities (1/10000$^{th}$ of 1 Sun) of various wavelengths of light. The highest increase in light generated current was observed at wavelengths <500nm which represents light absorbed in the CdS layer. Based on these observations the dark vs light J-V crossover was modeled to be a front contact “leaky” diode opposite to the main junction of CdTe/CdS [7]. A contact barrier of 0.2eV is expected between the fermi level in CdS and SnO$_2$ due to electron affinity mismatch. In the dark when the main junction $R_{sh}$ is $10^6$-$10^9$ $\Omega$, the front contact diode $R_{sh}$ is approximated at $10^3$ $\Omega$. Under illumination, when the main junction $R_{sh}$ decreases to $10^3$ $\Omega$, the front contact diode $R_{sh}$ possibly drops to ohms or tenths of $\Omega$ or less. At this point the current will bypass this diode going through a light activated shunt path [7].

The front region of CdS/CdTe solar cells has also been modeled by Agostinelli G. et. al. [36]. The model proposes the presence of a modulated barrier photodiode (MBP) in series with the main junction at the front as a consequence of compensation of CdS, which induces crossover of light/dark J-V and in worst cases rollover. It also proposes the presence of a buried homojunction (type converted CdTe intermixing layer).
Figure 18. General Band Diagram for the Proposed Model [36]

The CdS layer (compensated by acceptors) in between the n-type CdTe\(_{1-x}\)S\(_x\) layer and n-type ITO maybe intrinsic or maybe slightly p-type. In these conditions, the CdS layer is fully depleted and is sandwiched between degenerate ITO (N\(^+\)) and n-doped CdTe\(_{1-x}\)S\(_x\) layer. This creates a hump in the band diagram (figure 18) acting as a potential barrier for electrons and potential minimum for holes. Accumulation of Cu in CdS from contacts can result in the compensation of CdS by its acceptor type defects. Under illumination, photogenerated holes in CdS will move towards this minimum. They can then recombine with electrons trapped by acceptor defects causing an “electronic doping” effect in CdS (figure 19).
Figure 19. Light Induced Barrier Modulation: Accumulation of Photogenerated Holes Neutralizes Some of the Ionized Negative Charge in the Layer and Leads to Lowering of the Bulk Barrier [36]

Both the above models explain observations in CdS/CdTe devices and are actually interrelated. The presence of an entire layer of type-converted CdTe intermixed layer has been disproved for typical USF devices by Visoly-Fisher et al. [20]. Conversion of CdS to p-type has been excluded by AES, which showed Te/S ratio in the CdS layer of <0.6. A ratio of 0.8 is required to type convert CdS.

3.4 CdS/CdTe Interface

The CdS/CdTe interface is one of the critical device regions in CdTe solar cells. Te-rich and Cd-rich ternary compounds of CdTe and CdS have been reported by various groups at this interface [50]. The intermixing of CdS and CdTe is believed to be enhanced by CdCl₂ heat
treatment [21, 47]. This intermixing was found to correlate with high efficiency CdS/CdTe devices. High CdTe deposition temperatures are favorable towards formation of high quality junctions [50]. The intermixed layer is believed to improve device performance by:

a) Reducing the lattice mismatch between CdTe and CdS

b) Reducing the interface defect density and decrease in leakage current caused by tunneling and interface recombination.

However, the intermixed layer could also have the following detrimental properties that can decrease the device performance [21].

a) Reduction in window layer transmission reducing maximum J_{sc}

b) Doping level changes causing junction and SCR width variation possibly reducing V_{oc}

c) Composition and bandgap changes cause shift in junction location and affect the built-in voltage

d) Rapid GB diffusion (ex: S in CdTe) may cause increased shunting due to reduced bandgap or formation of metallic-like alloy causing performance degradation

This shows that the CdS/CdTe interface and its properties are not clearly understood at this time and its influence on device stability still unknown.

The intermixing layer CdTe_{1-x}S_x alloy with x<0.25 is known to have smaller bandgap than CdTe as shown in figure 20 [26]. The width, structure and composition of this layer is found to depend strongly on the post-deposition treatment parameters and the individual layer deposition process.
Study of USF devices has also shown that high resistivity (HR) SnO₂ in the bilayer SnO₂ used is electronically similar to CdS and helps support the junction photo-voltage or band bending [20]. This means the thin CdS layer is fully depleted with space charge region extending into HR SnO₂ layer. It was also shown that the photovoltaic and metallurgical junctions coincide.

### 3.5 CdTe Layer

The primary purpose of an absorber layer is to efficiently collect the light energy incident on it and convert it to electricity. CdTe was found to be an ideal junction partner for CdS with an electron affinity mismatch of only 0.3eV. The effect of this lattice mismatch is alleviated by the formation of an intermixing layer of CdS and CdTe enhanced in the presence of CdCl₂. CdTe can exist both as n-type and p-type material. The presence of V₉ as native defects is what makes it p-type. It has a high absorption coefficient of $10^4$ to $10^5$ cm⁻¹ which means only 1-2μm thick CdTe is enough to absorb all the incident light above its bandgap of 1.44eV. CdTe is therefore one of the leading materials for solar cell applications with a very high theoretical photovoltaic conversion efficiency [8]. Typical absorption coefficients for CdTe is shown in figure 21.
Figure 21. Typical Absorption Coefficient for CdTe and CIGS Solar Cells [26]

The penetration depths of photons for different wavelengths (inverse of absorption coefficient) varies from \(~0.1\mu m\) for blue light of 450nm, \(~0.2\mu m\) for 600-700nm, \(~0.47\mu m\) for 788nm, \(~1.4\mu m\) for 820nm to 34.6\mu m for 855nm [26]. Typical dopant concentrations are \(~10^{14}\) to \(10^{15} \text{ cm}^{-3}\) for polycrystalline CdTe which is limited by the number of V_{Cd} present in intrinsic CdTe [9]. The limiting factor for extrinsic p-type doping of CdTe is not having a dopant with both high solubility and shallow acceptor level [49]. Some of the defects have shallow acceptor levels but their defect formation energies are too high (eg. CdTe:N, CdTe:P). Other dopants have low formation energies but their acceptor level is too deep (eg. CdTe:Cu) [49]. This being two orders of magnitude less than its heterojunction partner CdS, the junction is one-sided with the depletion region extending \(~2\) to \(3\) microns into the CdTe layer. This is advantageous for carrier collection since most of the light is absorbed very close to the space charge region of the junction. Structurally CdTe is known to form columnar grains of \(>1\mu m\) in size [50]. Unlike single crystal material, a polycrystalline thin film of CdTe will have grain boundary (GB) effects also contributing to the device performance. GBs have been known to act as traps and recombination centers for minority carriers, potential barriers for the majority carrier transport or as shunt paths.
causing substantial reduction in device performance [23]. The interaction of GBs with free charge carriers, native point defects such as vacancies and interstitials, free charge carriers in the bulk etc. are to be considered. The conduction properties of the material are significantly altered when permanent trapping of charge carriers at GB form a potential barrier that hinders the flow of free carriers through the grain boundary. GB defects may act as gettering sites for undesirable impurities in the bulk thus improving the bulk electronic properties. This has been confirmed by studies of Visoly-Fisher et. al. on USF samples [18]. It was shown that there is a barrier for hole transport across GBs causing GBs to be depleted.

Figure 22. Simultaneously Collected AFM Topography and CP-AFM Current Mapping Images of the Standard CdTe/CdS Cell

It was also observed that inversion of GBs after CdCl$_2$ treatment occurs possibly due to the presence of Cl$_{Te}$ donor like surface defects. This should reduce the current collection of the device. However polycrystalline CdTe/CdS solar cells have been found to perform better than their single crystal counterparts with higher current collection. Simultaneous atomic force microscopy (AFM) and conductive probe AFM (CP-AFM) measurements have shown (figure 22) surprising result of higher currents at the GBs than bulk CdTe crystals [17]. The current transport in polycrystalline CdTe solar cells have been modeled as shown in figure 23.
Figure 23. Schematic Illustration of Electron Energy (vertical) vs Spatial (horizontal) Coordinate of CdTe Grains in the Solar Cell [17]

The CdS is in front of the plane of the paper. Blue/red circles show holes/electrons, and blue/red arrows show their direction of movement. $E_c$ and $E_v$ stand for the conduction band bottom and the valence band top. The scheme illustrates proposed electronic energy variations near CdTe GBs, resulting in the separation of photo generated electron-hole pairs near GBs and “funneling” of electrons into and their channeling along GB core [17]

It is proposed that the electrons are drawn to the depleted GB core and flow along GBs to the junction while holes are transported through the grain bulk towards the back contact. The charge separation along with reduced recombination in grain bulk (reduced defects in bulk) and in GBs causes reduction in net recombination and improved collection of photogenerated carriers.

### 3.6 Back Contact

The formation of a stable, low resistance contact to p-type CdTe is a major challenge due to high work function of CdTe and the inability to obtain low resistivity (high level doping) CdTe. The work function of CdTe is $\sim 5.9\text{eV}$. The work function of commonly used metals range from 4.2-5.6eV. Thus no metal exists that can make a barrier free or at least quasi-ohmic contact to CdTe. Most metal contacts to CdTe are rectifying.
Doping polycrystalline CdTe at the contacting interface is problematic due to the existing potential barrier. The barrier height is controlled by impurity/dangling bond states and carrier density in the bulk adjacent to the barriers. Compensation of the dopant by oppositely charged grain boundary states also exists. The effective carrier density and effective mobility are reduced due to the presence of grain boundaries. This barrier height has to be minimized to reduce the surface recombination velocity and improve device efficiency.

The most common and successful approach to obtain ohmic or pseudo-ohmic contacts to CdTe has been to modify the CdTe surface to make it Te rich or Cd deficient (P⁺). This promotes tunneling carrier transport between the semiconductor and metal. Graphite paste doped with HgTe:Cu is used in this research and has been previously used to obtain world record efficiencies [1]. Formation of p-type Cu₂Te and Hg₁₋ₓCdₓTe interlayers help tunneling of holes across the contact. Details of other contacting procedures and contacts can be found in [24].

3.7 Factors Affecting Stability

It has been well known that routine fabrication of high efficiency CdTe/CdS devices has been only possible with the help of Cu doped back contacts. Some groups have demonstrated Cu free back contacts with high efficiencies recently [21,24], however their long term stability has not yet been established. Preliminary stability studies have shown back contact degradation under thermal stressing [24]. Research to-date have proposed that Cu, Cl and their defect complexes are the key factors of degradation [21]. The most suspected cause of cell instability is the diffusion of Cu from the back contact into the junction and the CdS region. Cu is known to be a fast diffuser in CdTe. Grain Boundary (GB) diffusion is the most likely mechanism of transport of Cu into the cell junction. Because Cu⁺ and Cd²⁺ ions are similar in size, Cu⁺ was thought to substitute readily for Cd²⁺ in CdTe. However lattice defects are slow diffusers compared to defects at GB. Cu doping of the entire CdTe layer should be observed and indeed Cu has been detected at the
CdS/CdTe interface. Cu was proposed to form recombination centers and shunt pathways limiting the lifetime of the cell.

It has already been established that GB diffusion is the main mode of Cu diffusion into the CdTe, CdS layers and CdTe/CdS interface [21] as shown in figure 24.

![Figure 24. Comparison of Cu SIMS Profiles in CdTe with Different Degree of Crystallinity [21]](image)

Within polycrystalline CdTe films smaller grain sizes have shown several orders of magnitude higher Cu concentrations throughout the whole film. The same GB diffusion mechanism is believed to be the mechanism of Cl movement into the CdTe layer and the junction interface during CdCl₂ treatment.

### 3.8 Spatial Variation of Device Parameters in Polycrystalline CdTe/CdS Solar Cells

Uniformity of solar cell parameters was previously studied and reported [25] on high efficiency USF samples. Scanning for V<sub>oc</sub>, J<sub>sc</sub>, FF, R<sub>sh</sub> with a helium-neon laser of spot size diameter 1mm at regions 1mm apart on the cell showed localized “good” and “bad” regions.
Localized micro defects like pinholes, GB defects are responsible for the “bad” regions which also affect the overall performance of the device. This was confirmed by work of Rangaswamy A [22]. A high efficiency CdTe/CdS device ($V_{oc} > 800\text{mV}$, $FF > 60\%$) was found to degrade severely after 1000 hours of light stress ($V_{oc} \sim 270\text{mV}$, $FF \sim 29\%$). Upon breaking up the device into two halves, the first half showed $V_{oc} \sim 810\text{mV}$, $FF \sim 64\%$ and the second half showed $V_{oc} \sim 160\text{mV}$, $FF \sim 28\%$. This shows the necessity of optimizing the fabrication process and starting materials/device layers to prevent such defect formation. This goal is more complicated due to the fact that low cost processing techniques are required to make polycrystalline solar cells cost effective which inherently are more defect prone. Device structure has to be optimized to prevent such localized defect formation even during device operation to enhance device stability.

Further investigation into spatial parametric variation with spot sizes up to $1\mu\text{m}$ was reported by Hiltner J.F [26]. Large number of local electrical defects were found in CdTe cells causing a reduction in current collection. The most common cause of local reductions in current collection was due to local variations in series resistivity of the material. These high resistivity regions appear to be more strongly alloyed with sulfur as measured by the degree of bandgap variation. Wavelength dependence of collection near and slightly below the CdTe bandgap was attributed to local variations in the bandgap due to formation of CdTe$_{1-x}$S$_x$. This observation is supported by PL measurements on CdTe by others [26]. Comparison of identical samples with and without post deposition CdCl$_2$ treatment has shown that CdCl$_2$ treatment improves uniformity of collection for photons with energies above the CdTe bandgap. However, the treatment was also found to increase the spatial variation of CdTe bandgap. The low bandgap regions did not show evidence of high resistance suggesting that lower bandgap regions do not directly increase the series resistance. Elevated thermal stress produced local increases in the resistivity of the material in regions of lower bandgap i.e. higher sulfur alloying. The correlation between variations in bandgap and increase in series resistance is possibly due to non-uniform penetration of both
CdCl₂ (which enhances the alloying) and of contaminants from the back contact. This suggests the same root cause exists for both lowering of bandgap regions and the formation of high resistance regions during contact anneal or thermal stressing [26].

3.9 Defects in CdTe/CdS Solar Cells

Imperfections in a crystal lattice are called defects. Individual atomic or complex-related defects are called point defects. The following three defects fall into this category:

1) Vacancies – missing atom from the lattice
2) Interstitials – extra atom between normal lattice sites
3) Substitutionals – an atom occupying another element’s lattice site

Vacancies and self-interstitials are called intrinsic defects while substitutional and external interstitial atoms are called extrinsic defects. Schottky defects involve vacancies like an anion or cation or both missing from the lattice (ex: Cd or Te vacancy in CdTe). Frenkel defects are formed when an atom migrates from its lattice site to an interstitial position (ex: Cadmium vacancy and cadmium interstitial). Point defects are the main dopants in thin film semiconductors. Complex defects formed by combination of atomic defects also exist such as \([\text{Cu}^-_{\text{Cd}}-\text{Cl}^+_{\text{Te}}], [\text{V}^{2-}_{\text{Cd}}-2\text{Cl}^+_{\text{Te}}], [\text{Cu}^-_{\text{Cd}}-\text{Cu}^+_i]\) etc.

Dislocations are 1-D defects and are caused by a line of defects. Grain boundaries, stacking faults, interfaces and twin boundaries are 2-D defects. Grain boundaries are a source of high densities in polycrystalline CdTe [30].

The defects of interest for this study are intrinsic cadmium vacancies, extrinsic copper interstitials and complexes as well as chlorine related defects. The density of these defects found in CdTe/CdS polycrystalline structures have been found to exceed or equal intrinsic layer doping concentrations of CdS or CdTe. The formation energy of a particular defect is the change in
energy of the crystal between initial and final states. Thus, a defect with high formation energy is less likely to form or exist.

Figure 25 shows the defect sites present in the heterojunction CdS/CdTe structure.

![CdS/CdTe Structure](image)

CdTe is a called a defect semiconductor because its native defects are responsible for its electrical properties i.e. donor-like cadmium interstitial, \( \text{Cd}^+ \) (donates an electron to the lattice) for its n-type conductivity, and acceptor-like cadmium vacancies, \( \text{V}_{\text{Cd}}^- \) (accepts an electron from the lattice) account for its p-type conductivity. Various native defects possible in CdTe are Cadmium vacancy, \( \text{V}_{\text{Cd}}^{-1/2} \), cadmium interstitial, \( \text{Cd}^{1/2+} \), tellurium vacancy, \( \text{V}_{\text{Te}}^{+1/2} \), tellurium interstitial, \( \text{Te}^{1/2-} \). These can also form complexes with residual impurities or dopants. The existence of metastable states [41] have been found changing from shallow to deep traps or vice versa with or without change in charge [42]. Illumination and thermal excitation could cause these metastable transitions. Deep Level Transient Spectroscopy (DLTS) is one way to identify these defects, though it is not as straightforward as in single crystalline structures.

Cu and Cl are common elements found in CdTe as both are used during the fabrication process. Cu is used during the back contact process and Cl is used during the CdCl\(_2\) high temperature anneal. The diffusion of Cu to the junction is believed to be responsible for the
instability of CdTe/CdS solar cells [21]. The presence of Donor-Acceptor pair transitions due to cadmium vacancy coupled to some unknown donor is expected. Various Cu complexes are also likely to be formed (Cui\(^+\)-V\(_{Cd}\)). These complexes could act as acceptor states to explain the observed increase in carrier concentration with Cu diffusion. Light Soaking or electric field could split the complexes to Cui\(^+\)+V\(_{Cd}\), (2Cui\(^+\)-V\(_{Cd}\)) or Cu clusters to reduce the carrier concentration and formation of traps and recombination centers.

This discussion underscores the complex defect mechanisms involved in the polycrystalline CdS/CdTe structure. The degradation mechanisms are neither quantified nor completely understood at this time. A review of existing literature on the defects in CdTe/CdS solar cells is discussed next.

Komin, V [23] had studied the defects present in CdTe/CdS solar cells by DLTS technique. A summary of all defects are shown in table 1 and figure 26.

Table 1. Deep Levels Found in the Polycrystalline CdS/CdTe Thin-Film Solar Cells [23]

<table>
<thead>
<tr>
<th>EA [eV]</th>
<th>(\sigma_n ) [cm(^{-2})]</th>
<th>Chemical nature</th>
</tr>
</thead>
<tbody>
<tr>
<td>(H1) 0.120</td>
<td>1.0E-16</td>
<td>Trigonal symmetry (A_2)-center ((V(<em>{Cd})(^{2-}) - Cl(</em>{Te})(^+))</td>
</tr>
<tr>
<td>(H2) 0.140</td>
<td>4.0E-17</td>
<td>((V(<em>{Cd})(^{2-}) - Cui(^+)), (2Cui(^+) - V(</em>{Te})) \text{ or complexes involved } \frac{V(<em>{Cd})(^{2-})}{V(</em>{Te})(^+)}</td>
</tr>
<tr>
<td>(H3) 0.200</td>
<td>3.0E-16</td>
<td>growth process</td>
</tr>
<tr>
<td>(H4) 0.320</td>
<td>8.0E-16</td>
<td>growth process, Te(<em>{Cd})(^-)-complex, after CdCl(<em>2) anneal: Te(</em>{Cd})(^-) \rightarrow V(</em>{Cd})(^{2-}) + Te(_i)</td>
</tr>
<tr>
<td>(H5) 0.330</td>
<td>8.0E-18</td>
<td>Ag(_{Cd})</td>
</tr>
<tr>
<td>(H6) 0.270 – 0.35</td>
<td>3.9E-19 – 9.5E-16</td>
<td>(\text{Cu}<em>{Cd})(^-), (Cui(^+) - 2Cui(</em>{Cd}))(^-)</td>
</tr>
<tr>
<td>(H7) 0.430</td>
<td>1.0E-14</td>
<td>isolated V(_{Cd})(^{2-})</td>
</tr>
<tr>
<td>(H8) 0.760</td>
<td>6.0E-13</td>
<td>complex of V(_{Cd})(^{2-}) and an impurity</td>
</tr>
<tr>
<td>(E1) 0.140</td>
<td>5.0E-18</td>
<td>DX(<em>2)-state of ((V(</em>{Cd})(^{2-}) - Cl(_{Te})(^+)); Cui(^+)-related</td>
</tr>
<tr>
<td>(E2) 0.640</td>
<td>2.0E-13</td>
<td>isolated Cd(_{2})(^{2+})</td>
</tr>
<tr>
<td>(E3) 0.790</td>
<td>4.0E-14</td>
<td>A-center ((V(<em>{Cd})(^{2-}) - 2Cl(</em>{Te}))(^0)</td>
</tr>
<tr>
<td>(E4) 1.100</td>
<td>1.0E-13</td>
<td>isolated V(_{Te})(^+)</td>
</tr>
</tbody>
</table>
Figure 26. Summary of Deep Levels Observed in the Polycrystalline CdS/CdTe Thin-Film Solar Cells [23]

Standard CdTe/CdS solar cells fabricated at USF have shown defects H4-H6 and H8 [23].

Admittance spectroscopy studies of unstressed and stressed CdTe solar cells showed that the total concentration of different types of traps can exceed the doping level of CdTe [33]. The characteristic times of traps vary widely along with their energy level positions. High concentrations of slow (deep) traps can be attributed to grain boundary states. Trap bands found with energies $E_v + 0.35eV$ are attributed to $\text{Cu}_{\text{Cd}}$ substitutionals. The energy level of these traps is a band with a width of about 0.05eV.

Self-compensation is another mechanism that is present in the devices. Species like Cu have been found to self compensate. This means there are equal levels of Cu-related donor defect states (ex: Cu interstitials) as acceptor defect states (ex: cadmium substitutionals) in a material
and thus the net doping concentration of the material remains unchanged. Studies on single crystal CdTe intentionally doped with Cu was found to self-compensate 99% of the time for concentrations up to $1 \times 10^{19}$ cm$^{-3}$ [30].

Even in the presence of complex degradation mechanisms, there is evidence that polycrystalline CdS/CdTe solar cells are stable under outdoor (figure 27) and indoor (figure 28) testing [45,4]. This data reiterates the promise shown by CdTe for fabrication of thin film solar cells and emphasizes the need to understand the underlying degradation mechanisms to help sustain its long term usage.

![Figure 27. Outdoor Performance of CdTe Submodule [45]](image1)

![Figure 28. Performance History of Two CdTe Submodules [4]](image2)
3.10 Current literature on Stress Testing of CdTe/CdS Solar Cells

With the success of fabricating high efficiency thin film solar cells, the CdTe research community has now shifted focus on understanding the degradation mechanisms involved to increase their longevity and make them cost effective. This section will summarize stress analysis of only CdTe solar cells under various stress conditions like temperature, illumination, bias and ambience.

Hegedus et.al. [31] have studied the stress-induced degradation of CdS/CdTe solar cells at elevated temperatures and bias, both in the dark and under illumination. Three degradation modes had been identified: 1) Formation of a blocking back contact, 2) Higher junction recombination, and 3) Increased dark resistivity. The blocking back contact was the result of forward bias stressing. Both high temperature and forward bias was required for junction degradation. Recontacting the device after stress removed the blocking behavior with no further junction degradation. Devices without Cu in the contact had poor initial performance with degradation independent of bias. Initial efficiencies of 10-12% were obtained for devices with Cu in the back contact and 7-9% for Cu-free back contacted devices which also showed blocking behavior. Uncontacted CdS/CdTe structures were stressed @ OC at 100 oC. Contacting these substrates after stress resulted in Voc~0.8V which is comparable to the initial performance of standard unstressed devices. When the CdS/CdTe/6nmCu structure was subjected to similar stress and contacted, the Voc of the device dropped to 0.65V. The intrinsic CdS/CdTe junction is stable but the presence of Cu during stress causes junction degradation. The relative change in efficiency after stress for devices with various contacting processes stressed at reverse bias (RB), short circuit (SC), maximum power point (MP) and open circuit voltage (OC) at 100 oC in dry air is shown in figure 29.
Degradation was maximum in the presence of Cu in the back contacts @ OC and minimum @ SC. There was degradation in devices with no Cu in the back contacts, however it was relatively independent of bias during stress. J-V comparison of SC stressed devices showed large cross-over of dark/light curves though the device degradation was minimum, indicating a large photoconductivity effect. This was attributed to Cu doping of CdS [16].

The effect of forward bias (FB) during stress in the dark @ 60°C for both Cu and Cu-free contacts was studied with bias stress extended to 2.5V (figure 30). Degradation was negligible upto 1V of FB stress and increased drastically at higher bias. Cu-free back contacted devices show no bias dependence to degradation. The effect of temperature, bias, and time are separated in the dark J-V comparison of a device stressed @ +2V. The device was initially stressed for 1 day @ 28°C, then stressed for 1 day @ 60°C and then finally for 10 days. Then the device was recontacted.
Figure 30. FF and $V_{oc}$ for Devices with 0 or 6nm Cu After Stress @ FB in the Dark at 60°C for 10 Days

Figure 31. Analysis of Dark J-V Curve as $dV/dJ$. The Slope is $AKT/q$ and Intercept is $R_s$ and Curvature at Large J Indicates a Blocking Contact a) has $A=1.6$, $R_s=4 \ \Omega\cdot cm^2$ b) has $A=2.2$, $R_s=9 \ \Omega\cdot cm^2$
Bias stressing at 28°C in the dark for 1 day created a blocking contact. Raising the temperature to 60°C the following day resulted in higher recombination currents, higher A, and increase in $R_s$ along with the existence of the blocking contact and remained the same for the remaining 9 days (figure 31). Recontacting after stress eliminated the contact barrier but the bulk and junction characteristics of $R_s$ and A remained unaffected.

Degradation is predominant and fast in Cu doped devices @ OC or FB compared to SC. Both junction and back contact degradation occurs rapidly (<24 hours). Glancing incident X-ray studies of CdTe surface before and after stress showed cuprous telluride, Cu$_2$Te, present initially converting to cupric telluride, CuTe, after stress. It was proposed that the Cu ions liberated by this process could be moved by field-driven diffusion along GBs or electromigration. While Cu$_2$Te is a highly conductive p – type material making good ohmic contact, CuTe is a poor conductor that can cause the blocking behavior at the back contact after degradation. Though this model explained some of the results, it also raised a few questions on the electromigration of Cu. It does not explain why the Cu free devices degrade, why the degradation is not monotonic with bias (showed least degradation @ SC) and why large photoconductivity developed for stress at SC and RB. The degradation of Cu free devices can be explained by the results of this research where Cu was found by SIMS analysis at the junction of Cu-free devices coming from starting materials and contamination at various processing steps. The back contact barrier opposes the main junction. This should result in Cu ions drifting in the opposite direction at the back compared to the main junction at a given bias. Thus electromigration of Cu along GBs may be plausible, it is possibly not the only degradation mechanism.

Thus three degradation mechanisms are identified: 1) Cu-related field driven diffusion at FB occurs within hours increasing recombination and is partially reversible with field, 2) Formation of a blocking contact in a few hours due to loss of Cu from the back contact which is
not reversible with field (Recontacting with Cu-free contact eliminated the blocking contact), 3) A slower process not Cu related causing photoconductivity in CdS or CdTe.

It was proposed that the Cu\(^{++}\) ions are liberated from Cu\(_2\)Te and moved via GBs under forward bias. The concentration gradient driven diffusion lengths for Cu in bulk CdTe and along GBs for 1 hour @ 100°C results in 0.3\(\mu\)m for bulk and 30\(\mu\)m for GBs. Clearly GB diffusion is the dominant mechanism.

Visoly-Fisher et.al. [16] studied the degradation of CdS/CdTe devices in the dark to thermal stress @ 200°C under different environments (N\(_2\) and air) and under illumination (N\(_2\)). Thermal stressing in dry N\(_2\) in the dark for > 50 hours was shown to result in minimal or no degradation. 50% of the cells stressed in dry N\(_2\) showed decrease in efficiency by 10-20% due to drop in FF and J\(_{sc}\). Rollover was not observed with longer stress times. Increase in dark R\(_s\) with significant increase in dark/light J-V crossover was observed with stress times. No changes to Laser Beam Induced Current (LBIC) image of the cell was seen compared to unstressed device. SIMS analysis showed low levels of Cu in the CdTe (10\(^{17}\) Cu atoms cm\(^{-3}\)) in a non-contacted CdS/CdTe substrate but a higher level in CdS (9 x 10\(^{19}\) Cu atoms cm\(^{-3}\)). Thus, Cu was present in the cell in significant amounts even prior to contacting, originating from impurities in starting materials. Accumulation of Cl in the CdS layer (10\(^{20}\) Cl atoms cm\(^{-3}\) compared to 10\(^{19}\) Cl atoms cm\(^{-3}\) in the CdTe layer) from the CdCl\(_2\) treatment was observed. Contacting with Cu-doped graphite paste results in further accumulation of Cu in the CdS. The Cu concentration increases to 1.5 x 10\(^{20}\) atoms cm\(^{-3}\) compared to 3 x 10\(^{18}\) atoms cm\(^{-3}\) in the CdTe. The accumulation of Cu was verified by Auger electron spectroscopy (AES) and X-ray photoelectron spectroscopy (XPS) analysis. Cu clearly exhibited high affinity towards small grained polycrystalline CdS diffusing rapidly through the CdTe layer. Study of Cu diffusion in CdTe/TCO/glass structure showed no accumulation profile but a U-shaped profile with high levels of Cu in CdTe/TCO interface. This represented a profile when a diffuser is reflected at the diffusion barrier. No significant increase
in Cu levels in the CdTe layer was observed with 15 hours of thermal stress @ 200°C in dry N₂. There was a slight increase in Cu levels to 2-3.5 x 10^{20} \text{ atoms cm}^{-3}. This can further increase with higher stress times. Similar observations are noted during stressing in air, which implies Cu diffusion through CdTe/CdS structure is thermally accelerated. No pattern of Cl accumulation (increase or decrease) with stress was observed. SIMS analysis of CdS layer after stress showed significant Cu accumulation at the CdS/TCO interface, increasing with stress time. Photoluminescence analysis of non-contacted, contacted and thermally stressed device is shown in figure 32.

![Figure 32. PL Spectra of CdS Layers from Non-Contacted, Contacted and Stressed CdTe/CdS Cells. Stressing was Performed at 200°C in Dry N₂ in the Dark for 16 Hours [16]](image)

The non-contacted substrate showed a spectrum with two bands at 680nm and 750nm. The 680nm band was assigned to a (Cl \_x - V_{Cd}) type complex. Contacting the substrate results in reduction in the 680nm band and formation of a new band at 790nm instead of 750nm band. This peak is assigned to Cu_{Cd}-related transition. Stressing reduces the 680nm band further and it was observed to drop with increasing stress time in comparison the 790nm band. The spectrum of a non-contacted substrate did not change after thermal stress irrespective of ambient conditions.
The effect of Cl was investigated in cells prepared without CdCl$_2$ treatment. This resulted in poor quality devices with efficiencies of 2-3.5%. Stressing caused degradation of $V_{oc}$ from ~800mV to ~650mV but no rollover at forward bias was observed. Dark $R_s$ increased with stress. SIMS analysis of these untreated and non-contacted substrates showed low levels of Cl ($\sim 2 \times 10^{17}$ cm$^{-3}$) throughout the cell with some accumulation in the CdS layer. The origin of Cl is possibly from the commercial TCO layer as an impurity left from the manufacturing process. Cl levels in CdTe did not vary with contacting or stress. Cu levels are similar to CdCl$_2$ treated samples. The only difference is that the peak of Cu accumulation appears to be located at the CdS/CdTe interface. Following stressing, the profiles obtained become similar to the standard cells with Cu accumulation throughout CdS region. Since these devices had not received CdCl$_2$ treatment, the extent of CdTe/CdS intermixing is expected to be less than standard devices. Therefore, after contacting Cu accumulates at the CdTe side of the interface. Stressing causes this interface to further intermix and Cu to diffuse through the CdS region. PL spectra of CdS for these cells before CdCl$_2$ treatment was very different from standard cells. Weak peaks at ~600nm and 640nm and a very weak and broad band centered at ~760nm was present in this spectrum. No change in this spectrum was observed after contacting. Stress caused a new and very intense band at 790nm to form. This was found to correlate with SIMS analysis of non-CdCl$_2$ treated cells, which showed low levels of initial Cu accumulation in the CdS after contacting. Only stressing caused the CdS layer to be doped by Cu (forming Cu$_{Cd}$ complexes). Thus Cl may be involved in Cu-doping of CdS.

Thermal stressing @ 200$^\circ$C in air after ~20 hours resulted in rollover causing reduction in the FF, $J_{sc}$, and $V_{oc}$. Increase in $R_s$ due to photodoping of CdS and hence dark/light J-V crossover is observed which increased with stress time. Degradation rates are initially faster and slow upon continued stress. SIMS analysis shows no difference in Cu distribution within the cell in the presence of air or dry N$_2$. Stressing in humid air increased the degradation accompanied by
increased rollover. Storing samples in room temperature under humid conditions for several days showed degradation of device parameters especially FF. Recontacting stressed devices without first etching the exposed CdTe surface showed no change in cell J-V and rollover. Etching of CdTe prior to recontacting however improved J-V and reduced rollover. LBIC image comparison at 0, 18 and 35 hours of air stress is shown in figure 33. Image is bright and homogeneous before stress with small dark area (low current) due to regions of poor contact or mechanical damage. An increase in dark regions along with a reduction in overall image contrast was observed with stressing, indicating low currents in localized areas and decrease in current over the whole sample. Both electronic and mechanical degradation are possible reasons for loss in current.

Figure 33. Front-wall LBIC Images of Cu/HgTe/Graphite Contacted Cells Recorded Following:
a) 0, b) 18, and c) 35 Hours Air Stressing in the Dark at 200°C [16]

LBIC changes from pre-stress samples were smaller for thermal stressing in dry N₂.

Changes to the CdTe back surface chemistry was investigated using XPS analysis. Unstressed cells, cells stressed in dark in dry N₂ and in air were compared (figure 34).
The CdTe Te peak in each spectrum was accompanied by an additional Te peak at a higher binding energy (BE) corresponding to oxidized Te. The BE refers to electron binding energy and is defined as the energy required to free an electron from the coulombic attraction of the atom. The separation in BEs is $3.7 \pm 0.1$ eV, suggesting the presence of TeO$_2$ or CdTeO$_3$ on the surface (before sputtering). The intensities of the Te(oxide)-related peak in the non-stressed and N$_2$-stressed samples are much smaller ($\sim 1/3$) than in air stressed ones. After short sputtering, the separation between the Te BEs decreased ($3.2 \pm 0.1$ eV). This suggested the presence of CdTeO$_3$ or CdTe$_2$O$_5$ in the air-stressed sample after sputtering. No Te oxides were found in the non-stressed and N$_2$-stressed samples after sputtering.

Stressing @ 200°C in N$_2$ under illumination at $V_{oc}$ caused device degradation. The degree of degradation varied from 10-20% in good cells with $>9$% initial efficiency to upto 50% for initially poor cells. The greatest drop was observed in FF. Both efficiency and FF dropped gradually during 50 hours stressing unlike the air-stressed cells in dark with rapid initial drop. Some rollover in about half of the devices was observed following illumination stress. SIMS

Figure 34. Te 3d 5/2 Region of XPS Spectra of the CdTe Surface, From Beneath the Back Contacts of Cells a) Air-Stressed in the Dark (33 h), b) N$_2$-Stressed in the Dark (33h), and c) Unstressed Cells [16]
analysis showed Cu content to be higher in light stressed cells in all areas of the device, especially CdS. This indicates enhanced Cu in-diffusion during light stressing. Degradation under illumination was found to be reversible for cells stressed for short period of time (~20 h) under ambient conditions (order of days), or by heat treatment at 200°C in dry N₂ in the dark. Degradation was permanent for longer stress periods.

Thermally stressed and degraded samples have shown recovery (up to 50% recovery of efficiency loss) upon light stressing due to increase in J_sc and V_oc. Decrease in dark R_s and reduction in dark/light J-V crossover was also observed due to decrease in photoconductivity.

The PL spectrum of CdS layer from a contacted, unstressed cell was significantly different from a non-contacted substrate. The changes in the spectrum were assigned to effects of Cu ions diffusing into the bulk of the CdS grains, forming Cl₅-CuCd complexes and CuCd centers at the expense of Cl₅-V Cd complexes. Cells with no CdCl₂ treatment have shown that Cl affects Cu diffusion and doping of CdS during contact formation. The presence of Cl in CdS may accelerate the rate of Cu doping of CdS layer, as CuCd is known to complex with Cl in CdS, which causes increased co-solubility of Cu and Cl. The amount and extent of Cu doping in the CdS increases significantly with stress with less change in its levels in CdTe layer. The PL results showed a decrease in the intensity of Cl₅-V Cd transition with increasing intensity of the transition ascribed to the CuCd complex. The observed changes in PL and SIMS are due to back contact effects and not due to changes to CdS induced by the stress conditions. The high affinity of Cu for polycrystalline CdS is due to the greater chemical stability of Cu-S bonds over Cu-Te bonds as a possible driving force. Cl is shown to enhance Cu diffusion in CdS and is involved with Cu in co-doping of CdS. Recrystallization of CdS in the presence of Cu and Cl results in photoconducting CdS. Stressing of cells with significant concentrations of Cu and Cl in CdS layers is expected to increase photoconductivity. Increasing photoconductivity of CdS and hence the dark resistivity of the material will not affect the illuminated J-V until the resistivity under
illumination remains low. Higher dark $R_s$ causes decrease in slope of dark $J$-$V$ and higher
dark/light crossover. It was proposed that this photoconductivity may be related to stability during
stress in dark due to complexes of Cl and Cu related defects in CdS possibly $\text{Cl}_{\text{S}}$-$\text{Cu}_{\text{Cd}}$. This
complex may prevent Cu from acting as a deep trap in CdS assuming Cu levels in CdS to be
lower than or of same order of magnitude as Cl (shown by contacted and dark-stressed cells in
SIMS analysis). As PL and SIMS analysis of thermally stressed devices in both $N_2$ and air show
same behavior of Cu, it is deduced that degradation seen during stressing in air is a result of back
contact/junction degradation driven by atmospheric humidity. Data shows 50% of thermally
stressed devices in dry $N_2$ have 10-20% degradation. Therefore the assumption of minimal
degradation during thermal stressing in $N_2$ is questionable.

Cell degradation is accelerated by illumination during stress @ $V_{oc}$. The process is
similar to a forward bias stressing which causes a reduction in electrostatic barrier to $Cu^+$ ion drift
at the junction and promoting accumulation in CdS. The built-in voltage of the heterojunction
slows the concentration gradient driven diffusion towards CdS in equilibrium while forward bias
and/or light lowers this barrier for diffusion. Similar Cu accumulation was also observed in stable
cells thermally stressed in the dark. However, excess Cu accumulation shown in SIMS analysis
for light stressing can form deep acceptor states which act as recombination centers and decrease
the effective donor concentration of the CdS. Enhanced Cu diffusion into the CdS can be
correlated with Cu depletion at the back contact, forming a barrier for current transport. This
explains the small rollover seen in light stressed devices. Partial or full recovery of light-stress
(short period ~ 20h) induced degradation by storage or anneal in the dark is possible due to
dissociation of the acceptor defects in CdS ($Cu_{\text{Cd}}, \text{V}_{\text{Cd}}$-$\text{Cu}_i$ type defects dissociating into $V_{\text{Cd}}$ +
$Cu_i$) and back diffusion of Cu$^+$ driven by concentration gradient and the restored junction field.
The permanent degradation of longer stress times suggest that the level of Cu concentrations
causing degradation are critical and above a threshold value back diffusion/drift does not assist in
performance recovery. Heat treatment of devices in the dark before light stressing was found to stabilize their performance. It was suggested that this is due to the completion of contact anneal which may have been too short. Sufficient Cu and Te are converted to relatively more stable Cu-rich Cu$_{2-x}$Te known to form a good ohmic contact to high efficiency CdTe. This will result in less Cu$^+$ ions available for diffusion which slows down Cu diffusion into the junction compared to Te-rich Cu telluride. Further studies and chemical analysis is necessary to verify this theory.

Oxygen migration through the back contact and formation of insulating oxide layer on the CdTe surface is postulated to be the main reason for degradation of unencapsulated cells in air. CdTeO$_3$ (stable thermal oxide of CdTe) decreases the hole current from p-CdTe in a p-CdTe-oxide-metal junction. Thus the probability of tunneling is lowered with increasing oxide thickness and the contact barrier height is increased due to trapped charges in the oxide causing rollover. This barrier can also explain increase in Rs in the dark. Thus humidity accelerates the oxidation of CdTe causing larger degradation during thermal stressing in air.

The following degradation mechanisms are postulated based on the results described above.

Figure 35. Schematic Representation of Mechanisms Explaining the Behavior of CdTe/CdS Cells Under Various Stress and Recovery Conditions (Layer Thicknesses are not to Scale) [16]
The proposed changes are:


b) Stress in dark, O₂/H₂O-containing atmosphere. Observed behavior: severe degradation, J-V rollover. Mechanism: Oxidation of CdTe/back contact interface

c) Stress in light, inert atmosphere. Observed behavior: degradation, slight J-V rollover. Mechanism: Enhanced Cu diffusion into CdS, loss of favorable Cu₂₋ₓTe at the CdTe/back contact interface

d) Recovery after light stress degradation, in ambient atmosphere at room temperature or by heat treatment in inert atmosphere. Observed behavior: J-V recovery. Mechanism: dissociation of Cu-related defects in CdS, back diffusion of Cu out of CdS, Cu₂₋ₓTe restored. The cell returns to a state similar to case (a)

Thus, presence of Cu is NOT a dominant factor in initial degradation modes of thermal stressed devices. Significant levels of Cu and Cl in CdS increase its photoconductivity. This increases the dark resistivity of CdS causing an increase in dark/light J-V crossover. This change does NOT affect the light J-V characteristics of the device. However, excessive Cu doping of CdS during light stressing is found to degrade device performance due to creation of deep acceptor states in CdS and decrease its effective donor concentration. The role of ambient atmosphere on unencapsulated devices during stress is seen in the back contact degradation due to oxidation of CdTe back surface when exposed to air.

Townsend S.W [14] had studied the effect of bias stress on CdTe solar cells. Ionic diffusion of Cu into CdS was proposed to be the root cause of bias degradation of CdS/CdTe solar cells based on the results. This along with back contact degradation was found to increase device Rₛ. The difference in dark and light Rₛ was attributed to highly resistive CdS where trap concentration is above the carrier concentration. Degradation due to bias stress was found to be
different from studies of Hegedus and Visoly-Fisher discussed previously. Most severe
degradation was found to occur under RB stress. Similar reduction though not as drastic was seen
under OC and minimal loss in efficiency was observed under FB stress. $V_{oc}$ was still found to
drop considerably with FB stress along with an increase in diode quality factor, $A$. The apparent
doping density within CdTe layer was lowered at FB and increased near the back contact. This
increased the zero bias depletion width from 1.5um to 2.7um accompanied by an increase in
current collection of long wavelengths. RB caused an increase of apparent doping density within
CdTe causing a reduction in depletion width and decrease in current collection of long
wavelengths. Back contact barrier lowered from 0.34eV (unstressed) to 0.30eV with FB stress
and increased to 0.51eV with RB stress. The doping concentration at the back contact interface
did not change significantly with FB, but decreased with RB stress. The increase in barrier height
explains the increase in $R_s$ observed with RB stress. Enhanced recombination occurs with FB
stress with diode quality factor $>2.0$ after stressing, which implies a tunneling enhanced
recombination mechanism evolving with stress under reduced electric field. Both OC and RB
stress showed an increase in $R_s$ attributed to highly resistive Cu doped CdS film. Changes to
CdTe region outside the depletion width also adds to this resistance. PL spectra showed the
presence of Cu on the grain boundaries in CdS. When CdS is treated with Cu along with CdCl$_2$
treatment it results in the spectra changing, which shows Cu present in CdS bulk with reduction
in the peak of Cu on the grain boundaries. RB stress has Cu within the bulk CdS due to high
electric field. Photoconductivity effect was observed in CdS films intentionally doped with Cu.
Thus devices with Cu within CdS layer are expected to exhibit a difference in $R_s$ from dark to
light measurements. This effect was observed in actual devices. Cells completed with
intentionally Cu doped CdS layer showed many similarities to RB stressed devices such as drop
in FF and increase in $R_s$. Thus stress-induced degradation of CdS/CdTe devices is in part due to
the changes to CdS layer during stress. The changes to back contact barrier are attributed to
CHAPTER 4
EXPERIMENTAL

4.1 Device Structure & Fabrication

A conventional CdS/CdTe solar cell structure with the n-type window layer of CdS and p-type absorber layer of CdTe is shown in the figure 36.

![Figure 36. Conventional CdTe/CdS Solar Cell (Superstrate Structure)](image)

Light enters these cells through the transparent substrate (glass) and is called the backwall or superstrate configuration. The TCO layer of SnO$_2$:F film is the frontwall contact. The doped graphite paste and silver paint forms the back contact to the cell.

The fabrication process of devices used in this study begins with the deposition of a degenerately doped layer of SnO$_2$:F on a clean 7059 glass substrate which provides films with a sheet resistivity of the about 7-10 $\Omega$/sq. The film serves as a transparent conducting oxide (TCO)
which conducts the current from the CdS/CdTe junction to the front metal contacts around the cell. This film is deposited by MOCVD technique. Halocarbon 13B-1 serves as a source of fluorine (dopant) and tetramethyltin (TMT) provides Sn. He and O₂ are ambient gases for the deposition. The final thickness of SnO₂ films are about 0.8-1 μm thick.

CdS films were deposited using chemical bath deposition (CBD). Cadmium acetate (CdAc) - the Cd ion source, thiourea - the sulfur ion source, and the buffer - ammonium acetate (NH₃Ac) and ammonium hydroxide (NH₄OH) constitute the reactants. A solution containing measured amounts of CdAc, NH₃Ac and NH₄OH is prepared along with a solution of thiourea. The deposition process involves immersing the SnO₂:F coated substrates held by a glass holder into a beaker with water and heating the solution to 90°C. The temperature is maintained constant throughout the deposition. The rate of formation of CdS can be adjusted by varying the concentration of ammonia and its salts in the solution. Homogeneous formation of CdS in the solution produces CdS precipitate whereas heterogeneous formation produces adherent CdS deposits on the substrate surface. Thus, the homogenous process which yields powdery, non-adherent films on the substrate is undesirable. This is suppressed using conditions for the formation of CdS at low rates like low temperature, high concentration of NH₃ and NH₄ salt, and low concentration of Cd salt and thiourea.

Figure 37. CSS Deposition Chamber [50]
The CdTe film is deposited over the CdS film by the CSS technique. The deposition setup for CSS process is shown in figure 37. The substrates are annealed in H$_2$ for 10 minutes at 400°C before CdTe deposition. The CdTe deposition by CSS is its sublimation from a 99.999% pure CdTe source. The deposition is done at source temperature of 600 to 680°C and substrate temperature of 500 to 600°C for 1-7 minutes in the presence of He/O$_2$ as ambient gases. Films of 4-10 micrometers thickness are obtained.

The cadmium chloride (CdCl$_2$) treatment of a heterojunction is essential to increase the grain size of CdTe films, which reduces grain boundaries, potential shunting paths and recombination centers which effect cell performance. It is also believed to improve the interface between CdS and CdTe enhancing the open circuit voltage of the device. The treatment involves the evaporation of CdCl$_2$ and annealing the substrate at 400°C in the presence of He and O$_2$ for 45 minutes. Excess CdCl$_2$ is removed by rinsing the samples in methanol and then treating with bromine solution leaving a smooth Te rich surface for contacting.

The final step in the fabrication of this cell involves contacting. Graphite paste doped with HgTe:Cu is painted on the CdTe film and the substrates are annealed at 250°C in He ambient. The graphite contact is then coated with a thin conductive layer of silver paint. This completes the back contact for the solar cell. The CdTe around the cell is removed, exposing the SnO$_2$:F surface. Indium solder is applied to this film, which serves as a front metal contact. This completes the fabrication of a CdS/CdTe solar cell.
4.2 Thermal Stress (TS)

Thermal degradation of CdS/CdTe solar cells was accelerated by stressing cells at higher temperatures than they are likely to operate under normal operating conditions. The annealing process is carried out in a vacuum chamber in an inert ambient of UHP He at temperatures of 60°, 70°, 80°, 90°, 100° & 120°C. A schematic drawing of the chamber is shown in figure 38. Inside the chamber are six zones of quartz heating lamps individually controlled by temperature controllers. Above each zone a graphite boat was placed which could hold 15-20 cells to be thermally stressed. A thermocouple was attached to the boat which enabled the temperature control of each zone to a unique temperature. The chamber has an outlet connected to a vacuum pump at the bottom. An inlet for UHP Helium on one side of the chamber was used to purge the system before starting an annealing process. Each run is started with a purge and backfill of the chamber with UHP He to remove any adsorbed moisture and air in the chamber. The chamber is
filled with UHP He to a positive pressure of 20 psi before start of thermal stressing. Due to malfunctioning of the temperature controller at 60°C, the temperature of this zone could not be controlled constantly and thus results from samples in this zone are discarded from our analysis. Stressing for gradually increased from 1, 2, 3, 4, 8, 16, 32… hours. Light/Dark J-V and C-V analysis was performed after each stress period.

4.3 Illumination Stress or Light Soaking (LS)

Figure 39. Illumination Stressing Chamber

A schematic of illumination stressing chamber is shown in figure 39. It consists of a vacuum sealed quartz tube which allows illumination of the solar cells inside and keeps out moisture, humidity and air. Samples are mounted in the chamber with outlets for electrical wires to monitor device performance and a thermocouple to monitor the temperature of the devices under stress. The solar cell simulator based on tungsten halogen quartz lamps is calibrated to ~AM1.5 conditions. Lightsoaking is performed in a N₂ ambient. Continuous flow of N₂ gas is maintained from the inlet during stressing which enables cooling the device under stress and
helps keep air and humidity out of the chamber. Stressing was performed initially for small periods of 2, 4, 6 hours and increased to 8-10 hours/day after 50 hours. Light J-V testing was performed everyday during stressing @ 70°C. Dark J-V testing was performed before the start of stressing each day. Room temperature J-V testing was performed infrequently at ~200 hour stress periods.

4.4 Characterization Techniques

During the light-soaking and thermal stressing of the CdS/CdTe solar cells, the following measurement techniques were used to characterize the device performance. Current – Voltage (I-V), Capacitance – Voltage (C-V), Capacitance – Frequency (C-F) and Spectral Response (SR) measurements taken intermittently are used to study the device behavior.

4.4.1 J-V Measurements

Dark and light J-V measurements were performed on the devices, both initially and during the various stages of annealing and light soaking. Many important device parameters can be deduced from this data. From a typical light J-V curve, apart from measuring the values of diode parameters $V_{oc}$, FF, $J_{sc}$ and $\eta$ it is possible to extrapolate shunt and series resistance values. Shunt resistance is calculated by taking the slope of J-V in the reverse bias condition while series resistance can be obtained from the slope at high forward bias region. The shunt resistance @ $J_{sc}$ is measured by taking the slope of the J-V curve between voltages of ±100mV and the series resistance is measured from the slope of the J-V curve between currents of 90-100mA. Diode leakage current, $J_0$, can be deduced from the extrapolation of the slope of dark ln(J) vs V curve between 0.2V and 0.6V to zero bias.

The diode quality factor, $A$, is deduced from the dark J-V curve using the simplified diode equation,
\[ A = \Delta V/(kT/q* \ln(\text{ABS}(J_{01}/J_{02}))) \]

Plotting A vs Voltage between 0.3V and 0.6V, the minima of the curve is calculated. Shunt and series resistance affect the value of diode quality factor below 0.3V and above 0.6V. A is typically between 1.5±0.2 for CdTe devices.

The dependence of A on voltage and light intensity was discussed in the theory section. This results in questioning the accuracy of measuring A. This is especially true of the degraded devices measured in this study with severe shunting or high leakage currents or presence of a collection function. The value of \( J_0 \) and A are in doubt simply due to the fact that recalculation of \( J_0 \) from the \( V_{oc} \) of the cell results in different values than the extrapolated \( J_0 \).

### 4.4.2 C-V Measurements

Capacitance measurements are performed in the dark at a high frequency of 300kHz. The doping concentration, \( N_A \) and \( V_{bi} \) of the device can be obtained from the C-V measurements for uniformly doped materials. Slope of \((A/V)^2\) curve at reverse bias provides \( N_A \) and the intercept on the x-axis provides the \( V_{bi} \).

### 4.4.3 Spectral Response Curves

Spectral response (SR) is used to measure the \( J_{sc} \) of the device. The current generated from an incident light source of 400nm to 900nm is collected to calculate the \( J_{sc} \) of the device.

### 4.5 Device Behavior of USF Cells

This section discusses the CdS/CdTe cells fabricated at USF and summarize their behavior studied in the past.
4.5.1 I-V Analysis

4.5.1.1 Temperature I-V Analysis

The reverse saturation current variation with temperature was measured by Chris Ferekides [43] as shown in figure 40. \( J_0 \) values were obtained from y-intercept of dark J-V curves. The exponential dependence of \( J_0 \) on \( 1/T \) indicates that the cells are not dominated by tunneling currents. The standard recombination model predicts a slope of \( E_g/2 \) (0.72 eV) for this graph. The measured slope of 0.66 eV is close indicating that recombination current dominates device behavior above 220K.

Figure 40. Temperature Dependence of \( J_0 \) [43]

4.5.1.2 Light & Dark J-V Analysis

The typical light J-V curves of USF cells do not have any “roll over” at forward bias, indicating a quasi-ohmic back contact to CdTe. An example of a device with a non-ohmic back contact with “rectification” or “roll-over” is shown in figure 41. The device has an ohmic back contact initially, which degrades under thermal stress showing a rollover effect.
Figure 41. “Rollover” Observed in J-V Curves

The “crossover” behavior of dark and light J-V of USF cells is illustrated in figure 42.

Figure 42. “Crossover” of Dark & Light J-V in USF Cells [7]
electromigration of Cu$_{\text{cd}}^-$ over Cu$_{\text{i}}^+$. FB stress assists the electromigration of negatively charged species towards the back contact and RB depletes it from the back contact causing formation of back barrier.

Morgan D.T [13] also studied the degradation of CdS/CdTe solar cells under bias stress conditions in the dark and light. The highest degree of degradation of all parameters was observed for RB in the dark. Doping levels and magnitude change significantly with bias stress and this change was proposed to be the major determining factor of degradation. The bias dependence of degradation clearly shows a considerable role of electromigration of charged impurities and defects (Cu-related) in device degradation.

Gilmore A.S [30] observed that samples stressed under OC (which improved efficiencies) exhibited an increase in the defect state density of the shallow defect state (associated with Cu$_{\text{cd}}^-$). Samples stressed under RB (-2V, which decreased efficiency) showed a marked decrease in the density of defects associated with the same level. Neither stress condition changed the defect density of deep level associated with cadmium vacancies. These observations also point towards the migration of copper and its defects under stress. Its depletion at the back contact is proposed to cause the degradation in device performance.

It is clear from the above studies that Cu and its defect complexes have been identified as the primary factor responsible for degradation. However, the nature of the mobile species and the mechanism of its transport (electromigration or field assisted diffusion) and the degraded layer (CdTe or CdS) is widely debated and still speculative based on the results of individual research groups.
Extensive study of this behavior was done by Dan Oman [7]. The bias and spectral
dependence of the dark J-V has shown the existence of a “front junction” at the CdS/SnO₂
interface opposing the main junction. The front junction however has very low Rₚ in light
making its effect negligible under illumination.

The J-V of a good device with efficiency > 10% can be simulated from the equation
given below.

\[ I = I_o \left[ e^{\frac{q(V-I_R_s)}{A_kT}} - 1 \right] - I_L - \frac{(V-I_R_s)}{R_{sh}} \]

4.5.2 Spectral Response Analysis

It was observed that USF cells showed no voltage dependent collection for unstressed
devices [7]. This suggests that expanding the SCR into the bulk CdTe does not collect any
additional carriers. This observation agrees with the capacitance measurements, which have
shown that SCR extends more than 1µm into the bulk.
CHAPTER 5
RESULTS AND DISCUSSION

5.1 Thermal Stress

This section discusses the effects of thermal stress on device performance. The degradation process was accelerated by stressing cells at higher temperatures than they are likely to reach under normal operating conditions. A few witness samples were put aside in a desiccator at room temperature. Devices from the same substrates were subsequently used for thermal stress. The stressing process was carried out in a vacuum chamber in an inert ambient of UHP He at temperatures of 70°, 80°, 90°, 100° & 120°C. It was observed that temperatures above 100°C degraded the silver epoxy contact, resulting in stressing and peeling of underlying films from the substrate. Due to the peeling of backcontacts at high temperatures, the current cell design cannot be used for accelerated stress testing above 100°C, in order to study the intrinsic junction and back contact degradation mechanisms.

The cells have been characterized using J-V, SR and C-V measurements. The first set of data summarizes the performance changes in the device short circuit current ($J_{sc}$), open-circuit voltage ($V_{oc}$), fill factor (FF), cell efficiency ($\eta$), diode quality factor (A) and reverse saturation current density ($J_o$) after stressing for 3600 hours at various temperatures. Each datapoint for stressed devices in figures 43, 44 & 45 indicates the normalized parametric change and is an average of change observed in three samples. The datapoint for witness samples is an average of change in two samples.
5.1.1 Effect on Open-Circuit Voltage (V\text{oc})

A general trend of decreasing V\text{oc} with increasing stress temperature was found. Figure 43 shows a normalized change in V\text{oc} with time for devices with various stress temperatures.

Witness samples do not degrade over time for V\text{oc}. In stressed devices, the most significant drop in V\text{oc} occurred within 500 hours of stressing irrespective of the stress temperature. Subsequently the V\text{oc} “leveled off” over time. Total drop in V\text{oc} was less than 4% up to 100°C stress temperature, but jumped to 11% at 120°C.

![Normalized Voc vs Time](image)

Figure 43. Normalized V\text{oc} vs Time at Various Stress Temperatures

The change in V\text{oc} at 500 hour intervals is tabulated in table 2. Typically there was a decrease in V\text{oc}, though there are instances of increase. It is not exactly clear if this recovery is real on all occasions as this is within the range (10-15mV) of measurement error. However, such
recovery in device parameters had been observed by others [23] in polycrystalline devices due to relaxation of defects at the junction.

Table 2. Change in $V_{oc}$ at 500 Hour Intervals

<table>
<thead>
<tr>
<th>Stress Period, Hrs</th>
<th>0-500</th>
<th>500-1000</th>
<th>1000-1500</th>
<th>1500-2000</th>
<th>2000-2500</th>
<th>2500-3000</th>
<th>3000-3600</th>
<th>Average</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature, C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-3.2</td>
<td>-3.2</td>
</tr>
<tr>
<td>70</td>
<td>-11.4</td>
<td>6.2</td>
<td>-3.2</td>
<td>-5.5</td>
<td>-6.2</td>
<td>-2.3</td>
<td>4.0</td>
<td>-2.6</td>
<td>-18.4</td>
</tr>
<tr>
<td>80</td>
<td>-11.7</td>
<td>5.4</td>
<td>-5.6</td>
<td>-14.6</td>
<td>-2.2</td>
<td>1.7</td>
<td>2.1</td>
<td>-3.6</td>
<td>-24.9</td>
</tr>
<tr>
<td>90</td>
<td>-25.3</td>
<td>3.8</td>
<td>5.0</td>
<td>-13.0</td>
<td>2.4</td>
<td>-3.4</td>
<td>-1.2</td>
<td>-4.5</td>
<td>-31.6</td>
</tr>
<tr>
<td>100</td>
<td>-35.3</td>
<td>7.8</td>
<td>2.7</td>
<td>-13.8</td>
<td>3.1</td>
<td>-10.2</td>
<td>9.4</td>
<td>-5.2</td>
<td>-36.4</td>
</tr>
<tr>
<td>120</td>
<td>-70.2</td>
<td>11.4</td>
<td>-12.8</td>
<td>-10.5</td>
<td>-9.1</td>
<td>-4.3</td>
<td>5.4</td>
<td>-12.9</td>
<td>-90.0</td>
</tr>
</tbody>
</table>

Note: "-" shows DECREASE, "+" shows INCREASE

The drop in $V_{oc}$ increases with high stress temperatures and is a result of increasing recombination losses and reverse saturation current, $J_o$ along with junction “shunting” as will be shown later during the J-V analysis.

5.1.2 Effect on Fill Factor (FF)

![Normalized FF vs Time](Figure 44. Normalized FF vs Time at Various Stress Temperatures)
The fill factor showed significant degradation due to thermal stressing. The figure 44 shows changes observed over time. Most of the decrease is early, similar to \( V_{oc} \), but takes 1000 hours instead of 500 hours. A linear degradation can be seen over time for each temperature. A drop of 7\% @ 70\(^\circ\)C to 36\% @ 120\(^\circ\)C can be seen within the first 1000 hours. From 1000-3600 hours the rate of degradation decreases to 3\% @ 70\(^\circ\)C to 7\% @ 120\(^\circ\)C.

A tabulation of the absolute FF variation over 500 hour intervals is shown in table 3. The variation ranges from 1.5\% for an unstressed device to 31\% for a device stressed at 120\(^\circ\)C.

### Table 3. Change in FF at 500 Hour Intervals

<table>
<thead>
<tr>
<th>Stress Period, Hrs</th>
<th>0-500</th>
<th>500-1000</th>
<th>1000-1500</th>
<th>1500-2000</th>
<th>2000-2500</th>
<th>2500-3000</th>
<th>3000-3600</th>
<th>Average</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature, C</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-1.5</td>
<td>-7.5</td>
</tr>
<tr>
<td>70</td>
<td>-2.9</td>
<td>-2.3</td>
<td>-2.7</td>
<td>1.8</td>
<td>-0.3</td>
<td>-0.8</td>
<td>-0.3</td>
<td>-1.1</td>
<td>-7.5</td>
</tr>
<tr>
<td>80</td>
<td>-8.7</td>
<td>-3.9</td>
<td>-6.8</td>
<td>1.5</td>
<td>-2.1</td>
<td>-0.4</td>
<td>0.6</td>
<td>-2.9</td>
<td>-20.0</td>
</tr>
<tr>
<td>90</td>
<td>-9.4</td>
<td>-4.0</td>
<td>-2.9</td>
<td>1.3</td>
<td>-3.4</td>
<td>-0.1</td>
<td>0.6</td>
<td>-2.6</td>
<td>-18.0</td>
</tr>
<tr>
<td>100</td>
<td>-16.7</td>
<td>-4.8</td>
<td>-4.3</td>
<td>1.3</td>
<td>-3.9</td>
<td>-0.6</td>
<td>0.9</td>
<td>-4.0</td>
<td>-28.2</td>
</tr>
<tr>
<td>120</td>
<td>-24.6</td>
<td>-1.3</td>
<td>-2.9</td>
<td>0.4</td>
<td>-2.7</td>
<td>0.4</td>
<td>-0.7</td>
<td>-4.5</td>
<td>-31.4</td>
</tr>
</tbody>
</table>

Note: "-" shows DECREASE, "+" shows INCREASE

The FF degradation is a result of several factors: increasing \( R_s \), decreasing \( R_{sh} \), and increase in collection losses, which will be discussed in the later subsections discussing the effect of thermal stress on \( R_s \), \( R_{sh} \), and \( J_{sc} \).

### 5.1.3 Effect on Short-Circuit Current Density (\( J_{sc} \))

No significant change in \( J_{sc} \) was observed for the witness samples. Degradation is most prominent within the first 1000 hours for stressed devices. A linear and slow degradation is observed thereafter at all stress temperatures. \( J_{sc} \) losses range from 2\% at 70\(^\circ\)C to 23\% at 120\(^\circ\)C (figure 45).
Figure 45. Normalized $J_{sc}$ vs Time at Various Stress Temperatures

Figure 46. SR of a Witness Sample Stored at Room Temperature in a Desiccator
The $J_{sc}$ of a witness sample from SR measurements is shown in figure 46. A small improvement of 0.6mA/cm$^2$ in $J_{sc}$ was observed. The increase comes mostly from the improved collection of deeply generated carriers due to possible changes to the nature of the defects that lead to stronger electric fields (higher depletion). The doping profile generated from C-V analysis showed increase in depletion region of CdTe. The performance improvement has been observed in the past in CdTe devices fabricated at USF [23].

![CdTe#9-29A-11A(70°C)](image)

Figure 47. SR of Device Stressed @ 70°C Before and After 3600 Hours Stressing

A minimal change in spectral response was observed in devices stressed up to 80°C. A representative sample SR of a device stressed at 70°C is shown in figure 47 where the initial and final SR responses are essentially identical.

Above 80°C degradation in $J_{sc}$ was observed, which accelerated significantly at higher stress temperatures. The SR of a device stressed at 120°C is shown in figure 48. Predominant collection losses occurred in the red region suggesting changes deep in bulk CdTe, away from the depletion region. This means that the lifetime of photo-generated carriers deep in the CdTe is significantly reduced. The carriers are lost to recombination before reaching the space charge region (SCR) and being swept by the electric field.
5.1.4 Effect on Shunt Resistance ($R_{sh}$)

The shunt resistance of devices drastically decreases with increasing stress temperature.

Table 4 shows the variation in $R_{sh}$ @ $J_{sc}$ over time for a representative sample from each stress temperature and table 5 shows the variation in FF over time for the same samples. The effect of $R_{sh}$ on FF becomes significant below values of 1.5k $\Omega$-$cm^2$. Below this value the FF decreases drastically by >20%.

Table 4. $R_{sh}$ @ $J_{sc}$ Variation over Time

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Sample#</th>
<th># of Hours in thermal stress</th>
<th>0</th>
<th>580</th>
<th>1260</th>
<th>3000</th>
<th>3600</th>
<th>% Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>25°C</td>
<td>9-29A-10A</td>
<td>4188</td>
<td>0</td>
<td>580</td>
<td>1260</td>
<td>3000</td>
<td>3600</td>
<td>-22%</td>
</tr>
<tr>
<td>70°C</td>
<td>9-29A-11A</td>
<td>3343</td>
<td>3319</td>
<td>3274</td>
<td>2034</td>
<td></td>
<td></td>
<td>-39%</td>
</tr>
<tr>
<td>80°C</td>
<td>9-29A-8D</td>
<td>3371</td>
<td>2678</td>
<td>946</td>
<td>1390</td>
<td>1063</td>
<td></td>
<td>-68%</td>
</tr>
<tr>
<td>90°C</td>
<td>9-29A-11B</td>
<td>4230</td>
<td>1221</td>
<td>1086</td>
<td>750</td>
<td></td>
<td></td>
<td>-82%</td>
</tr>
<tr>
<td>100°C</td>
<td>9-29A-10C</td>
<td>7116</td>
<td>790</td>
<td>379</td>
<td>304</td>
<td>262</td>
<td></td>
<td>-96%</td>
</tr>
<tr>
<td>120°C</td>
<td>9-29A-11C</td>
<td>3634</td>
<td>161</td>
<td>163</td>
<td>144</td>
<td>146</td>
<td></td>
<td>-96%</td>
</tr>
</tbody>
</table>

Note: "-" change indicates DECREASE, "+" change indicates INCREASE
Table 5. FF Variation over Time

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Sample#</th>
<th>FF, %</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of Hours in thermal stress</td>
<td>0/580</td>
</tr>
<tr>
<td>25°C</td>
<td>9-29A-10A</td>
<td>0.71</td>
</tr>
<tr>
<td>70°C</td>
<td>9-29A-11A</td>
<td>0.73</td>
</tr>
<tr>
<td>80°C</td>
<td>9-29A-8D</td>
<td>0.72</td>
</tr>
<tr>
<td>90°C</td>
<td>9-29A-11B</td>
<td>0.74</td>
</tr>
<tr>
<td>100°C</td>
<td>9-29A-10C</td>
<td>0.74</td>
</tr>
<tr>
<td>120°C</td>
<td>9-29A-11C</td>
<td>0.74</td>
</tr>
</tbody>
</table>

Note: "-" change indicates DECREASE, "+" change indicates INCREASE

The FF vs R_sh are plotted in the figure 49 from measurements taken for the above devices at various times during stress. A drastic decrease in FF for R_sh < 1.5k Ω-cm^2 was observed.

![FF vs Rsh @ Jsc](image)

Figure 49. FF vs R_sh @ J_sc of Devices Stressed to 3600 Hours and Simulations

In the same figure, the FF vs R_sh @ J_sc profile simulated from the J-V equation of a diode with varying R_s is plotted. The FF closely matches simulations at high R_sh (typical USF device R_s ~ 2Ω) which represent data points before the devices were stressed. The lower R_sh @ J_sc <2kΩ are measured after stressing devices at various temperatures. The FF does not match simulations at low R_sh below 2kΩ. Along with the reduction in R_sh, the R_s of degraded devices had increased up
to $6\Omega$. The simulated FF for low $R_{sh}$ and $R_s$ of $6\Omega$ is higher than measured FF. Thus, it can be concluded that there are other factors causing the reduction in FF.

Collection losses are found to be the third factor responsible for reducing FF. When photogenerated carriers are lost to recombination centers that lead to lower $J_{sc}$, they cause a drastic reduction in FF. Forward bias decreases the collection field increasing the losses. This effect can be verified by measuring the reverse bias $R_{sh}$ of the device at $-2V$. Reverse bias makes the depletion width wider. Due to the N'-P structure of CdS/CdTe solar cell, the depletion width modulation occurs predominantly in the CdTe. This helps collect more photogenerated carriers in the bulk CdTe that are lost to recombination at zero or forward bias. Thus studying the variation in $R_{sh}$ @ $-2V$ and @ $J_{sc}$ will clearly show if any collection effects are dominant in the degraded devices. The J-V curves of devices thermally stressed for 3600 hours is shown in figure 50.

![J-V Curves after Thermal Stress](image)

Figure 50. J-V Curves of TS Devices to 3600 Hours at Various Temperatures
The reduction in $R_{sh} @ J_{sc}$ due to increasing collection losses at higher thermal stress are tabulated in table 6 along with the FF degradation.

Table 6. $R_{sh} @ J_{sc}$ and $R_{sh} @ -2V$ after Thermal Stress at Various Temperatures

<table>
<thead>
<tr>
<th>Sample#</th>
<th>$R_{sh} @ J_{sc}$ (ohm-cm$^2$)</th>
<th>$R_{sh} @ -2V$ (ohm-cm$^2$)</th>
<th>$R_{sh} @ J_{sc} / R_{sh} @ -2V$ FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>9-29A-11A(70°C)</td>
<td>3333</td>
<td>5435</td>
<td>0.61</td>
</tr>
<tr>
<td>9-29A-8D(80°C)</td>
<td>781</td>
<td>3774</td>
<td>0.21</td>
</tr>
<tr>
<td>9-29A-11B(90°C)</td>
<td>901</td>
<td>2597</td>
<td>0.35</td>
</tr>
<tr>
<td>11-17A-2C(100°C)</td>
<td>526</td>
<td>1266</td>
<td>0.42</td>
</tr>
<tr>
<td>9-29A-11C(120°C)</td>
<td>143</td>
<td>134</td>
<td>1.07</td>
</tr>
</tbody>
</table>

It is clearly evident that up to 100°C the $R_{sh} @ -2V$ is higher than 1kΩ which means the devices are not “shunting”. The low $R_{sh} @ J_{sc}$ is the effect of collection losses deep in the CdTe layer. The device degradation at 120°C is caused by severe “shunting”, resulting in high leakage currents. Thus shunting effects outweigh collection losses at high stress temperatures.

### 5.1.5 Effect on Series Resistance ($R_s$)

Another parameter that has a direct influence on the FF of a device is its series resistance. Bulk $R_s$ can be deduced from the slope of the light J-V at high forward currents. The $R_s @ V_{oc}$ is a good indicator of the presence of back contact barrier in the device which may not be captured by measuring $R_s$ at high forward currents.

Table 7 indicates the changes in $R_s$ at high forward current for a representative sample at each stressing temperature. A clear increase in $R_s$ was measured over time with higher stress temperatures. Witness sample shows minimal change.
Table 7. Rs @ High Current for Thermal Stress at Various Temperatures

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Sample#</th>
<th>Series Resistance @ High Current, Ohm-cm²</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of Hours in thermal stress</td>
<td>0</td>
<td>580</td>
</tr>
<tr>
<td>25°C</td>
<td>9-29A-10A</td>
<td>2.7</td>
<td></td>
</tr>
<tr>
<td>70°C</td>
<td>9-29A-11A</td>
<td>2.1</td>
<td>2.0</td>
</tr>
<tr>
<td>80°C</td>
<td>9-29A-8D</td>
<td>1.6</td>
<td>2.1</td>
</tr>
<tr>
<td>90°C</td>
<td>9-29A-11B</td>
<td>2.0</td>
<td>2.6</td>
</tr>
<tr>
<td>100°C</td>
<td>9-29A-10C</td>
<td>1.9</td>
<td>3.5</td>
</tr>
<tr>
<td>120°C</td>
<td>9-29A-11C</td>
<td>1.8</td>
<td>2.1</td>
</tr>
</tbody>
</table>

Note: "-" shows DECREASE, "+" shows INCREASE

The Rs increases up to 6Ω with increasing stress temperatures after 3600 hours. Simulation of Rs vs FF in Figure 49 and Rsh @ -2V in Table 6 show that the change in Rs does not completely explain the loss in FF due to thermal stress. The FF is lower than the simulated values for Rs of 6Ω and Rsh of 1kΩ, which means collection losses as explained in section 5.1.4 contribute to device degradation along with Rs and Rsh effects.

**5.1.6 Diode Quality Factor, A & Reverse Saturation Current Density, Jo**

A & Jo do not show significant degradation up to thermal stressing of 70°C. However, high leakage currents cause A & Jo to increase at 80°C and above. Higher recombination losses at low bias voltages result in deducing accurate A & Jo values extremely difficult as seen in table 8 where unrealistic A values above 2 are calculated from the data. A discussion of these results can be found in the next section 5.1.7.
Table 8. A & $J_o$ for Thermal Stress at Various Temperatures

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Sample#</th>
<th>A</th>
<th>Change in</th>
<th>$J_o$, A/cm²</th>
<th>Change in $J_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td># of Hours in thermal stress</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0°C</td>
<td>3600</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3600</td>
</tr>
<tr>
<td>25°C</td>
<td>9-29A-10A</td>
<td>9.29A-10A</td>
<td>1.6</td>
<td>1.7</td>
<td>0.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.6E-10</td>
<td>3.2E-11</td>
<td>4.0E-10</td>
<td>2.6E-11</td>
</tr>
<tr>
<td>70°C</td>
<td>9-29A-11A</td>
<td>9-29A-11A</td>
<td>1.6</td>
<td>1.8</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.2E-11</td>
<td>3.2E-11</td>
<td>4.0E-10</td>
<td>12.5</td>
</tr>
<tr>
<td>80°C</td>
<td>9-29A-8D</td>
<td>2.2</td>
<td>2.7</td>
<td>0.5</td>
<td>3.0E-06</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.2E-06</td>
<td>3.2E-06</td>
<td>4.4E-09</td>
<td>x 1466</td>
</tr>
<tr>
<td>90°C</td>
<td>9-29A-11B</td>
<td>9-29A-11B</td>
<td>1.6</td>
<td>2.3</td>
<td>0.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.6E-11</td>
<td>2.6E-11</td>
<td>9.0E-10</td>
<td>x 34</td>
</tr>
<tr>
<td>100°C</td>
<td>9-29A-10C</td>
<td>9-29A-10C</td>
<td>1.5</td>
<td>3.1</td>
<td>1.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.5E-11</td>
<td>1.5E-11</td>
<td>3.9E-08</td>
<td>x 2600</td>
</tr>
<tr>
<td>120°C</td>
<td>9-29A-11C</td>
<td>9-29A-11C</td>
<td>1.7</td>
<td>15.0</td>
<td>13.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.4E-10</td>
<td>1.4E-10</td>
<td>6.0E-04</td>
<td>x 4.3E6</td>
</tr>
</tbody>
</table>

Note: "-" shows DECREASE, "+" shows INCREASE

5.1.7 Dark J-V Analysis

Dark J-V curves for a witness sample is shown in figure 51.

Figure 51. Ln(J)-V and Linear J-V in the Dark for a Witness Device Stored @ Room Temperature

There were no significant changes in the dark J-V behavior as shown in the Ln J-V & linear J-V data.

The J-V characteristics of a device stressed @ $V_{oc}$ in the dark at 70°C is shown in figure 52. The Ln J-V curve in figure 52 shows possible increased shunting with time. However, $R_{sh}$ @ -
2V for this device measured at >3k ohms after 3600 hours of stressing (Table 6). This suggests that the increase in current is not “shunting”. Thus, the increase in recombination current is most likely associated with the creation of deep-level defects that cause a drop in $V_{oc}$ over time. Several acceptor like defects related to Cu, Cl and their complexes were detected by DLTS studies of CdS/CdTe solar cells at USF [23]. An increase in concentration of these defects is postulated to be the root cause for increase in $J_0$ and decrease in $V_{oc}$. The nature of these defects will be discussed later in the literature. Another key change to note is that the major increase in $J_0$ occurs within the first 500 hours of stressing which subsequently saturates. This agrees with the observation of a rapid drop in $V_{oc}$ initially and its “leveling” after ~1000 hours of thermal stress.

The linear J-V curve also captures an interesting trend where the “knee” or “turn-on” of J-V shifts towards higher voltages over time. The presence of a barrier at CdS/SnO$_2$ interface against the main junction and the change in photocurrent of CdS is believed to be associated with this J-V behavior [7, 16]. This results in a dark J-V turning “ON” after the breakdown of this blocking diode at voltages higher than $V_{oc}$ causing a crossover of dark and light J-V. Thus, the shift suggests an increase in the blocking barrier. This can occur if there is a drop in concentration of CdS w.r.t SnO$_2$. If the high level of acceptor like defects (Cu and Cl complexes) accumulate in CdS, it will reduce the net doping of CdS by compensation.

The shift of the knee is gradual over time, however the corresponding FF levels off after 1000 hours. This means the front contact barrier changes may not be influencing the device under illumination. Two simultaneous effects can be deduced from the dark J-V curves.

a) A “fast” process (that occurs within the first 500 hours of stress) leads to increased recombination currents, and

b) A “slow” process (that appears to be on-going throughout the entire stress period of 3600 hours) that results in increased compensation of CdS, leading to a larger barrier between CdS and SnO$_2$. 

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Based on the discussion above, we can conclude that higher recombination currents are the root cause of degradation. The photoconductive nature of CdS has been well documented and crossover of varying degrees has been observed in high efficiency CdS/CdTe solar cells [7,16]. Since changes to the front contact barrier have not significantly altered the light J-V characteristics of the device they may not be playing a role in degradation. However, continual compensation of CdS increases its resistivity causing an increase in the device R_s and reducing the FF.

![Figure 52. Ln(J)-V and Linear J-V in the Dark for TS Device at 70°C](image)

Consider the J-V behavior of a device stressed at 120°C in figure 53. An increase in leakage losses and a consequential reduction in V_oc was observed, as can be expected for higher thermal stressing. Severe “shunting” was also observed within the first 500 hours of stressing at 120°C and was verified by measuring R_sh @ -2V. We observe a worsening of the front contact barrier with the dark J-V gradually deteriorating from a “shift” to a “collapse” over time. Junction “shunting” is believed to be the primary cause of device degradation due to a large drop in V_oc & FF observed within the first 500 hours of thermal stressing at high temperatures. Secondary effect of continual compensation of CdS exist, causing deterioration of CdS/SnO_2 barrier, but most
importantly increasing the $R_s$ of CdS layer, causing FF deterioration over time. The increase in $R_s$ @ $V_{oc}$ shown later in the light J-V indicates a possible back contact degradation.

Figure 53. Ln(J)-V and Linear J-V in the Dark for TS Device at 120°C

5.1.8 Light J-V Analysis

The witness device showed no significant change in performance over time as seen from figure 54.

Figure 54. Light J-V for a Witness Device Stored at Room Temperature
By comparing the light J-V characteristics of samples stressed at 70°C & 120°C (figure 55), a decrease in V<sub>oc</sub> and FF with increasing stress temperature is evident. A gradual increase in light R<sub>s</sub> under illumination was observed. This change mirrors the increase in dark J-V crossover. These two effects are related and are attributed to CdS compensation by deep level defects that form or mutate during the stress process. This forms the slow component of FF degradation. The faster component of degradation is most likely due to changes in CdTe and CdS/CdTe junction. Up to 90°C, collection and recombination losses are dominant as seen in the light J-V. Over 100°C, junction shunting also contributes to the performance degradation along with possible back contact degradation within 500 hours of thermal stress.

### 5.1.9 Capacitance-Voltage Measurements (C-V)

With a typical CdTe acceptor concentration of ~10<sup>14</sup>/cm<sup>3</sup> and CdS donor concentration of ~ 10<sup>16</sup>/cm<sup>3</sup>, the depletion width will extend predominantly into CdTe and thus, biasing will
result in modulating the depletion width into CdTe. Thus changes in capacitance will be primarily an effect of changes in bulk CdTe.

Figure 56 shows the net acceptor concentration ($N_A$) calculated for the control sample using C-V measurements at 300kHz. The data suggests that the net acceptor concentration at the junction had dropped from $\sim 7 \times 10^{13}$ to $3 \times 10^{13}$ due to an increase in SCR width, but the bulk concentration had increased from $1.5 \times 10^{14}$ to $2 \times 10^{14}$. This is a result of the aging effect previously discussed, where defect rearrangement and diffusion of ionic dopant species like Cu, Cl or their defect complexes occur even at room temperature over time, resulting in passivation of existing defects or compensation. This reduction in $N_A$ at zero bias with time will result in an increase in the depletion width into CdTe. This should cause an increase in current collection especially in the red region in CdTe. The SR in Figure 46 clearly shows this improvement in collection for this witness device. Note that the grading in the doping profile had increased as a result of the changes in the defect structure of the CdTe. This is due to the diffusion of dopant species such as Cu from the back contact into the CdTe, junction and the CdS as observed in SIMS analysis.

![Figure 56. $N_A$-V in the Dark for a Witness Device](image)

Figure 56. $N_A$-V in the Dark for a Witness Device
The effect of stress temperature on the C-V behavior is shown in figure 57. Changes in both bulk CdTe, SCR and CdS were observed for 70°C stressing. There is a gradual reduction in $N_A$ at reverse bias (~1.4E14 to 4.9E13) over time. The shift in linear dark J-V to the “right” with thermal stress suggests photodoping of CdS by Cu related defects. The gradual increase in $R_s$ for light J-V suggests increase in bulk resistivity possibly from both CdTe and CdS compensation. The SCR width changes from ~3.3µm to 0.9µm ($N_A$ changes from ~8E13 to 5E13) at zero bias, suggesting an increase in recombination current as seen in the ln dark J-V data. No significant collection losses were observed in the SR discussed earlier in figure 47.

![Figure 57. $N_A$-V in the Dark for a TS Device at 70°C](image)

Changes are more drastic when stress temperatures are higher than 90°C. As can be noted from the profile below for a device stressed at 100°C, bulk doping is close to initial values (changes from ~1.3E14 to 1.7E14) however $N_A$ drastically increases at the junction (changes from ~5.8E13 to 1.5E14). At high stress temperatures, clearly a high level of deep level defects exist at the junction and bulk. These defects contribute to the higher capacitance at both zero bias and reverse bias. This should result in significant reduction in depletion width (from ~4µm to
causing an increase in collection losses. The spectral response in Figure 48 depicts a large drop in “red region” current due to these changes in the high temperature stressed devices. The increase in capacitance values with stress temperatures can also be caused by increasing front contact barrier capacitance. Thus, the C-V data can only be used to make qualitative conclusions but may not be accurate quantitatively, as the C-V model predicts changes only to the main diode.

![Figure 58. N_A-V in the Dark for a TS Device at 100°C](image)

The collection losses are most likely due to activation or creation of Cu and Cl related acceptor like defects [23]. Large quantity of Cu was found to accumulate at the junction during device formation as shown later by SIMS analysis. It had been shown to exist as an ionized interstitial (shallow donor) diffusing via GBs into the bulk CdTe, junction and CdS bulk during the contact anneal. During the thermal stressing process, Cu can diffuse into the grains from their GBs readily substituting \( V_{Cd} \) due to its similar atomic size to Cd. \( Cu_{Cd} \) acts as an acceptor like defect. This will cause an increase in doping concentration of the CdTe layer and compensate the CdS layer. This clearly explains the increase in CdTe doping concentration especially close to the
junction where the highest concentration of Cu exists. The continual compensation of CdS explains the increase in dark J-V cross-over with time and the increase in bulk series resistance.

It is postulated that the continual device degradation during thermal stressing is due to creation and activation of acceptor-like substitutional defects of Cu and its complexes.

5.2 Illumination Stress

Illumination studies were performed in a vacuum sealed quartz tube. The setup involved cooling of illuminated devices with jets of N₂ gas to maintain the cells at a desired temperature. All the devices loaded for testing were generated from the same substrate and had high starting conversion efficiencies of 10.6-12.5%. An unstressed witness device (9-29A-7E) from the same substrate was stored in a desiccator. Four cells (9-29A-7D, 9-29A-7B, 9-29A-7F, 9-29A-7C) were stressed @ Vₜₙ conditions under 1 Sun intensity for ~10 hours each day. After 850 hours, resistive loads were applied on two devices and maintained @ Vₘ (9-29A-7F, 9-29A-7C). After another 400 hours & 650 hours, the devices were brought back to stressing @ Vₜₙ (9-29A-7C & 9-29A-7F). The dark J-V and C-V measurements were taken at room temperature. The light J-V measurements were carried out intermittently at room temperature under a solar simulator after the devices were allowed to cool down by the ambient N₂ gas. Most cases were measured at operating temperature of 70°C during light soaking. The temperature of the devices was monitored using “stick-on” thermocouples glued to their back surface. The changes to key parameters are described below.

5.2.1 Effect on Open-Circuit Voltage (Vₜₙ)

There was a clear reduction in Vₜₙ observed due to light soaking in all four devices. Normalized Vₜₙ reduction is shown in figure 59 for room temperature measurements. No significant reduction in Vₜₙ was observed in the unstressed sample.
All four stressed samples had shown a $V_{oc}$ reduction of ~5%. A linear drop of ~3% was observed within the first 500 hours. The $V_{oc}$ was found to “level off” at ~1000 hours.

Figure 59. Normalized $V_{oc}$ @ Room Temperature vs Time

Figure 60. Normalized $V_{oc}$ @ 70°C vs Time
The average $V_{oc}$ drop of ~ 5% was observed in the devices at 70°C as shown in figure 60. This change is tabulated in table 9 showing a reduction in $V_{oc}$ by 43mV.

Table 9. Change in $V_{oc}$ at Room Temperature and 70°C

<table>
<thead>
<tr>
<th>Condition</th>
<th>No Stress</th>
<th>At Voc-2100hrs</th>
<th>At Voc-2100hrs</th>
<th>At Voc-850hrs, Vm-650hrs, Voc-600hrs</th>
<th>At Voc-850hrs, Vm-400hrs, Voc-850hrs</th>
<th>Mean Change (Lightsoak Samples)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample#</td>
<td>9-29A-7E</td>
<td>9-29A-7D</td>
<td>9-29A-7B</td>
<td>9-29A-7F</td>
<td>9-29A-7C</td>
<td></td>
</tr>
<tr>
<td>Change in Voc - Rm Temp (mV)</td>
<td>-8</td>
<td>-39</td>
<td>-44</td>
<td>-40</td>
<td>-48</td>
<td>-43</td>
</tr>
<tr>
<td>Change in Voc - 70°C (mV)</td>
<td>-31</td>
<td>-58</td>
<td>-36</td>
<td>-49</td>
<td>-43</td>
<td></td>
</tr>
</tbody>
</table>

Note: "+" indicates "INCREASE", "-" indicates "DECREASE"

No significant effect on the net $V_{oc}$ was observed even in the devices stressed for some time at their maximum power point, $V_m$. The reduction in $V_{oc}$ can be attributed to increase in recombination currents in the device during stressing as will be shown later in the J-V curves.

Table 10. Change in $V_{oc}$ for Various Stress Periods

<table>
<thead>
<tr>
<th>Part#</th>
<th>Condition</th>
<th>Stress Period, Hours</th>
<th>Stress Period, Hours</th>
<th>Stress Period, Hours</th>
<th>Stress Period, Hours</th>
<th>Stress Period, Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>0-600</td>
<td>600-1000</td>
<td>1000-1600</td>
<td>1600-2114</td>
</tr>
<tr>
<td>9-29A-7E</td>
<td>No Stress</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9-29A-7D</td>
<td>At Voc-2100hrs</td>
<td>-21.72</td>
<td>-18.91</td>
<td>10.22</td>
<td>-8.50</td>
<td>-9.73</td>
</tr>
<tr>
<td>9-29A-7B</td>
<td>At Voc-2100hrs</td>
<td>-24.80</td>
<td>-16.01</td>
<td>17.83</td>
<td>-21.17</td>
<td>-11.04</td>
</tr>
<tr>
<td>9-29A-7F</td>
<td>At Voc-850hrs, Vm-650hrs, Voc-600hrs</td>
<td>-18.17</td>
<td>-3.54</td>
<td>-1.73</td>
<td>-16.76</td>
<td>-10.05</td>
</tr>
</tbody>
</table>

Note: "+" indicates "INCREASE", "-" indicates "DECREASE"
The breakdown of parametric change over time is shown in table 10. It is hard to conclude if the drop in \( V_{oc} \) is gradual or abrupt from this tabulation as the drop in \( V_{oc} \) at each point is so close to measurement error of 10-15mV.

![Figure 61. \( V_{oc} \) @ Room Temperature and 70°C vs Time During LS @ \( V_{oc} \)](image)

The \( V_{oc} \) trend of a representative sample @ \( V_{oc} \) (9-29A-7D) throughout the stressing period is shown in figure 61. It shows a linear degradation of \( V_{oc} \) within the first 1000 hours and a subsequent “leveling off” both at room temperature and at 70°C.

The \( V_{oc} \) trend of a sample stressed first @ \( V_{oc} \) for the first 850 hours, then at its maximum power point for 400 hours and then brought back to \( V_{oc} \) for another 850 hours (9-29A-7C) is shown in figure 62. A linear drop in \( V_{oc} \) can be seen during the first 850 hours. A sudden drop in \( V_{oc} \) by \(~15mV\) can be noted during its presence @ \( V_m \) (maximum power point) when current flows through the device under stress. However, the \( V_{oc} \) still “levels off” following the same trend of the devices under stress at \( V_{oc} \). The \( V_{oc} \) recovers by \(~10mV\) after the device is brought back to being stressed at \( V_{oc} \) instead of \( V_m \). This phenomenon is most likely due to the field assisted migration of charged impurities like Cu, Cl-related defects into the bulk and junction during
stress at \( V_m \) as there is continuous flow of current in the device, causing increased recombination losses. The recovery in \( V_{oc} \) and FF when brought back to stressing at \( V_{oc} \) indicates that the losses are reversible.

![Figure 62. \( V_{oc} \) @ Room Temperature and 70°C vs Time During LS @ \( V_{oc} \), \( V_m \) and \( V_{oc} \)](image)

The sudden drop in \( V_{oc} \) of this device at ~1900 hours is due to increased leakage current caused by shunting observed in this device. Due to the polycrystalline nature of this junction, migration of ionic impurities and interstitial defects can form shunting paths along the grain boundaries causing sudden deterioration in device performance. Cases where shunted devices recover over time have also been observed. This latter drop could also be due to a local defect (some type of catastrophic event) that simply brought down the performance. Study of micro-nonuniformity of CdS/CdTe polycrystalline devices clearly show that small defective regions - on the order of a few microns - can cause a significant drop in performance because they act like shunting weak diodes [26].
5.2.2 Effect on Fill Factor (FF)

A net reduction in fill factor was observed due to light soaking. The normalized FF over time from room temperature measurements are shown in figure 63. The witness sample showed a 3% reduction in FF.

![Normalized FF @ Room Temperature vs Time](image)

Figure 63. Normalized FF @ Room Temperature vs Time

An average reduction of ~5% was observed for the light soaked devices at room temperature. This reduction has occurred within the first 1000 hours. The fill factor has leveled off between 1000-2100 hours for devices stressed at $V_{oc}$. The fill factor shows an abrupt increase when maintained at $V_m$ for two devices 9-29A-7F & 9-29A-7C. As soon as the devices are returned to $V_{oc}$, fill factors also drop to the previous values.
The normalized FF for devices maintained at $V_{oc}$ (9-27A-7D, 9-29A-7B) at 70°C is shown in figure 64. An interesting detail captured here that was missed in the earlier normalized plot at room temp. is the increase in FF by 3-10% during the initial 100 hours of light soaking. A linear drop was observed after this initial increase.

Figure 65. Normalized FF @ 70°C vs Time During LS @ $V_{oc}$, $V_m$ and $V_{oc}$
The normalized FF of the other two devices (9-29A-7F, 9-29A-7C) showed a similar trend for the first 850 hours when they were stressed at $V_{oc}$. When the devices were subjected to a load keeping them at the maximum power point, there was an abrupt drop in FF at 70°C. The FF also recovered over time moving towards its original value when stressed at $V_{oc}$. This data at 70°C conflicts with the FF data at room temperature (figure 65), where it was observed to have shown some recovery @ $V_m$. This could be a result of lattice scattering in the materials at higher temperatures that will affect the carrier mobility. It could also be a result of deep level defects being active at higher temperature and inactive at room temperature changing the FF. The drop in FF is recoverable. One device (9-29A-7C) returns to its original value as soon as it is brought back to stressing at $V_{oc}$. The FF of device 9-29A-7F is more unstable and takes longer to return to its original value.

The increase in FF within the first 100 hours can be clearly explained by examining the $R_{sh} @ J_{sc}$ which is a good indicator of “collection losses” of the devices. Figure 66 of representative sample 9-29A-7C suggests the $R_{sh} @ J_{sc}$ exhibits a rather “fast” increase from about 500 to 2000 $\Omega$-cm$^2$ in the first 100 hours and then appears to steadily decrease (the data scattering observed is due to noise in the light J-V data near $J_{sc}$). This change appears to “mirror” the improvement observed in the FF suggesting improved collection. The increase in depletion width from C-V analysis shown later supports this observation. An increase in $J_0$ which is directly proportional to the widening of SCR was also observed [8].

The sudden drop in FF, when a device was stressed at $V_m$, can also be explained by the sudden drop in $R_{sh} @ J_{sc}$ seen below at 70°C. The $R_{sh} @ J_{sc}$ trend at room temperature does not show this drop explaining the higher FF measured at room temperature (figure 63) during this stress period. The deep level defects are most likely activate at 70°C but not at room temperature. Since the room temperature measurement in figure 63 is taken after allowing the device to cool down and recover for at least 8-10 hours, this drop in FF is not observed. The decrease in $R_{sh} @
J_{sc} suggests an increase in the “collection losses” possibly due to the field assisted migration of charged impurity defects to the SCR causing it to shrink. A decrease in the leakage currents can be seen from the dark J-V curves. The degradation at V_m are reversible as observed in figure 66 when the device is brought back to light soaking at V_{oc}.

![Figure 66. Normalized R_{sh} @ J_{sc} at 70°C vs Time During LS @ V_{oc}, V_m and V_{oc}](image)

The average reduction in absolute % of FF is ~3% at both room temperature and 70°C. The FF in a device is affected by reduction in R_{sh} @ J_{sc} (collection losses) and increase in R_s. A linear decrease in R_{sh} @ J_{sc} was observed after the initial increase for the first 100 hours which explains the drop in FF.

A point to be noted from the above results is that the initial increase in FF seen here cannot be expected for all light stressed samples, though similar improvement in efficiency was reported by BP solar in CdTe modules [27]. Light stress studies done on similar USF samples [22] have not shown this effect.
Table 11. Change in FF @ 25°C and 70°C for LS Devices

<table>
<thead>
<tr>
<th>Sample#</th>
<th>9-29A-7E</th>
<th>9-29A-7D</th>
<th>9-29A-7B</th>
<th>9-29A-7F</th>
<th>9-29A-7C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Change in FF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rm Temp (%)</td>
<td>-2</td>
<td>-3</td>
<td>-2</td>
<td>-3</td>
<td>-5</td>
</tr>
<tr>
<td>Change in FF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>70°C (%)</td>
<td>-4</td>
<td>-3</td>
<td>-2</td>
<td>-3</td>
<td>-3</td>
</tr>
</tbody>
</table>

Note: "+" indicates "INCREASE", "+" indicates "DECREASE"

The change in FF for light soaked devices as shown in table 11 decreases by ~3% irrespective of the light soaking conditions. The breakdown of this absolute FF variation over time is shown in table 12. The changes observed have already been described while discussing the normalized trend plot.

Table 12. Change in FF @ 25°C over Various Stress Periods

<table>
<thead>
<tr>
<th>Part#</th>
<th>Condition</th>
<th>0-600</th>
<th>600-1000</th>
<th>1000-1600</th>
<th>1600-2114</th>
<th>Average</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>9-29A-7E</td>
<td>No Stress</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-2</td>
<td></td>
</tr>
<tr>
<td>9-29A-7D</td>
<td>At Voc-2100hrs</td>
<td>-4</td>
<td>-2</td>
<td>-1</td>
<td>3</td>
<td>-1</td>
<td>-3</td>
</tr>
<tr>
<td>9-29A-7B</td>
<td>At Voc-2100hrs</td>
<td>-3</td>
<td>-3</td>
<td>0</td>
<td>4</td>
<td>0</td>
<td>-2</td>
</tr>
<tr>
<td>9-29A-7F</td>
<td>At Voc-850hrs, Vm-650hrs, Vm-600hrs</td>
<td>-2</td>
<td>1</td>
<td>-8</td>
<td>7</td>
<td>-1</td>
<td>-3</td>
</tr>
<tr>
<td>9-29A-7C</td>
<td>At Voc-850hrs, Vm-400hrs, Vm-850hrs</td>
<td>-3</td>
<td>2</td>
<td>-5</td>
<td>1</td>
<td>-1</td>
<td>-5</td>
</tr>
</tbody>
</table>

Note: "+" indicates "INCREASE", "+" indicates "DECREASE"
5.2.3 Effect on Short-Circuit Current Density ($J_{sc}$)

Two distinct changes were observed in $J_{sc}$ at room temperature and 70°C. An increasing trend was observed from room temperature measurements for the stressed devices. No significant change was observed to the $J_{sc}$ of the unstressed device.

![Figure 67. Normalized $J_{sc}$ @ 25°C vs Time for LS Samples](image)

This observation was confirmed by spectral response (SR) measurements of the devices. SR measurements were taken only at the beginning and end of the stressing period; no SR data is available during the light soaking period. A representative SR plot of device 9-29A-7D is shown in figure 68.
No significant change in $J_{sc}$ is seen for the unstressed witness sample 9-29A-7E. The lightsoaked device shows an increase in $J_{sc}$ by 1.1mA/cm². The SR plot also shows clearly the increase in current collection in the “red region”.

The normalized $J_{sc}$ at 70°C is shown in figure 69. The sudden jump in $J_{sc}$ at ~250 hours is due to a change in the light source. The gradual drop in $J_{sc}$ over time is not consistent with the $J_{sc}$ measurements at room temperature. This result could not be validated by high temperature SR measurements as the capability currently does not exist at USF. This observation can be an “artifact” caused by the aging of the light bulbs used for light soaking or it could also be due to reduced mobility of charge carriers due to lattice scattering at high temperature or activation of deep level defects at high temperature.
Figure 69. Normalized $J_{sc}$ of LS Samples at 70°C

Table 13 outlines the change in $J_{sc}$ observed in each of the devices at room temperature. An increase in $J_{sc}$ is observed possibly due to the widening of SCR and improved collection shown by C-V measurements.

Table 13. Change in $J_{sc}$ for Control and Lightsoak Samples

<table>
<thead>
<tr>
<th>Condition</th>
<th>No Stress</th>
<th>At Voc-2100hrs</th>
<th>At Voc-2100hrs</th>
<th>At Voc-850hrs, Vm-650hrs, Voc-600hrs</th>
<th>At Voc-850hrs, Vm-400hrs, Voc 850hrs</th>
<th>Mean Change (Lightsoak Samples)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample#</td>
<td>9-29A-7E</td>
<td>9-29A-7D</td>
<td>9-29A-7B</td>
<td>9-29A-7F</td>
<td>9-29A-7C</td>
<td></td>
</tr>
<tr>
<td>Change in $J_{sc}$ (SR) (mA/cm²)</td>
<td>0.1</td>
<td>1.1</td>
<td>0.5</td>
<td>1.2</td>
<td>0.7</td>
<td>0.9</td>
</tr>
<tr>
<td>Change in $J_{sc}$ Rm Temp (mA/cm²)</td>
<td>0.4</td>
<td>0.9</td>
<td>0.9</td>
<td>1.0</td>
<td>1.8</td>
<td>1.1</td>
</tr>
</tbody>
</table>

Note: "+" indicates "INCREASE", "-" indicates "DECREASE"
5.2.4 Effect on Shunt Resistance ($R_{sh}$)

The normalized $R_{sh} @ J_{sc}$ for room temperature measurements is shown in figure 70. The $R_{sh} @ J_{sc}$ values are indicative of collection losses but cannot explain changes to leakage currents in the device as previously discussed. Thus, an increase in $R_{sh} @ J_{sc}$ suggests improved collection of photo-generated carriers and a decrease suggests higher collection losses.

Figure 70. Normalized $R_{sh} @ J_{sc}$ of LS Samples at 25°C

The general trend showed an initial improvement in collection and subsequent drop after the first 1000 hours. The data is noisy due to noise in light J-V at $J_{sc}$. The witness device also shows an improved collection possibly due to passivation of deep level defects.

The normalized $R_{sh}$ at 70°C is shown in figure 71 for devices at $V_{oc}$.
Figure 71. Normalized $R_{sh} @ J_{sc}$ at 70°C of LS Samples at $V_{oc}$

The data shows an initial jump in $R_{sh} @ J_{sc}$ of ~250-300% within the first 100 hours of lightsoaking. This explains the jump in FF and improved collection observed. Subsequently, a linear decrease is observed over time with $R_{sh} @ J_{sc}$ values still higher than the start. This means after the initial passivation effects seen due to light soaking, there is a second slower degradation mechanism working towards increasing the collection losses of the device.

Figure 72. Normalized $R_{sh} @ J_{sc}$ at 70°C of LS Samples at $V_{oc}$, $V_m$ and $V_{oc}$
The normalized $R_{sh}$ at 70°C for devices whose stress conditions was shifted to $V_m$ from $V_{oc}$ after 850 hours shows a sudden drop (figure 72). Increase in deep level defects causing a reduction in SCR and increasing collection losses is the possible cause for this drop in $R_{sh}$ and FF as seen from C-V behavior later. This degradation is reversible as shown when the devices were brought back to light soaking at $V_{oc}$.

### 5.2.5 Effect on Series Resistance ($R_s$)

The change in series resistance at room temperature due to stressing is shown in the table 14. $R_s$ @ $V_{oc}$ and $R_s$ at high currents show both increase and decrease for various devices. The net change is within 1 Ω-cm$^2$. The unstressed device showed improvement in $R_s$, however this does not result in an increase of FF. We can conclude from these results that the variation in $R_s$ is minimal to cause a significant effect on the device performance.

Table 14. Change in $R_s$ for Control and Lightsoak Samples

<table>
<thead>
<tr>
<th>Condition</th>
<th>No Stress</th>
<th>At Voc-2100hrs</th>
<th>At Voc-2100hrs</th>
<th>At Voc-850hrs, Vm-650hrs, Voc-600hrs</th>
<th>At Voc-850hrs, Vm-400hrs, Voc-850hrs</th>
<th>Mean Change (Lightsoak Samples)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample#</td>
<td>9-29A-7E</td>
<td>9-29A-7D</td>
<td>9-29A-7B</td>
<td>9-29A-7F</td>
<td>9-29A-7C</td>
<td></td>
</tr>
<tr>
<td>Change in $R_s$</td>
<td>-0.85</td>
<td>0.03</td>
<td>0.50</td>
<td>0.00</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>@ Voc (ohm-cm$^2$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Change in $R_s$</td>
<td>-0.55</td>
<td>-0.35</td>
<td>0.52</td>
<td>-0.03</td>
<td>0.16</td>
<td>0.08</td>
</tr>
<tr>
<td>@ High Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(ohm-cm$^2$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: "-" indicates "INCREASE", "+" indicates "DECREASE"
5.2.6 Diode Quality Factor, A & Reverse Saturation Current Density, $J_o$

These two parameters can be deduced from the dark J-V curves for normal devices as shown in table 15.

Table 15. Change in A and $J_o$ for Control and Lightsoak Samples

<table>
<thead>
<tr>
<th>Stress Condition</th>
<th>Sample#</th>
<th>No Stress</th>
<th>At Voc-2100hrs</th>
<th>At Voc-2100hrs</th>
<th>At Voc-850hrs, Vm-650hrs, Voc-600hrs</th>
<th>At Voc-850hrs, Vm-400hrs, Voc 850hrs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A-initial</td>
<td>9-29A-7E</td>
<td>1.91</td>
<td>1.56</td>
<td>2.11</td>
<td>2.30</td>
<td>2.20</td>
</tr>
<tr>
<td>A-final</td>
<td>9-29A-7D</td>
<td>2.28</td>
<td>2.81</td>
<td>1.60</td>
<td>2.40</td>
<td>2.20</td>
</tr>
<tr>
<td>Change in A</td>
<td></td>
<td>0.38</td>
<td>1.25</td>
<td>-0.51</td>
<td>0.10</td>
<td>0.00</td>
</tr>
<tr>
<td>$J_o$-initial</td>
<td>9-29A-7B</td>
<td>2.03E-09</td>
<td>2.76E-11</td>
<td>1.38E-08</td>
<td>1.01E-08</td>
<td>6.73E-08</td>
</tr>
<tr>
<td>$J_o$-final</td>
<td>9-29A-7F</td>
<td>3.62E-07</td>
<td>3.41E-08</td>
<td>4.74E-09</td>
<td>9.57E-08</td>
<td>4.55E-08</td>
</tr>
<tr>
<td>Change in $J_o$</td>
<td></td>
<td>x 100</td>
<td>x 1000</td>
<td>- x 10</td>
<td>x 9</td>
<td>- x 2</td>
</tr>
</tbody>
</table>

Note: "+" indicates "INCREASE", "-" indicates "DECREASE"

An increase in $J_o$ & A is observed causing degradation in $V_{oc}$ & FF. The $J_o$ values extrapolated from slope of dark ln J-V plots @ 0.35-0.55V are good qualitative indicators but not accurate quantitatively. Though the projected tabulation for 9-29A-7B shows a reduction of $J_o$ after stressing, the ln dark J-V plot shows a definite increase in recombination current after stress. In devices with high recombination currents, when A is deduced from dark J-V at low forward bias, unrealistic numbers above a typical of “1-2” are observed along with higher $J_o$. 

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5.2.7 Dark J-V Analysis

The dark J-V curves for a witness device are shown in figure 73.

![Figure 73. Ln(J)-V and Linear J-V in the Dark for Witness Device Stored @ Room Temperature](image)

From the ln J-V plot, an increase in the recombination current was observed despite being under no stress. This is not due to “shunting” as no significant change to light J-V was observed. The increase in recombination current is due to increase in SCR possible due to CdTe compensation as seen in the C-V analysis shown later. An increase in the series resistance is also observed from the linear dark J-V response.

The dark J-V curves of a device stressed at \( V_{oc} \) is shown in figure 74. The ln J-V curve clearly showed higher recombination current with time. The increase in recombination current should result in drop of \( V_{oc} \) over time as already observed. The linear J-V curve in the dark had shifted to the left. The “turn-on” of initial J-V was higher than what one would expect from an ideal CdTe device. This turn-on behavior has been previously explained by Dan Oman [7] as coming from the CdS/SnO\(_2\) interface acting as a blocking diode against the main junction. This results in the dark J-V turning “ON” after the breakdown of this blocking diode at voltages...
higher than $V_{oc}$ of the device, resulting in the crossover of dark and light I-V. Thus, the shift suggests a reduction of this barrier which can occur: 1) if the CdS doping is enhanced 2) if the barrier can be overcome by tunneling mechanisms. SIMS analysis of light-soaked devices have shown large accumulation of Cu in CdS in quantities higher than during thermal stress [21].

This is due to the diffusion of Cu ions into the bulk CdTe, CdS and junction. GB diffusion of Cu ions is known to be the dominant mechanism. Thus Cu interstitial accumulation will increase the CdS doping, as it acts as a shallow donor. Another possibility is that Cu could exist as a substitutional impurity compensating CdS initially. This explains the shift of J-V to the right initially. Upon light soaking, the Cu could possibly convert to an interstitial impurity species reducing the CdS compensation. This can explain the shift in dark J-V to the left within the first 100 hours of light soaking.

A device stressed at $V_{oc}$ for 850 hours, then at $V_m$ for 400 hours and returned back to $V_{oc}$ for the remaining 850 hours is shown in figure 75. From the ln J-V curve below it can be noted...
that this device was shunted initially with high leakage currents. The start of lightsoak stressing had resulted in a recovery of this device and a reduction in the leakage current possibly due to localized defect rearrangement. However this recovery was not permanent and the device was shunted again towards the end. The linear dark J-V curve showed a very interesting behavior. First, a decrease in slope was observed by light soaking due to reduction in $R_s$ reducing dark & light J-V cross-over.

![Figure 75. Ln(J)-V and Linear J-V in the Dark for LS Device at $V_{oc}$, $V_m$ and $V_{oc}$](image)

However, when the device is maintained at $V_m$ with current flowing in the device under load, the $R_s$ increases and shifts the curve to the right again. An immediate recovery from this effect is seen when the device is brought back to stressing under $V_{oc}$. The $R_s$ variation is possibly due to Cu related defect morphing in CdS. Initially and during light soaking at $V_m$, Cu related defects possibly compensate CdS, increasing its $R_s$. During light soaking at $V_{oc}$, reduction in CdS compensation occurs possibly due to Cu related interstitial defects.
### 5.2.8 Light J-V Analysis

From this J-V curve of the witness device (figure 76), no significant changes in $V_{oc}$ & FF can be seen. A small increase in $R_s$ was observed from both the dark and light J-V, but no significant change in performance was seen.

![7E @ rm temp](image1)

Figure 76. Light J-V of a Witness Device Stored at Room Temperature

![7D @ rm temp](image2)

Figure 77. Light J-V of a LS Device @ $V_{oc}$
The Light J-V curve at room temperature for a representative light soaked device is shown in figure 77. Along with the decrease in $V_{oc}$ and FF, the elimination of cross-over for light and dark J-V is the most significant observation. The cross-over behavior is usually attributed to a barrier present at the front of the device (CdTe/CdS or SnO$_2$/CdS interface) [7]. Lightsoaking has shown to reduce or eliminate this barrier due to reduction in photoconductivity of CdS by saturation with Cu related interstitial donors. Two key observations to be made from the light J-V curves are the absence of:

1) a “kink” in the fourth quadrant

2) “roll-over” of J-V in the first quadrant

Both these phenomenon indicate degradation of the back contact resulting in blocking contact formation. Thus, it is fair to conclude that no significant degradation in back contact was observed due to illumination stressing in CdTe devices fabricated at USF.

5.2.9 Capacitance-Voltage Measurements (C-V)

By plotting $N_A$ vs bias voltage applied to measure capacitance for the control sample, changes in $N_A$ can be observed even without any stressing (figure 78). A reduction in $N_A$ can be observed even without stress possibly due to dopant diffusion along GBs and compensation of CdTe, junction and CdS. This results in increasing the width of the SCR.
Figure 78. $N_A$-V in the Dark for a Witness Device

Light soaking was found to increase the width of SCR possibly due to compensation. Significant decrease in capacitance is observed on all devices after the start of light soaking. All devices show a drop in $N_A$. The presence of a graded bulk in observed with the drop in carrier concentration towards the interface. A plot of the $N_A$ w.r.t bias voltage deduced from the C-V data of a representative device subjected to light soaking @ $V_{oc}$ (figure 79) clearly explains the observations. Much of the change in acceptor concentration at the junction occurs right at the beginning of the stressing period. As illumination reduces the barrier for diffusion of Cu ions from the back contact, significant diffusion occurs into the junction and into CdS layers probably resulting in compensating effects. This can explain the reduction in junction capacitance. Under reverse bias the SCR extends further into CdTe. Thus, the profile in the reverse bias shows the doping in bulk CdTe. An increase in the graded doping profile for CdTe is observed due to possible compensation of CdTe near the junction. Cu diffusion does not significantly reduce the
amount of Cu in the back contact of HgTe:Cu doped graphite paste used in USF devices as observed from the SIMS analysis shown later and reported by others [16].

Figure 79. $N_A$ - $V$ in the Dark for a LS Device @ $V_{oc}$

Significant changes are noted in the devices when they were under load at $V_m$. Large increase in capacitance for cells 7F & 7C when being stressed at $V_m$ was observed suggesting an increase in charged states at the junction interface. Thus higher interface states due to diffusion or possible field-assisted migration of Cu through grain boundaries or formation of Cu related metastable states towards the junction increasing the capacitance. The drastic change in FF could be explained by these species acting as recombination centers. However, it was observed that these changes are reversible. The FF was completely recovered when the device was taken back to light soaking at $V_{oc}$ conditions. $V_{oc}$ degradation was observed to be permanent and no recovery was observed.
The acceptor concentration and depletion widths deduced from C-V curves are shown in table 16. \( N_A \) does not significantly change in the bulk of CdTe. However, \( N_A \) at zero bias shows the doping profile near the junction reduces by an order of magnitude. The widths of SCR can be deduced from the capacitance values and we see an increase in the zero bias depletion width due to reduction in capacitance.

Table 16. \( N_A \) and Depletion Width of Witness and Lightsoak Samples

<table>
<thead>
<tr>
<th>Condition</th>
<th>Part#</th>
<th>Test time</th>
<th>Acceptor Conc. (cm(^{-3})) from</th>
<th>Depletion Width, um @ 0V</th>
<th>Acceptor Conc. (cm(^{-3})) @ 0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Stress</td>
<td>Witness</td>
<td>Start</td>
<td>3.38E+14</td>
<td>1.22</td>
<td>2.02E+14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Finish</td>
<td>7.51E+13</td>
<td>1.76</td>
<td>3.55E+13</td>
</tr>
<tr>
<td>At Voc-2100hrs</td>
<td>9-29A-7D</td>
<td>Start</td>
<td>2.22E+14</td>
<td>1.29</td>
<td>1.76E+14</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.14E+14</td>
<td>2.69</td>
<td>3.90E+13</td>
</tr>
<tr>
<td>At Voc-2100hrs</td>
<td>9-29A-7B</td>
<td>Start</td>
<td>2.47E+14</td>
<td>1.41</td>
<td>1.52E+14</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.18E+14</td>
<td>2.49</td>
<td>1.85E+13</td>
</tr>
<tr>
<td>At Voc-850hrs, Vm-650hrs,</td>
<td>9-29A-7F</td>
<td>Start</td>
<td>2.23E+14</td>
<td>1.42</td>
<td>1.38E+14</td>
</tr>
<tr>
<td>Voc-600hrs</td>
<td></td>
<td></td>
<td>2.22E+14</td>
<td>2.93</td>
<td>3.55E+13</td>
</tr>
<tr>
<td>At Voc-850hrs, Vm-400hrs,</td>
<td>9-29A-7C</td>
<td>Start</td>
<td>2.54E+14</td>
<td>1.31</td>
<td>1.81E+14</td>
</tr>
<tr>
<td>Voc-850hrs</td>
<td></td>
<td></td>
<td>2.17E+14</td>
<td>3.35</td>
<td>2.17E+13</td>
</tr>
</tbody>
</table>

5.3 SIMS Analysis of Thermal Stress Devices

The elemental analysis of degraded devices by SIMS analysis helps understand the possible root cause of device degradation. Studies have already identified two possible species most likely responsible for the parametric changes, Cu and Cl. The profile in figure 80 is the Cu and Cl profiles in devices which were stressed without any contacts for 1500 hours at 70°C and
118°C. Minimal levels of Cu are found in the bulk CdTe. However, high levels of Cu at the CdTe surface and CdS/SnO$_2$ layers for devices with no intentional Cu doping of these substrates are to be noted. This means that a substantial amount of Cu in the device accumulates due to contamination from various starting materials and fabrication processes. It is not clear if the Cu levels at the top surface of CdTe are real or an artifact of SIMS analysis and needs to be verified. If it is real, it can be deduced that Cu contamination accumulates at the two regions of highest defectivity namely the oxidized CdTe top layer and CdS/CdTe interface. The profiles are similar to non-contacted substrates analyzed without any thermal stressing. Samples contacted after thermal stressing for 1500 hours has shown similar device parameters as a newly made device, which clearly shows that probably the root cause of degradation is Cu is initially present in the contact. Cl levels are relatively higher in the bulk though accumulation occurs at the front and back similar to Cu due to CdCl$_2$ treatment of the substrates.

![Substrate A](image)

Figure 80. SIMS Analysis of Non-contacted Substrates Thermally Stressed to 1500 Hours
Profiles of Cl distribution for both contacted & non-contacted devices are very similar in content and distribution in the device. Profiles of contacted devices before and after stress can be seen in figure 81. Concentration reduces an order of magnitude towards the back-contact but no significant changes were observed in the devices with thermal stress.

![Cl profile](image)

Figure 81. SIMS Comparison of Cl Content Before and After Thermal Stress

The profile in figure 82 shows Cu distribution in a contacted sample with no stressing and two uncontacted samples stressed at 70°C and 100°C. Cu levels are higher in the bulk and an order of magnitude higher at the junction for the contacted sample verifying that Cu from the back contact diffuses into the CdTe and reaches the CdTe/CdS junction and the CdS.
The effect of thermal stress can be seen in the Cu profile in figure 83. Comparison with an unstressed control sample shows higher levels of Cu in the bulk CdTe towards the junction and at the junction for both 70°C and 100°C stressed samples. Note that the Cu levels at the front of CdTe have not significantly reduced which could explain why we see no “roll-over” effect on the stressed devices.
Comparison of Cu distribution at the junction for a non-contacted (figure 84) vs contacted device (figure 85) shows a distinct difference. Cu contamination in the non-contacted sample accumulates at CdS/SnO₂ interface and in the SnO₂ and not the CdTe/CdS junction. This result is questionable and may actually be an artifact as Cu diffusion into SnO₂ is unlikely. The high level of Cu in the front of CdTe surface also needs to be confirmed.

The levels of Cu increase by an order of magnitude after contact application and anneal which redistributes the Cu into the junction.
Figure 84. SIMS Analysis of Non-contacted Sample

Figure 85. SIMS Analysis of a Contacted Sample
5.4 Effect of Re-contacting Thermal Stress Samples

A device thermally stressed at 70°C for ~3000 hours was re-contacted after stripping the existing contact by sonication in acetone. This was a device on which thermal stressing studies were initiated. It was annealed at 70°C in incremental steps of 1, 2, 4, 8 hours and so on. This resulted in the device being tested ~250 times during its 3000 hours anneal. The CdTe layer was re-contacted with graphite paste (Cu : HgTe doped) after preparing the top surface of CdTe by etching in Br2/methanol solution to leave a Te rich surface. The changes to device parameters are tabulated in table 17.

Table 17. Effect of Re-contacting on Device Parameters

<table>
<thead>
<tr>
<th></th>
<th>Jsc(A/cm²)</th>
<th>Voc (V)</th>
<th>FF</th>
<th>Eff. (%)</th>
<th>Rsh @ Jsc (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>initial</td>
<td>0.0211</td>
<td>0.8584</td>
<td>0.703</td>
<td>12.74</td>
<td>923</td>
</tr>
<tr>
<td>2990 hours</td>
<td>0.0221</td>
<td>0.8218</td>
<td>0.425</td>
<td>7.71</td>
<td>522.3</td>
</tr>
<tr>
<td>recontacted</td>
<td>0.0209</td>
<td>0.6860</td>
<td>0.509</td>
<td>7.31</td>
<td>513.6</td>
</tr>
</tbody>
</table>

A significant reduction in Voc was noted after re-contacting due to “shunting” and increased leakage losses in the junction, however the FF has shown improvement. A significant reduction in Jsc was also observed possibly due to increase in recombination losses.

Increased shunting is clearly noted from the ln J-V curve (figure 86) in the dark after re-contacting. The dark J-V curve shows an interesting phenomenon of shifting of the “knee” to the left reducing the light and dark J-V cross-over. This is similar to the observations under illumination stressing. This could explain the elimination of cross-over behavior for lightsoaked devices. Higher Cu diffusion during illumination or re-contact annealing into the junction and CdS could explain the elimination of cross-over behavior. High Cu content was found in light-stressed devices compared to thermally stressed devices most significantly in CdS [16]. Reduction in cross-over was also observed. The light J-V curve of this device (figure 87) demonstrates two key changes. Thermal stressing had significantly reduced the FF of this device
as seen from the high $R_s @ V_{oc}$ along with an onset of a “kink” in the fourth quadrant usually attributed to back contact degradation.

Figure 86. Ln(J)-V and Linear J-V in the Dark for Re-contacted Device

Figure 87. Light J-V for Re-contacted Device
Significant physical deterioration of back contact due to probing ~250 times and electronic degradation (oxide barrier formation) due to exposure to atmosphere and humidity every time it was tested, was thought to be the root cause. Both $R_s @ V_{oc}$ and $R_s @$ high forward currents are improved on recontacting the back surface. Significant drop in $V_{oc}$ and $J_{sc}$ are observed due to shunting and increase in leakage losses due to Cu accumulation. Recontacting of the device has not resulted in any improvement of device efficiency meaning junction losses are most likely non-reversible.

5.5 Comparison of Thermal Stress & Light Soak Results

The comparison of various device parameters of representative samples after 2100 hrs of stressing under illumination and thermal stress in the dark at 70°C are tabulated in table 18. Positive values represent increase in parametrics and negative values indicate a decrease.

Table 18. Device Parameter Comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Thermal Stress (9-29A-11A)</th>
<th>LS (Rm) (9-29A-7D)</th>
<th>LS (70°C) (9-29A-7D)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$J_{sc}$ (mA/cm²)</td>
<td>-0.15</td>
<td>0.87</td>
<td>-1.15</td>
</tr>
<tr>
<td>$V_{oc}$ (mV)</td>
<td>-14</td>
<td>-40</td>
<td>-31</td>
</tr>
<tr>
<td>FF (%)</td>
<td>-4.5</td>
<td>-3.5</td>
<td>-3.8</td>
</tr>
<tr>
<td>$\eta$ (%)</td>
<td>-1.0</td>
<td>-0.6</td>
<td>-1.5</td>
</tr>
</tbody>
</table>

The drop in $V_{oc}$ is higher when stressed under illumination. This is possibly the effect of increase in Cu levels at the junction as explained previously. The drop in $J_{sc}$ under illumination at 70°C could not be verified by high temperature SR and could possibly be a result of “aging” of
the bulbs used for LS. The reduction of carrier mobility due to lattice scattering or collection losses due to active recombination centers at 70°C could also possibly result in the decrease in $J_{sc}$.

The worst effects of degradation are obviously for device operation at 70°C with a net reduction of ~10-27% in efficiency after 2100 hours of illumination stressing.

Comparing the dark & light J-V curves (figure 88), we do not see any significant change between the lightsoaked device and thermal stressed device except for a higher drop in $V_{oc}$. Both devices show a small increase in $R_s$ both at high current and at $V_{oc}$. The dark J-V cross-over however is distinctly different for both with cross-over nearly eliminated after illumination stress and increasing for thermally stressed device. The dark to light J-V cross-over is more than 0.8V for a thermally stressed device as shown in figure 88.

To understand this cross-over phenomenon better, J-V analysis under band pass filters of 460nm, 640nm, 800nm and light J-V were performed. Illumination with various filters has reduced the cross-over, with 460nm filter reducing it most followed by 640nm and 800nm (figure 89). With SnO₂ bandgap of 3.5eV(360nm) and CdS bandgap of 2.42eV(510nm), most of the 460nm blue light should be absorbed in the CdS with some light reaching CdTe if the CdS is very thin. This results in the reduction of the $R_{sh}$ of this front contact “leaky” diode (photodoping of CdS). Thus the J-V under this filter shows reduction in crossover as previously proposed by Dan Oman [7]. Both red light filters 640nm and 800nm show higher crossover. This confirms the presence of a front contact barrier dependent crossover phenomenon. The parametric summary of band pass filter testing can only provide qualitative information, as the intensity of incident light for each filter was not constant. But since the irradiance of blue light is lower compared to red light for AM1.5 light spectrum, it means significantly lower levels of blue light photons could successfully reduce the front contact barrier compared to the higher levels of red light. This confirms that the cross-over effect is due to photodoping of CdS. The general trend of low FF for higher wavelengths was observed (figure 90). The low FF of “red light” signifies collection losses
in the bulk CdTe due to thermal stressing with lifetime of the carriers generated in the CdTe bulk lost to recombination before reaching the depletion region.

Figure 88. J-V Comparison of LS and TS Device at 70°C
Figure 89. J-V Comparison of TS Device Under Band Pass Filters

Figure 90. FF Variation of TS Device Under Various Band Pass Filters
The dark J-V response of a lightsoaked device under various filters shows no significant crossover from dark to light and by use of any filters (figure 91).

Figure 91. J-V Comparison of LS Device Under Band Pass Filters

Figure 92. FF Variation of LS Device Under Various Band Pass Filters
The change in FF under the filters is shown in figure 92. No significant change is observed for all the filters. The small fluctuations observed are due to light intensity dependence of FF. The lowest FF measured was for observed for light J-V under the solar simulator under AM1.5 conditions.

5.6 Acceleration Factor for Thermal Stress

A reduction of Voc and FF with increasing temperature of thermal stressing was observed. An Arrhenius rate relationship can be used to determine the acceleration factor (a) for this degradation. We used the average drop in Voc and FF for 3 devices at each temperature of stressing. With the assumption that normal operating conditions for a device is 50°C, the above an acceleration factor of ~ 5 is deduced at 100°C.

Table 19. Acceleration Factor for Degradation of Voc and FF

<table>
<thead>
<tr>
<th>Stress Temperature, °C</th>
<th>a,Voc(mV)</th>
<th>a,FF(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>60</td>
<td>1.4</td>
<td>1.4</td>
</tr>
<tr>
<td>70</td>
<td>1.9</td>
<td>1.8</td>
</tr>
<tr>
<td>80</td>
<td>2.5</td>
<td>2.4</td>
</tr>
<tr>
<td>90</td>
<td>3.2</td>
<td>3.2</td>
</tr>
<tr>
<td>100</td>
<td>4.1</td>
<td>4.1</td>
</tr>
<tr>
<td>120</td>
<td>6.6</td>
<td>6.5</td>
</tr>
</tbody>
</table>

The acceleration factors deduced above in table 19 are by no means statistically complete. Statistically significant sample sizes have to be evaluated in the future to generate accurate degradation factors. We could also possibly generate two acceleration factors one to represent the first 1000 hours of rapid degradation and the second to represent the remaining 1600 hours of gradual degradation.
5.7 Simulation

We have simulated the Voc and FF responses using the diode light I-V equation:

\[ J = J_0 \left[ e^{(V-JR_s)/AKT} - 1 \right] - J_L + (V-JR_s)/R_{sh} \]

The values of \( J_L, R_s, R_{sh} \) deduced from the light J-V curves and \( A, J_0 \) values deduced from the dark J-V curves before and after stressing devices were used to simulate the response.

Table 20. Comparison of Voc and FF Before and After Degradation

<table>
<thead>
<tr>
<th>Stress</th>
<th>Voc, V (meas)</th>
<th>Voc, V (sim)</th>
<th>Voc Change, V (meas-sim)</th>
<th>FF, % (meas)</th>
<th>FF, % (sim)</th>
<th>FF Change, % (meas-sim)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anneal-70°C</td>
<td>0 0.846 0.837 0.009 73.1 75.3 -2.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3600 0.831 0.822 0.009 67.9 72.3 -4.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Anneal-100°C</td>
<td>0 0.836 0.814 0.022 73.7 76.6 -2.9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3600 0.806 1.007 -0.201 53.9 55.2 -1.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Anneal-120°C</td>
<td>0 0.848 0.828 0.02 73.5 74.7 -1.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3600 0.776 1.12 -0.344 44.3 32.9 11.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Illumination - 70°C</td>
<td>0 0.84 0.82 0.02 72.4 76.7 -4.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2100 0.801 0.781 0.02 68.9 70 -1.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: "+" indicates "INCREASE", "-" indicates "DECREASE"

It can be seen from the data in table 20 that a reasonable estimate of the \( V_{oc} \) and FF can be deduced before stressing. Extraction of device parameters such as \( A, J_0, R_{sh}, \) and \( R_s \) for stressed devices is not accurate and therefore quantitative analysis becomes difficult. However, the results presented in this work, clearly demonstrate that even the qualitative changes can be used to study degradation in CdTe cells.

5.8 Summary

Both thermal and illumination stressing have resulted in degradation of devices. When comparing samples stressed at 70°C both thermally and under illumination, similar levels of
degradation in efficiency were observed from room temperature J-V measurements. The major difference in parametric changes between the two conditions has been that illumination stressing has higher reduction in $V_{oc}$ along with increase in $J_{sc}$ (SR analysis) compared to thermal stressing. SIMS analysis has shown that higher accumulation of Cu occurs at the junction and CdS for illumination stress compared to thermal stress conditions [16]. The key difference is how the Cu exists at the CdTe/CdS junction, bulk CdTe, bulk CdS and CdS/SnO$_2$ interface. If Cu exists as an interstitial defect $\text{Cu}_{i}^{+}$, it is a shallow donor state enhancing CdS doping and compensating CdTe. If Cu exists as a substitutional defect, $\text{Cu}_{\text{Cd}}^{-}$ is a deep-level acceptor enhancing CdTe doping and compensating CdS.

Cu diffusion from back contact into the bulk CdTe and accumulation at the junction and CdS has been well documented [16]. It exists predominantly as an interstitial after fabrication diffusing via GBs during contact anneal [16].

1. Light soaking @ $V_{oc}$ enhances the diffusion of $\text{Cu}_{i}^{+}$ from the back contact into the junction and CdS via GB diffusion [16]. GB diffusion being a fast process occurs within 100 hours of lightsoaking. This reduces the net $N_A$ in CdTe and increases the net $N_D$ in CdS. Increase in depletion width from C-V analysis, improved collection from SR analysis and improved FF from J-V analysis in LS devices support this observation within 100 hours. This is also accompanied by an increase in recombination current resulting in a rapid drop in $V_{oc}$ in the first 1000 hours. Deep level defect formation of $\text{Cu}_{i}^{+}$ and related complexes at the junction possibly form this fast component of degradation.

2. Thermal stressing @ $V_{oc}$ is believed to enhance Cu-related substitutional defect formation. However, the fast initial drop in performance within 500 hours is believed to be due to the formation of Cu-related deep level defects similar to LS at the junction and increases with stress temperature. The evidence of increase in recombination currents is
found in the dark J-V analysis. Collection losses were found to increase with stress temperature as shown in the SR analysis. The levels of Cu accumulation at the junction and CdS for thermal stress are lower than during LS [16]. Thus, the doping concentration of CdS is not significantly altered to change the depletion width.

A slower substitutional defect formation is proposed to exist for both light soaking and thermal stress. Deep level Cu and Cl defect complexes or clusters possibly form at the junction and CdS. This will compensate CdS and increase its photoconductivity/resistivity. The continuous degradation of $V_{oc}$ and FF both for light soaking and thermal stressing over time is possibly a result of enhanced substitutional defect formation. This degradation appears to be permanent. Higher temperatures of thermal stressing increase these defects. The high recombination losses and “shunting” observed in devices stressed over 100°C along with reduction in depletion widths corroborate this theory.

Saturation or overdoping of Cu in CdS can lead to:

1. Reduction of the front contact barrier due to higher $N_D$ of CdS.

2. Formation of shunt paths for carriers to tunnel through the CdS/SnO$_2$ interface barrier.

This explains the elimination or reduction of crossover observed during illumination stressing or recontacting thermal stressed devices. However, if Cu substitutes Cd in CdS, which means Cu has to enter the CdS grains and form a deep acceptor, it will compensate the net CdS doping resulting in photoconductive/resistive CdS. This occurs gradually during thermal degradation over time, increasing dark vs light J-V cross-over due to higher front contact barrier.

Front-contact barrier changes observed at the two stress conditions due to photodoping changes of CdS by Cu is proposed to have minimal impact on device degradation. This conclusion can be drawn based on:

1. The varying levels of cross-over observed in high efficiency CdTe devices fabricated at USF.
2. From the fact that elimination of cross-over has not stopped the light stressed devices from further degradation.

The drop in FF accompanied by drop in $R_{sh}$ @ $J_{sc}$ for cells at $V_m$ and increase in J-V cross-over suggests the diffusion or possible field assisted migration of charged Cu ions and their defect complexes at the junction and CdS. These defects can act as traps, deep states and form shunt paths along the GBs causing degradation of the junction. Increased capacitance during stress @ $V_m$ supports the presence or creation of the interface states. These changes have been found to be reversible. Re-stressing the devices at $V_{oc}$ shows immediate recovery of FF and J-V cross-over. Thus, the front-contact barrier changes are suggestive of the diffusion and migration of Cu ions and its defect states.

The absence of significant roll-over for both stress mechanisms signifies back contact integrity with no significant back contact barrier formation. Severe physical degradation and possible oxidation of back contact in the “original” thermal stressed device (figure 88) had shown the presence of back contact barrier.

It can be concluded that degradation of CdTe/CdS devices fabricated at USF mainly occurs at the junction and not at the back contact. DLTS analysis on USF samples had identified the presence of various deep level defects pertaining to Cu and its complexes [23] like $Cu^+_1$, $Cu_{Cd}^-$, $(Cu^+_1 - 2Cu_{Cd}^-)^+$ along with other defects associated with $V_{Cd}$ complexes. Increase in these defect levels are the root cause of junction degradation. It is necessary to quantify these defect levels in stressed devices in the future using simulation tools and better characterization methods.
CHAPTER 6

CONCLUSIONS

Both thermal and illumination stressing have resulted in degradation of devices. Two components of degradation were observed. The faster degradation component is seen both during thermal and illumination stressing. Cu interstitial diffusion from the backcontacts and their defect complexes contribute to the fast drop in $V_{oc}$ and FF. As the concentration of Cu interstitials are higher due to lightsoaking than thermal degradation [16], the performance drop is higher for lightsoaking than thermal stress. A slower component of degradation is also present that causes continual reduction in performance of the device. Substitutional defects and complexes of Cu in the junction and CdS are attributed to this degradation and the resulting parametric loss was found to be irreversible. As both interstitial and substitutional defects exist in varying concentrations after stressing, different levels of degradation are observed for thermal stress and lightsoaking.

It was concluded that degradation of CdTe/CdS devices fabricated at USF mainly occurs at the junction and not at the contact. DLTS analysis on USF samples has identified the presence of various deep level defects pertaining to Cu and its complexes [23] like $\text{Cu}_i^+$, $\text{Cu}_{\text{Cd}}^+$, $(\text{Cu}_i^+ - 2\text{Cu}_{\text{Cd}}^-)^-$ along with other defects associated with $V_{\text{Cd}}$ complexes. Increase in these defect levels is possibly the root cause of junction degradation. It is necessary to quantify these defect levels in stressed devices in the future.

Large statistically valid sample sizes have to be subjected to thermal and lightsoak stress to quantify the parametric losses and calculate acceleration factors. This will enable modeling of
the performance degradation. Bias stressing studies are required to further understand the field enhanced migration of defects. DLTS studies of stressed samples are required to identify and quantify the deep-level defects. Techniques to reduce junction degradation have to be investigated. It may be possible to optimize the quantity of Cu penetrating the junction in high efficiency CdTe/CdS solar cells to prevent degradation. Passivating the junction defects could reduce rate of degradation and has to be investigated. Alternative stable Cu free back contacts can also be developed to prevent the junction degradation.
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ABOUT THE AUTHOR

Bhaskar Reddy Tetali received his Bachelor’s Degree in Electronics and Communication Engineering from Andhra University, Visakhapatnam, A.P, India in 1994 and M.S. in Electrical Engineering in 1996 from the University of South Florida (USF). He has been associated with the Compound Semiconductor Laboratory (CSL) at USF since 1994 and his research has focused on development of CdTe/CdS thin film solar cells. His Master’s work involved optimizing CdTe/CdS device performance on soda-lime substrates. He had successfully fabricated devices with >13% conversion efficiencies on low-cost substrates (Highest efficiency of 13.6% achieved on a device tested at NREL – A record efficiency at that time). The focus of his dissertation has been on studying and understanding the stability of CdTe/CdS solar cells and identifying the degradation mechanisms. This will help develop solutions to increase the lifetime of CdTe/CdS solar cells and make this thin film technology financially viable for terrestrial applications as an alternative source of renewable energy.

He has worked both as a Research Assistant (RA) with CSL and Teaching Assistant (TA) with the Electrical Engineering Department. His TA experience includes teaching Electronics Lab, Logic Lab, Microprocessor Lab, Electrical Circuits, Linear Systems Analysis, RF Microwave Circuits and Linear Control Systems.

He was selected into the reputed “Worldwide Rotation Program” as a Rotation Engineer at International Rectifier (IR) in 2001. He is currently with the Advanced Technologies Division (FET R&D) of IR working as a Design Engineer involved in designing power MOSFETs for Automotive and DC-DC applications.