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Implant annealing of Al dopants in silicon carbide using silane overpressure

Shailaja P. Rao
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Implant Annealing of Al Dopants in Silicon Carbide using Silane Overpressure

by

Shailaja P Rao

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering
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Implant Annealing of Al Dopants in Silicon Carbide using Silane Overpressure

Shailaja P Rao

ABSTRACT

The goal of this research is to develop a post-implantation annealing process in silicon carbide (SiC). Due to the low diffusivities of dopants in SiC, even at temperatures in excess of 2000°C, diffusion is not a suitable process to achieve selective, planar doping. Ion implantation is therefore the most suitable means for achieving selective doping in SiC crystals. The strong covalent bonding in SiC requires that selective doping be performed via high-energy ion implantation. As a consequence of the high ion energy and flux, there is considerable lattice damage to the crystal surface. To repair the damage caused by the implantation, as well as to electrically activate the dopants, it is important to perform post-implantation thermal annealing at temperatures greater than 1600°C. However annealing at such high temperatures decomposes the SiC crystal surface due to the selective out-diffusion of Si causing surface morphology degradation. In this research two processes, both using a silane-based SiC CVD reactor, have been realized to minimize the evaporation of Si. This is accomplished by providing Si overpressure above the wafer surface during annealing thus suppressing the evaporation of Si from the lattice.

Post-implantation anneals were performed in both hot-wall and cold-wall silane-based chemical vapor deposition (CVD) reactors. For each process temperature developed, silane was added to a stream of Ar in such a concentration such that the
suppression of step-bunching, a well known phenomenon caused by the evaporation of Si at the surface, was achieved. The surfaces were studied after annealing via plan-view secondary electron microscopy (SEM) and atomic force microscopy (AFM). The resulting surface morphology was found to be both step-free and smooth. Results of the annealing processes developed, the surface characterization performed and electrical data relating to the dopant activation and implanted region conductivity are presented.
CHAPTER 1

INTRODUCTION

1.1 Properties of Silicon Carbide

Silicon Carbide (SiC) is evolving into a realistic alternative to Si for use in high temperature and high power electronic and mechanical devices, due to its wide band gap and high thermal conductivity. Some of these properties of SiC indicate the potential for high density integration of SiC devices [1]. Other superior physical properties of SiC, when compared to narrow band-gap semiconductors such as Si, include a lower intrinsic carrier concentration (by 10 orders of magnitude), higher electric breakdown field (4-20 times greater), higher thermal conductivity (3-13 times higher), and larger saturated electron drift velocity (2-2.5 times faster) [2, 3], which are explained in detail in the next paragraph. In addition to this silicon dioxide (SiO$_2$), which has the highest dielectric strength of all insulators and a key ingredient in the making of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the native oxide of SiC and can be thermally grown in dry oxygen or steam ambients [4]. Most of the other compound semiconductor materials such as GaN do not enjoy this particular advantage.

SiC possesses unique physical and chemical properties which enable its use under severe conditions (i.e., harsh environments) hence making it a promising material for
many electronic and optoelectronic device applications. Some of the unique properties of SiC are as follows:

(a) **Wide bandgap:** SiC with its wide bandgap has a higher intrinsic temperature compared to Si [5]. Hence at high temperatures the problem of device failure due to the thermal generation of electron-hole pairs in excess of the number of dopant-provided free carriers is overcome because of its wide bandgap.

(b) **High thermal conductivity:** As the temperature of a semiconductor increases the physical properties of the material change, especially the carrier mobility, which decreases with increasing temperature [6]. SiC is an excellent thermal conductor enabling heat to flow more readily than in other semiconductor materials. As a point of reference the thermal conductivity of SiC at room temperature exceeds the thermal conductivity of any metal [7]. This property enables the use of SiC for the manufacture of very high-power electronic devices, in which large amount of heat is generated during device operation. [6].

(c) **High electrical field:** Due to its wide bandgap, the impact ionization energy is much higher in SiC compared to Si or GaAs. SiC can withstand voltage gradients as high as 2.2 MV/cm, which is ten times higher than the value in Si [7]. This property allows the electric field to build up to a high value in the material without the avalanche multiplication of ionized carriers, which leads to the material electrical breakdown effect [8]. For a device designed for the same breakdown voltage using Si and SiC, the SiC device can have much thinner depletion region due to this parameter. Therefore the doping concentration in SiC can be much higher, which helps the series resistance of the active layers to be low due to the higher doping concentration.
**High saturated electron drift velocity:** SiC has a high saturated electron drift velocity of $2 \times 10^7$ cm/sec, which enables SiC devices to be operated at high frequencies [9]. At low the electric fields, drift velocity of the electron in a semiconductor is proportional to the electric field with a proportionality constant represented by the low-field carrier mobility. However, at higher fields the direct proportionality fails and the velocity saturates and stays constant with increasing electric field.

In addition to these advantageous properties, SiC exhibits two dimensional polymorphism called polytypism. Polytypes are alike in the two dimensions of a close-packed plane but differ in the stacking sequence in the dimension perpendicular to that plane. There are several hundred stacking orders possible and hence many polytypes of SiC exist [10]. The individual bond lengths of the polytypes are identical but the crystal symmetry is determined by the stacking periodicity, which is the main cause for the different electrical and optical properties of the polytypes as listed in Table 1.1 [2]. The polytypes are divided into three basic crystallographic categories: cubic (C), hexagonal (H) and rhombohedral (R). However to fabricate devices on single crystal substrates only a few of the polytypes are stable; these are 4H-, 6H- and 3C-SiC. 3C-SiC is not available in bulk form via seeded sublimation growth but can be grown on Si or 6H-SiC. Unfortunately there has been limited success due to the large (> 20%) lattice mismatch between $\beta$-SiC (i.e., 3C-SiC) and Si [11]. Therefore 6H-SiC and 4H-SiC are the only SiC polytypes currently available in bulk wafer form, with 2” and 3” wafers in production and 4” wafers demonstrated by several wafer vendors. Among all the polytypes, 4H-SiC has become preferred due to the more isotropic nature of many of its electrical properties.
Table 1.1: Physical properties of some of the common polytypes of SiC at room temperature compared to Si [2, 3, 6].

<table>
<thead>
<tr>
<th>Properties</th>
<th>3C-SiC</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap (eV)</td>
<td>2.39</td>
<td>3.00</td>
<td>3.23</td>
<td>1.12</td>
</tr>
<tr>
<td>Critical Electric Field (MV/cm)</td>
<td>2.12</td>
<td>2.5</td>
<td>2.2</td>
<td>0.25</td>
</tr>
<tr>
<td>Thermal Conductivity (W/(cm-K))</td>
<td>5.0</td>
<td>5.0</td>
<td>4.9</td>
<td>1.5</td>
</tr>
<tr>
<td>Saturated Electron Velocity (x 10^7 cm/s)</td>
<td>2.5</td>
<td>2.0</td>
<td>2.0</td>
<td>1.0</td>
</tr>
<tr>
<td>Electron Mobility $\mu_n$ (cm^2/(V-s))</td>
<td>750</td>
<td>370</td>
<td>1000</td>
<td>1500</td>
</tr>
<tr>
<td>Hole Mobility $\mu_p$ (cm^2/(V-s))</td>
<td>40</td>
<td>90</td>
<td>115</td>
<td>600</td>
</tr>
</tbody>
</table>

1.2 Motivation of this Research

One of the most important process steps for any semiconductor is the ability to selectively dope various regions on a semiconductor die and/or wafer. In conventional semiconductors such as silicon (Si) or gallium arsenide (GaAs), the process for selective doping is well established and is based on the thermal diffusion of dopants, which is a well understood and characterized process. These processes cannot be directly adapted into SiC technology because of the inherent material properties of SiC, namely the very strong covalent bonding of the lattice which makes thermal diffusion impractical. One approach used to achieve selectively doped regions on a SiC die is to dope various layers during epitaxial growth. One then etches back the areas that are not to be doped at this level, albeit at the expense of several additional processing steps. While this is a valid approach, it does not result in a planar selectively-doped area, which is very important for making SiC integrated circuits economically attractive [12].
Ion implantation and diffusion are the two processes that have been widely used in the Si community for selective doping. However, due to low diffusivities of the dopants in SiC even at temperatures in excess of 2000°C, diffusion is not a suitable process in SiC [12, 13]. Ion implantation is therefore the only feasible technique for planar area selective doping of SiC. In this process, the substrate is bombarded with heavy ions, which not only cause damage to the crystal lattice but also the implanted ions predominantly occupy interstitial lattice sites. In order to repair the damage as well as activate the dopants a high-temperature thermal annealing step is required after implantation. This research focuses specifically on the anneal process and the basic concept employed will be discussed in section 1.3.

Post ion implantation annealing is not a completely mature process in SiC. There are several issues which include selective evaporation of Si and C from the substrate surface during high-temperature annealing, which limits the maximum annealing temperature [14]. In addition this makes it difficult to restore the lattice quality back to the virgin (i.e., pre-implanted) level, especially if the degree of lattice damage is near the level where the material becomes amorphous. Many research works have been performed to overcome these critical problems and some of them are listed in the following section. This is intended to give a brief background for the work conducted during this doctoral research, namely the annealing of SiC ion-implanted layers in a silane ambient.

1.3 Background

The most popular and conventional method of SiC post-implant annealing is thermal annealing performed in an argon ambient at either atmospheric pressure or in
vacuum [15 - 17]. A slightly modified version of this method is the use of a SiC wafer cap that provides a silicon overpressure above the wafer and was adapted by M. A. Capano, *et al.* [14]. They performed annealing on boron (B) implanted 4H-SiC and B and Al implanted 6H-SiC with a SiC cap, which was another SiC wafer placed onto the surface of the wafer to be annealed. The implanted samples were annealed in a resistively heated furnace at various temperatures between 1500°C to 1800°C. Two sets of anneals were performed during these experiments. In one set the samples were annealed for 40 min in an Ar ambient at 5 Torr. The second set of anneals were performed with the cap separated from the implanted wafer by a distance of 250 μm. In this technique a SiC wafer is clamped to the implanted wafer so that Si surface out-diffusion is suppressed by the cap wafer. The surface of the annealed samples was characterized via atomic force microscopy (AFM). Electrical characterization was done by performing C-V measurements of schottky diodes formed by patterning Ni on to the implanted surface, and the contact resistance determined using transfer length method (TLM) measurements. It was observed that temperatures in excess of 1650°C were required to reach high activation levels for boron implants in 4H-SiC with complete activation achieved at 1750°C. The sheet resistances of the Al-implanted 6H-SiC samples that were annealed at 1800°C were measured to be 32.2kΩ/□. However there was an increase in the surface roughness after implant annealing of the samples in the Ar ambient. According to a model that was proposed in that work to explain the observed surface roughness, SiC sublimation and highly mobile species enable the surface to reconfigure itself. Saddow *et al.* [28] proposed that anneals performed in an ambient that prevents the evaporation of Si
containing molecules would suppress the mechanism which leads to step bunching and hence surface morphology degradation of the post-implanted annealed surface.

Similarly D. Kawase et al. investigated Si re-growth from the amorphous phase caused by Al-implantation [18]. Implantations were performed both at room temperature and at 1000°C. The samples were annealed in Ar for 30 min at temperatures between 800°C to 1600°C in order to re-crystallize the amorphous layer. The damage induced by the implantation and the damage reductions by the subsequent annealing were determined by electron spin resonance (ESR) and transmission electron microscopy (TEM). The ESR signal from the as implanted sample showed presence of dangling bonds which corresponds to amorphous SiC. The spin density of ESR increased with the fluence and decreased with the implantation temperature and annealing temperature indicating the re-crystallization of amorphous regions. However, electric properties (carrier concentration and mobility) were independent of the implantation temperature and D. Kawase et al. observed that residual defects appeared in the implanted regions after annealing.

K. A. Jones et al. used an AlN capping layer to prevent Si evaporation during activation of n-type dopants up to a temperature of 1600°C [19]. After annealing the AlN cap is stripped off. Of more concern was that pinholes in the AlN cap were observed to form, especially at temperatures above 1600°C, thus limiting the utility of this approach. This is especially true in the case of complete activation of p-type dopants, which require annealing temperatures above 1700°C. L. B. Ruppalt et al., proposed a dual BN/AlN capping layer for performing annealing on implanted SiC up to a temperature of at least 1700°C [20]. The AlN was used as a protective layer on SiC as it is chemically inert, while the BN layer on top of the AlN cap would prevent the AlN from evaporating at
temperatures in excess of 1600ºC. Both the layers were deposited by pulsed laser deposition (PLD). After performing high temperature annealing, the BN layer cap was removed by ion milling and the AlN was selectively etched with a warm KOH etch. The surface structure after etching off the cap layers was examined with scanning electron microscopy (SEM), X-Ray diffraction (XRD), atomic force microscopy (AFM) and High Resolution Transmission Electron Microscopy (HRTEM). It was observed that the surface of the film remained unchanged and there were no cracks or hexagonal thermal pits that had been observed when only AlN cap layer was used due to the exposed AlN. An Auger electron spectroscopy (AES) analysis of the surface showed no evidence of Al or N contamination. However, the processing steps involved using this method are daunting for production. First, large-area cap deposition using PLD is difficult as the deposition footprint is normally limited to a few centimeters in diameter. Second the two-step process to remove the dual-level cap is both time consuming and can lead to processing errors, such as ion-milling through the BN cap into the AlN cap or, worse, through both caps and into the underlying SiC surface.

K. V. Vassilevski, *et al.* developed a process similar to the one described in [19] and [20], but instead of AlN, graphite capping layer was used to protect the surface during post-implantation annealing [21]. Photoresist AZ-5214E, which is a special kind of resist that can be used as both positive and negative resist, was spun and baked in vacuum at temperatures ranging from 750 to 850ºC. This helps in formation of a graphite layer. Complete conversion of the polymer into a graphite layer was verified by Raman spectroscopy. After formation of the graphite layer, post-implantation annealing was performed at atmospheric pressure in an argon ambient for 30 mins at temperatures up to
1650°C. The capping layer was subsequently removed by dry oxidation followed by etching of the film in an HF:HNO₃ (1:3) solution. Surface characterization was performed using AFM, which showed no step bunching with a surface roughness of ~0.4 nm. The Schottky diodes fabricated on the capped epitaxial layer on the unimplanted regions showed ideal diode behavior. The electrical characterization of the implanted layer was not mentioned in the paper. Again, this process, like the BN/AlN cap, is very tedious and liable to several contamination issues because of the photoresist.

C. Dutto *et al.*, performed laser annealing (LA) as an alternative to the classical thermal annealing processes for activation of ion-implanted dopants in SiC [22]. They used powerful pulsed-excimer laser beams of nanosecond temporal duration to deposit large amounts of energy in a short period of time into the near-surface region, while maintaining the substrate essentially at room temperature. They demonstrated the possibility of annealing Al implant-induced damage in 4H-SiC by single-shot laser processing in the solid phase using a XeCl excimer source of 200 ns pulse duration. The surface study revealed that this process kept the surface stoichiometry (Si:C) near unity and prevented any strong surface degradation. The electrical activation of the Al dopant was confirmed by I-V measurements, which were performed on mesa *pn* junction diodes. Unfortunately, they did not report on the dopant activation percentage so it is difficult to assess the usefulness of this technique. In addition, while laser annealing is an attractive research approach, for high-volume device production the suitability of this approach is in doubt.

Several other types of annealing processes have been used, such as furnace annealing and rapid thermal annealing (RTA). Furnace annealing is reasonable for a
temperature below 1800°C because of the Si sublimation and carbonization of the SiC surface [23]. In RTA processing, as the temperature uniformity across the wafer is excellent, there is a reduction in the thermal gradient that can warp wafers. However, for temperatures in excess of 1400°C using an RTA process has proven to be problematic due to the out diffusion of Si from the SiC surface, which can cause step bunching [24]. It also was noticed that the surface roughness increased with the annealing time and temperature [25]. There was yet another technique in which a thermally grown silicon dioxide was used as a capping layer [26, 27]. However this process is very sensitive to the thickness of the oxide and the annealing temperature is limited by the melting point or cracking of SiO₂.

Most of the annealing techniques mentioned in this section showed limited success and/or are very tedious to perform. Saddow et al. [28] and S. Rao [29] et al. used silane over-pressure process to achieve this very goal. The concept of silane overpressure is similar to arsenic overpressure implemented in post-implantation annealing of implanted GaAs [30, 31]. In order to avoid preferential evaporation of As from the surface, arsenic overpressure was provided in either a hot-wall furnace or using RTA with a proximity cap. In case of the hot-wall furnace, annealing was performed in a As gas containing ambient. In case of RTA, the sample was placed in close proximity with another GaAs wafer, which acted as a source of As. For both cases As vapor pressure was provided above the surface of the process wafer and thus suppressing further decomposition of the surface of the implanted sample. A similar technique was used for post-implantation annealing of GaN, where some form on nitrogen overpressure was provided to minimize the loss of nitrogen from the semiconductor surface at high
temperature [32]. Based on these processes, silane overpressure was implemented in order to suppresses the selective evaporation of the Si from the SiC surface. This process, which will be discussed in more detail in following chapters, can be easily adapted by the SiC community since most SiC fabrication suites contain a high-temperature SiC CVD reactor which can be easily adapted for this process.

1.4 Organization of this Document

This dissertation will report on the importance of ion implantation and post implantation annealing in SiC. The research work done in this dissertation is divided into three main chapters. Chapter two will explain briefly about the general theory behind implantation and then go on to explain the different methods of implantation in SiC. This chapter will also explain the theory along with a thermodynamic simulation of the silane overpressure process for post-implantation annealing. Chapter three and four will discuss in detail the implant annealing processes developed here along with surface and electrical characterization of the samples annealed in cold-wall and hot-wall CVD configurations, respectively. Chapter five will summarize the work in this research and as well as discussing future work in this field.
CHAPTER 2
ION IMPLANTATION AND IMPLANT ANNEALING

As mentioned in Chapter 1, SiC is a promising wide bandgap semiconductor, whose properties are suitable for many applications, such as high power, high temperature and high frequency devices. However, there are several issues with the processing technology that need to be resolved to enable industrial-scale SiC device production. One of the most crucial processing steps is planar doping of SiC, especially for planar device fabrication. Controlled doping of bulk crystals and epitaxial layers can be performed in-situ during growth with help of chemical vapor deposition (CVD) [33]. However, to fabricate planar devices selective area doping is required. In SiC, thermal diffusion is not a viable process because of the extremely high temperatures (> 2000°C), normally required. Along with the thermal stability of SiC at such high temperatures there is also an issue regarding low atomic mobilities in SiC [1, 34]. To reach reasonable diffusivities (≥10\(^{-13}\) cm\(^2\)/s) temperatures around or in excess of ~1800°C are needed for most elements [6]. Only light elements with a small atomic radius, like hydrogen, lithium, beryllium and boron, exhibit a significant diffusion under equilibrium conditions at temperatures below 1800°C. Hence, ion implantation appears to be both attractive and the only practical method to realize a selective, planar area doping technology for SiC [35].
2.1 Overview on Ion Implantation

Ion implantation is a process in which high velocity ions of the element to be implanted are injected into the near-surface region of the target material [36]. The major advantage of implantation is that the surface concentration is not limited by the species solid solubility as ion-implantation is a non-equilibrium doping technique and all stable elements of the periodic table can be implanted. It also gives precise control over the dopant concentration and depth profiles. A wide range of profiles can be obtained such as shallow junctions, buried doped regions, box profiles, etc. Regions can be selectively doped by using implant masks that block the ions from penetrating into the surface.

2.1.1 Ion Implanter

An ion implantation system typically consists of a high-voltage particle accelerator that produces a high velocity beam of ions which strike the surface of the target material which is to be implanted. Figure 2.1 shows the basic schematic of an ion implanter from reference [37].

![Figure 2.1: Schematic of an ion implanter showing (1) ion source, (2) mass spectrometer, (3) ion electrostatic accelerator (4) beam scanning system and (5) end station, where the target is mounted [37]](image-url)
Most ion implanting systems are divided into five main components:

a. **Ion Source:** A high voltage is used to produce plasma of the desired ion impurities from either a feed gas or solid charge, which are the sources of the implant species. In the case of solid charges, material is heated and the resultant vapor used as the ion source, flows past a filament. These vapors, or the feed gas, are broken down into a variety of atomic and molecular species with the help of a plasma glow discharge, where they are ionized [38]. Only desired charged specie is selected, for example incase only the positive ions are required, beam of positive ion leaves the system through the exit, which is biased with a large negative potential with respect to the filament.

b. **Mass Spectrometer:** The beam now consists of variety of species, most of which are ionized. With the help of an analyzer magnet the desired impurity is separated from other species based on its mass. An analyzer magnet bends the beam through a right angle (magnetic field perpendicular to the beam velocity exists) and the desired specie is passed through an aperture slit to the main accelerator column.

c. **Accelerator:** The accelerator adds required energy based on the desired penetration depth, to the beam and accelerates the ions to their final (i.e. desired) velocity. The required maximum energy or voltage depends on the desired penetration depth of the ions into the target material. The accelerator column is typically several meters long and is maintained at high vacuum to avoid ion collisions during acceleration.

d. **Scanning System or Beam writing:** The ion beam may be rastered with the help of x- and y-axis deflection plates. This ensures uniform ion implantation across the target sample. In order to prevent neutral particles, which may have formed during acceleration, from hitting the target the beam is bent slightly.
e. **End Station:** Finally the target sample is mounted in a vacuum chamber, where the sample’s orientation and temperature are set [39]. Also precise control of the ion dose is done at the end station by placing the sample in a Faraday cup. The cup captures all of the charges that enter it and the ion current is directly measured by connecting an ammeter between the cup and electrical ground. The dose is calculated by integrating the current over time and dividing the resulting value by the sample area. This measurement is usually done before an experiment, since Faraday’s cup absorbs all the energy.

While a production-level ion implanter is very expensive; the flexibility and tight process control have overshadowed this disadvantage. As a consequence, ion implantation is currently the dominant tool used to selectively dope SiC.

### 2.1.2 Brief Theory on Ion Implantation

The theoretical background of ion implantation is based upon Bohr’s and Rutherford’s early work [40]. Rutherford first proposed that atoms consisted of a solid nucleus surrounded by a shell of orbiting electrons and Bohr based on the collision between particles and bound electrons, calculated the energy loss per path length for a heavy charged particle. This formed the basis of ion implantation and led to the theory that several different effects occur during the bombardment of solids with heavy charged particles that causes an energy loss [41]. As an ion enters the surface of a sample, it collides with atoms in the lattice and interacts with the electrons in the crystal. Inelastic collision with electrons (electronic stopping, $S_e$) and elastic nuclear collisions (nuclear stopping, $S_n$) play a significant role in the stopping of the particles. Each nuclear or electronic collision reduces the energy of the ion until it comes to rest within the target
The total stopping power, $S_{e,n}$ (cross-section for electronic and nuclear stopping), is thus defined as the energy loss per unit path length and can be calculated using equation 2.1

$$S_{e,n} = \left( \frac{dE}{dx} \right)_{\text{nuclear}} + \left( \frac{dE}{dx} \right)_{\text{electronic}}$$ (2.1)

Where $E$ is the beam energy at impact and $x$ is the distance the ion travels into the sample. From Figure 2.2(a) it can be seen that at lower energies nuclear stopping dominates, whereas at higher values the energy is transferred to the electrons of the target material [39].

Figure 2.2 (a): Plot of theoretical ion stopping power as a function of energy [39]. (b): Theoretical Gaussian distribution of the implanted ions in the target sample. The profile shows that the impurity is completely implanted into the wafer below the surface [37].

The energy range of ion implantation, or the ion interaction with the crystal is a statistical process that was first investigated by Lindhard, Scharff and Schiott (LSS) in
the early 60’s, called the LSS theory described in [42]. According to this theory, the ions have a Gaussian distribution function as shown in Figure 2.2(b) and mathematically described by equation (2.2):

\[
N(x) = N_p \exp \left( \frac{(x - R_p)^2}{2\Delta R_p^2} \right)
\]

(2.2)

where \(N_p\) is peak concentration, \(R_p\) is projected range, and \(\Delta R_p\) is straggle.

Due to the random nature of the collisions the total distance traveled, or range, and its projection on the direction parallel to the ion beam, called the projected range, \(R_p\), is the average distance an ion travels before it comes to stop. All of the parameters are random variables. The peak concentration \(N_p\) lies at \(x = R_p\) as shown in Figure 2.2 (b). The spread of the Gaussian distribution is given by the standard deviation, \(\Delta R_p\), which is also called the straggle. For practical purposes one can indirectly control the energy and the dose, or fluence, of the implantation by varying the ion beam voltages and currents. The dose, \(\Phi\), is defined as the area under the Gaussian distribution curve and is given by equation (2.3)

\[
\Phi = \sqrt{2\pi N_p \Delta R_p}
\]

(2.3)

Implant doses typically range from \(10^{10}\) cm\(^{-2}\) to \(10^{18}\) cm\(^{-2}\) [37].

Due to ion bombardment of the crystal surface, various defects can occur in the target material depending upon the energy, dose and mass of the implanted ion. Some of these defect formations are:

(a) **Channeling effect:** When implanting a single crystal material in which the atoms are regularly or symmetrically arranged, a space in the crystal exists at particular orientation. The ions can penetrate deeper into the crystal when the ion velocity is
parallel to these crystal orientations [38]. This is called ion channeling where ions do not suffer any nuclear collisions and thus penetrate deeper into the crystal [41]. Channeling can be avoided by tilting the target sample so that the ion entering the crystal lattice makes an angle less than a critical angle. The critical angle is the largest angle, $\psi$, whereby the “steering” action of the rows of atoms is lost. $\psi$ is given by equation (2.4) as

$$\psi = 9.73 \sqrt{\frac{Z_1 Z_2}{Ed}} \quad (2.4)$$

where $E$ is the incident energy in keV, $d$ is the distance between atoms and $Z$ is the charge number for the incident and target ions. The tilt angle of the sample with respect to the incident ion beam thus depends upon the lattice structure and crystal orientation.

(b) Amorphous layer formation: In the case of a sufficiently high ion dose, the damage due to displacement of target atoms by the implanted ion is very high [36]. The displaced atom can themselves displace other atoms, resulting in collision cascade effect. This leads to the accumulation of vacancies and atomic clustering effects and hence the formation of an amorphous layer. Amorphous layer formation can be reduced to a certain extent by heating the sample to a high temperature during implantation. At high temperatures, the substrate surface thermally “self-anneals”, but not completely. In order to re-crystallize the target surface, a post implantation anneal is performed at an even higher temperature, which is the basis of this research and is explained in the section 2.3.

Often a thin passivation layer is deposited or grown on the sample surface to protect the bare surface from contamination as well as to reduce the damage caused by the high energy ions. In the case of a single ion implant, the passivation layer also helps in placing the peak of the implanted Gaussian profile or to maximize the dopant
concentration, at the sample surface. This is particularly important to minimize the contact resistance of metal contacts applied to the implanted region. In the case of shallow junctions, to reduce the sheet resistance and short channel effect, especially in MOSFETs, multiple implantations are performed to obtain an implanted box-profile [43]. Figure 2.3 shows a typical box-shaped profile for a sequence if nitrogen implants into a SiC surface to form source and drain wells in a MOSFET [4].

![Figure 2.3](image)

Figure 2.3: A typical calculated implantation profile for a sequence of nitrogen implants in SiC to generate a box-shaped profile in order to form drain and source wells in a MOSFET [4].

2.1.3 Ion Simulation Tools: SRIM and TRIM

For a given ion energy and fluence it is possible to accurately model the distribution of the dopant ions in the substrate, which makes it convenient to determine the ion profile and concentration before hand. The most widely used software tool to predict the energy and depth of the implant profile is the Stopping and Range of Ions in
Solids (SRIM). SRIM is a group of programs which calculate the stopping and range of ions into matter using a full quantum mechanical treatment of ion-atom collisions [44]. During the collisions, the ion and atom have a screened Coulomb collision, including exchange and correlation interactions between the overlapping electron shells. The ion has long range interactions creating electron excitations and plasmons within the target. These are described by including a description of the target's collective electronic structure and interatomic bond structure when the calculation is setup (tables of nominal values are supplied). The charge state of the ion within the target is described using the concept of effective charge, which includes a velocity dependent charge state and long range screening due to the collective electron sea of the target. A detailed explanation of the calculation and the mechanism used for making the simulation tool can be found elsewhere [45].

One of the comprehensive programs included in SRIM is a Monte Carlo statistical analysis program called TRIM (Transport of Ions in Matter). TRIM accepts complex targets made of compound materials with up to eight layers, each of different materials. It calculates both the final 3D distribution of the ions and also all kinetic phenomena associated with the ion's energy loss: target damage, sputtering, ionization, and phonon production [44]. It was developed to determine ion range and damage distributions as well as angular and energy distributions of the backscattered and transmitted ions [41]. In this program the history of an individual ion or particle in the target is simulated. The particle is assumed to change directions as a result of binary nuclear collisions and move in straight free-flight paths between collisions. After a series of nuclear and electronic collisions the energy of the particle is reduced. The ion history is terminated if the
particle looses its energy and comes to a complete stop in the target or if the ion misses
the target sample completely. In this calculation, it is assumed that the target is
amorphous and hence the directional properties of the crystal lattice are ignored. Also the
nuclear and the electronic energy losses are assumed to be independent. As mentioned in
the previous section at lower energy nuclear stopping dominates, hence the program
utilized this mechanism.

SRIM was originally developed by J. P. Biersack and now is owned by IBM. It
can be run on a personal computer with either the DOS or Windows operating system. In
this research work this tool was used to predict the doping profile of the implanted layer
and also to compare these results with the ion implant profiles measured with Secondary
Ion Mass Spectrometry (SIMS).

2.2 Ion Implantation in SiC

Since SiC consists of the group IV elements Si and C that have four electrons in
the outer shell, SiC can be doped with the same elements that are used for Si. Group III
elements, such as aluminum and boron, are most commonly used for p-type doping,
while nitrogen and phosphorus are normally used for n-type doping [46]. Implantation
and activation of p-type dopant species results in the highest level of damage to the
crystal For this reasons and several others that are given in the next paragraph, the focus
of this research work is on p-type dopant activation.

Aluminum or boron are found to reside on silicon lattice sites and act as acceptors
in SiC [47 - 49]. The ionization energies for aluminum and boron in 4H-SiC are 191 to
230 meV and 285 to 390 meV, respectively [6, 49]. The ionization energies of aluminum
and boron acceptors decrease with increasing acceptor concentration or increasing compensation [50]. This might be reason for the wide range of published data for the ionization energies. Due to the crystal symmetry of 4H-SiC, there are two equivalent lattice sites (cubic and hexagonal) which result in two dopant energy levels in the crystal.

Boron is a lighter atom compared to aluminum thus the projected range of boron is a factor of 2 times deeper than aluminum, when implanted with the same energy [5]. In addition, boron causes less damage to the crystal lattice due to its size and mass. This property is an advantage if deep implantations are required, e.g. to form edge termination of diodes. However the based on the smaller value of ionization energies mentioned above, degree of ionization of aluminum is higher than that of boron and also the solubility of Al in SiC exceeds that of boron [49]. Therefore for high doping it is preferential to use aluminum. Also it has been observed that boron implanted in SiC results in deep level defects called the D-center defect, which is speculated to be one of several intrinsic defect complexes consisting of one boron atom [10]. During post-implant annealing at high temperatures, boron tends to diffuse easily and either out diffuses (i.e. leaves the crystal) or accumulates at the surface [50]. In this research the surface of 4H-SiC, which was implanted with aluminum, was studied.

In SiC in order to avoid ion channeling various implantation procedure are followed. Two of the most popular methods of implantation are listed here.

2.2.1 Random Implants

The implantation process is said to be “random” when the direction of the ion beam with respect to the crystal is such that the high energy ions experience the same
amount of energy loss and collisions as they would in a material with the same chemical composition but of amorphous structure [6]. In spite of this, there is always a probability that a few of these high energy ions scatter along major axial or planar directions, leading to channeled trajectories. In the case of SiC random implantation can be even more complicated because of the poor knowledge about ion channeling phenomena in the different SiC polytypes and also due to various different SiC crystal orientations with respect to the wafer primary flat. The primary flat is the longest length in the circumference of the wafer and has a specific crystallographic orientation relative to the wafer surface. The most general convention to identify the proper implantation geometry for random implants is to set tilt and twist angles with respect to the wafer normal and the wafer primary flat. The tilt angle corresponds to a rotation of the wafer normal with respect to the ion beam direction within the plane of the wafer flat as shown in Figure 2.4. The twist angle is the angle by which the wafer is rotated around the wafer normal while remaining within its own plane.

![Diagram of wafer orientation](image)

Figure 2.4: Sketch of the wafer orientation with respect to the ion beam in order to perform random implant. $T_w$ is wafer twist, $T_t$ is the tilt angle and $O_x$ is the off-axis of the wafer.
It is very hard to achieve accurate random implantation in SiC. Since the wafers are misoriented with respect to the (0001) plane to improve epitaxial deposition. For 4H-SiC the off-angle value is approximately 8°, which again is not accurate. Because of all these issues of inaccuracy, the usual convention to fix tilt and twist angles with respect to the wafer normal and the wafer flat does not guarantee the desired control and reproducibility of the implantation geometry. The relative orientation between ion beam and SiC crystals often does not minimize the probability of channeled implants. This explains the large spread of the published data regarding the shape and implant depth profile, particularly the tail of the implants.

2.2.2 Channeled (Aligned) Implants

When performing channeled implants the ion beam is used in the single spot configuration, which leads to a non-homogeneous flux distribution within the beam cross-section. The channeled profile is deeper than the random implantation profile and has a trapezoidal shape while, random profile is more Gaussian as shown in Figure 2.5. In Figure 2.5, profiles correspond to 1.5 MeV Al⁺ implants performed at room temperature with a low fluence of \( \sim 10^{13} \text{ cm}^{-2} \).
Figure 2.5: SIMS profiles for random and $<0001>$ channeled implant doping profiles in 6H-SiC for a low fluence values. Note that for comparable implants the channeled implant in much deeper and wider [51].

The differences between random and channeled implants are because channeled ions experience lower electronic loss and less nuclear collisions than the random ions. Nuclear collisions are responsible for the atom displacements that produce build up of disorder in the crystal surface. As the damage increases the material becomes more amorphous and/or contains more defects. Strong dechanneling occurs when the ions reach the buried damaged layer formed by a previous implant, since this layer contains more defects than the sub-surface regions. Thus the number of de-channeled ions in channeled implants increases and the doping profiles modify accordingly. The deepest edge of the channeled profile saturates with increasing ion fluence, and the profile shape starts resembling that of random implants or Gaussian profile as shown in Figure 2.6
Figure 2.6: SIMS doping profile for \(<0001>\) channeled implant in 6H-SiC, showing the effect of the implantation dose on the depth profile. As multiple channeled implantations are performed, the intermediate peak grows, due to accumulation of defects between 1 and 4 \(\mu m\) [52].

Another set of experiments were also performed to study channeled implants in 4H-SiC at two different orientations [53]. A 60 keV \(Al^+\) implantation was performed in (0001) with an off-axis miscut towards [11-20] and (11-20) oriented 4H-SiC wafers. For the (0001) wafers, tilting the wafer during implantation, along the (1-100) plane did not result in significant channeling in contrast to tilting along the (11-20) plane. But in case of (11-20) wafers, 10° tilt along various planes around the main crystallographic axis resulted in the largest degree of channeling along the (0001) plane with no channeling observed for the implant in the (1-100) plane. Therefore depending upon the orientation and the direction of the implantation channeling can be minimized.
There are however major technological difficulties with channeled implant method. The wafer has to be properly aligned. Rutherford backscattering spectroscopy (RBS) has to be performed on the sample in order to find the proper orientation of the sample. RBS is an in situ process and is performed before the implantation. In RBS measurements the material has to be irradiated with helium ions and the distribution if the backscattered helium ions are detected. The channeled orientation is found by minimizing the backscattering yield. RBS has to be carried out as fast as possible in order to minimize the damage created by the helium ion irradiation.

Based on all the complication involved with the channel implantation, in this research random implants were performed on the samples used for annealing experiments. Most of the aluminum implantation was performed by the group of Dr Nipoti at Consiglio Nazionale delle Ricerche (CNR, National research council), Istituto per la Microelettronica e Microsistemi (IMM Institute for Microelectronics and Microsensors), Bologna, on Tandetron 4117 HC implanter. The 1.7 MV Tandetron accelerator system mainly consists of ion sources a, magnetic mass analyzer, a high voltage power supply, ion beam tubes, a switching magnet, an end station and a computer control system. The high-voltage power supply system is a Cockroft-Walton type (model 4117-HC). The terminal voltage range for this system is from 0.1 to 1.7 MV. The accelerator system is controlled by a computer which allows for unattended start-up and operation of the accelerator system. The data transmission between the accelerator and the computer is done by a fiber optic cable to reduce electro-magnetic noise and potential sparking damage.
The implantation performed was a random implant described in section 2.2.1, in which the ion beam impinges on the 4H-SiC crystal at 15° with respect to the (0001) axis while remaining within a plane at 12° from the \{11-20\} crystal plane. In order to reduce the amount of damage accumulation or defects, the implantation were performed at a temperature higher than room temperature (typically ~ 400°C). The details about the implantations performed are mentioned in chapters 3 and 4 along with the post-implant anneals that were performed on implanted samples.

### 2.3 Importance of Post-Implant Annealing

In addition to ion implantation performed at elevated temperatures, thermal annealing is normally performed after ion implantation, which serves the dual purpose of repairing defects and activating dopants. Although a considerable part of the implantation-induced damage can be removed by annealing at 1200°C, to achieve reasonable electrical activation annealing at temperatures in excess of 1500°C should be performed because of the high bonding strength of the SiC lattice [54]. After bombarding the target surface with ions, the implanted ions predominantly occupy interstitial lattice sites [12]. These interstitial atoms do not affect the electrical properties and, in addition, these high energy ions damage the crystal lattice. The electrical activation of the implanted ions, via, the incorporation of dopants on to proper lattice sites known more formally as substitutional dopant incorporation, is performed by thermal annealing of the wafer.

It has been observed that at such elevated temperatures (>1500°C) the SiC surface degrades when annealed in inert gas (argon) as well as in vacuum. Silicon appears to
preferentially evaporate and a carbon-rich layer is left behind on the surface [55]. Hence a technique needs to be implemented to permit high temperature annealing of SiC implants which would allow for dopant activation while suppressing the evaporation of Si from the surface. Low resistance ohmic contacts are dependent on highly doped surface layers and good carrier mobility, which in turn is dependent on the anneal temperature and anneal time. The higher the annealing temperature the greater the degree of dopant activation. However, higher annealing temperatures also cause extended defects, dislocation loops, etc to appear which are similar to the end-of-range defects seen in implanted and annealed Si. This imposes further limits on the annealing temperature/time window that can be used in processing of ion implanted SiC [6].

As discussed in Chapter 1, various annealing techniques have been performed by the SiC research groups, mostly with limited success. Some results obtained showed promising results, but many of the processes are complicated and tedious to perform. In this research we have tried to implement a process we call the silane overpressure process, which is inherently simple and can be easily adapted by the SiC community. In the next section the theory behind this process is explained in detail and the process details implemented during actual implant annealing experiments are described in chapter 2 and 3.

### 2.4 Silane Overpressure Model

The most popular method of post-implant annealing of SiC is thermal annealing in an argon ambient [18]. As shown in Figure 2.7 (a) when a sample is heated to a high temperature, Si preferentially evaporates from the sample surface, leaving behind Si
voids. This leads to the so called step-bunching phenomena of the surface in addition to leaving a carbon-rich surface.

In the case of silane over pressure method, the basic principle is described as follows. When the SiC wafer is annealed at high temperatures (≥ 1600°C), Si atoms on the surface of the SiC wafer may be exchanged with Si atoms provided by the cracking of the silane gas in the vapor phase. This model is based on the hypothesis that if the partial pressure of Si atoms above the SiC surface during annealing is greater than the vapor pressure of Si in the SiC matrix, then the evaporation of Si from the surface can be suppressed, as shown in Figure 2.7 (b). The silane is introduced via an argon carrier gas, since argon is an inert gas and does not etch or dope SiC. Initial work done by Saddow et. al. used hydrogen as the carrier gas, but this lead to etching and was hence abandoned [28].

![Diagram](image)

Figure 2.7: A cartoon of the proposed mechanisms that can occur during post-implantation annealing of SiC in (a) an argon ambient. and (b) a silane/Ar ambient, which is the focus of this research.

In this research work post-implantation annealing process was developed for both cold-wall (Chapter 3) and hot-wall (Chapter 4) configurations, which are explained in
detail in the following two chapters. Initial thermodynamic calculations for both hot-wall and cold-wall, were performed based on the experimental flow rates, especially for the carrier gas argon. Thermodynamic calculations were performed for silane flow rates as a function of temperature to study the silane overpressure mechanism in order to be able to predict the required silane flow as a function of process pressure and temperature. These calculations were performed using the NASA-Glenn Chemical Equilibrium Program CEA2 [56]. Details about this software can be found in NASA publications [57, 58]. This software contains a graphical user interface (GUI) and can also be run using FORTRAN. With this software the chemical equilibrium compositions for assigned thermodynamic species can be predicted. These states are specified by assigning two thermodynamic state functions which, in our case, are temperature and pressure. The CEA program uses a minimization of free energy formulation, since each species can be treated independently without specifying a set of reactions. Gibbs free energies of formation is given by equation 2.5

\[ \Delta G_f^0 = \Delta H_f^0 - T \Delta S_f^0 \]  

(2.5)

where \( \Delta G_f^0 \) is the change in standard free energies (free energy of a reaction at 25°C and 1 atm pressure) when 1 mole of a substance is prepared from its constituent elements. \( \Delta H_f^0 \) is the change in standard enthalpy and \( \Delta S_f^0 \) is change in standard entropy of the closed system maintained at constant temperature and pressure. In order to characterize the thermodynamic state of the system, which is at constant pressure and temperature the Gibbs energy is most easily minimized since temperature and pressure are its natural variables. At equilibrium Gibbs free energy of a mixture of chemical species must be a
minimum. At equilibrium the total free energy of the mixture is the sum of all the chemical potentials of each species, weighed by the number moles of each specie as given by equation 2.6.

$$dG = \sum_{i=1}^{n} \mu_i dN_i = 0$$  \hspace{1cm} (2.6)

where $\mu_i$ is chemical potential, $N_i$ is number of moles of species anf $n$ is the total number of species in system.

In CEA program, equilibrium concentrations of species are calculated at specific temperatures and pressures. Once the thermodynamic states are established one can input the reactants and number of reactant moles into the calculation. Based on the reactants the program generates all possible known complex solid, liquid and gaseous species. Depending on the probability of occurrence of certain specie we can select or omit that particular specie for iteration purposes and this is saved as the input file with .inp extension. Details of the CEA input and output file are shown as Appendix A. This input file is then executed and the mole fractions for all the species that were included in the input file is obtained as an ASCII file with either .out or .plt extension.

The calculations were performed using typical process conditions such as process temperature and pressure, partial pressure of silane, an inert carrier gas (argon) and solid phase SiC (to take into consideration the substrate). The temperature, pressure and the carrier gas flow rate for the calculations were varied based on the reactor configuration and the experimental temperature values. Two set of calculations were performed for each anneal temperature. In the first calculation, solid phase SiC and gas phase argon were included as the reactants. This was done in order to obtain the theoretical value of
silicon in the vapor phase when SiC is heated in both an argon ambient and when silane in argon cracks over the crystal surface. Figure 2.8(a) shows the calculated vapor pressure in the reactor during annealing. Of the 20 or more species that were simulated for condensed SiC in an argon ambient, it was predicted that only Si$_2$C, Si and SiC$_2$ were present in the reactor during annealing. Thus the dominant species present in the gas phase over a solid SiC surface contains Si due to evaporation from the lattice.

Figure 2.8: Thermo-chemical predicted vapor pressure vs. temperature of SiC annealed in argon. All the dominant species out of ~ 30 predicted species by the simulation are shown. Note argon and condensed SiC are not shown in the plot since their values was much higher than the species shown.

In the silane overpressure model silicon, delivered via silane gas during annealing, must be of sufficient partial pressure to balance the partial pressure of silicon evaporating from the substrate. Therefore, in the next calculation only silane and argon
were incorporated into the calculations. A trial and error numerical iteration was performed with the help of Matlab to equate the silicon due to the cracking of silane with the silicon due to evaporation from the SiC substrate. A theoretical value of silane flow rate was thus obtained for both cold-wall and hot-wall CVD configurations. This numerical simulation process was repeated for all annealing temperatures in both configurations. However the assumption that the partial pressure of Si in the gas phase, \((PP)_{Si}\), must be equal to the vapor pressure of Si evaporating from the SiC substrate, \((VP)_{Si}\), is not correct. From the kinetic theory of ideal gases, the rate at which molecules hit surface of the substrate depends on the temperature, pressure, concentration of molecules and the thermal velocity and, hence, is a statistical process. Since the capture Si by the lattice to replace an evaporated Si atom is statistical in nature one can assume that more Si is needed to ensure this process occurs in a reasonable period of time. If we assume that the probability of capture is 10%, then \((PP)_{Si} = 10*(VP)_{Si}\). The predicted silane flow, based on this order magnitude higher partial pressure assumption, was used in these calculations and is plotted as a function of temperature in Figure 2.9 for both the cold- and hot-wall CVD configurations.
Figure 2.9: Predicted silane flow rates as a function of anneal temperatures for both cold-wall (circles) and hot-wall (triangles) CVD configurations. An exponential fit has been applied to the data to indicate the trend with temperature.

It can also be observed from the figures that the predicted flow rate of silane increases exponentially as the anneal temperature is increased, which is expected due to the exponential increase in Si vapor pressure as a function of temperature. In the following chapters these theoretical curves are compared with experimentally determined silane flow rates.

2.5 Summary

For selective doping of SiC in order to make planar devices, ion-implantation is the most feasible process. Two different methods of implantation in SiC have been explained in this chapter. Even though there has been significant progress made in both implantation processes, several issues have yet to be tackled. In addition to implantation
the importance of post-implant annealing is also mentioned. Implantation causes damage to the surface due to bombardment of ion. Thermal annealing has to be performed to both repair the crystal damage and electrically activate dopants. In this research work a silane-over pressure process has been established for this purpose. Thermodynamic calculations performed to predict the silane flow rate was presented in this chapter. The following two chapters will explain the actual processes in cold-wall and hot-wall CVD configurations.
CHAPTER 3

IMPLANT ANNEALING IN A COLD-WALL CVD REACTOR

Implant annealing normally is conducted in a high-temperature furnace that is capable of reaching temperatures of greater than 1600°C in the case of SiC. What is required for such a furnace is a high-purity housing, typically made from stainless steel or quartz, that limits the possibility of introducing impurities into the annealing environment. In this work implant annealing was conducted in a high-purity chemical vapor deposition (CVD) reactor since (a) it is capable of reaching temperatures in excess of 1700°C (cold-wall configuration, this chapter and 1800°C hot-wall configuration, chapter 4) and (b) the reactor uses silane gas as the silicon precursor for growth of SiC films. Indeed the second point is key to this research which is to use an overpressure of Si to suppress the evaporation of Si from the SiC lattice during high temperature annealing.

3.1 Chemical Vapor Deposition

Chemical Vapor Deposition (CVD) is a synthesis process in which the chemical constituents react in the vapor phase near or on a heated substrate to form a solid deposit [61]. It is a common method of choice for epitaxial growth, since epitaxial layers are the building blocks for use in various device applications. The basic idea of CVD is to flow precursors in a carrier gas through a heated reaction zone where the precursor diffuses to
the surface through a boundary layer and is adsorbed as reactants onto the substrate. At the substrate surface, after the deposition reaction takes place, gaseous by-products desorb and diffuse away from the surface through the boundary layer. The boundary layer is the region in which the flow is ideally laminar [61]. As shown in Figure 3.1, it starts almost at the front edge of the susceptor and increases in thickness until the flow is stabilized or the velocity gradient of the laminar flow decreases to zero. The deposition rate depends on the boundary layer thickness, which in turn depends on the pressure in the system. In the case of low process pressure the boundary layer is thin and the growth rate of the deposit is ideally controlled by surface-reaction kinetics [61]. (as a point of reference atmospheric pressure growth is ideally controlled by the diffusion of growth species through the boundary layer and is thus mass-transport limited [61]).

There are different types of CVD reactors based on their orientation, either horizontal or vertical, and based on the growth zone geometry, either cold-wall (where only the substrate is heated) or hot-wall (where both the substrate and hot zone walls are heated). In addition there are numerous other variations such as process pressure, the use of plasma chemistry to crack precursors, etc [62]. In this chapter the work related to implant annealing in a horizontal, cold-wall, low-pressure reactor is described starting with a description of the reactor used for this work.

Figure 3.1 shows the basic schematic of a growth zone for the horizontal-cold-wall reactor used in this work. Details pertaining to this reactor can be found in the master's thesis by M. Smith [63]. The susceptor is heated by a radio frequency (RF) generator which drives an induction coil that surrounds the reaction chamber as shown. In this configuration only the substrate, which is placed on the SiC coated graphite
susceptor, is heated. Therefore, ideally reactions take place on the substrate surface only although some deposit forms on the quartz cold-wall region.

Figure 3.1: Basic schematic of a horizontal-cold-wall CVD reactor growth zone. For reference a sketch of the boundary layer is shown. The susceptor sits on a quartz boat (not shown) to insulate it from the cold wall. The cooling water jacket is maintained at a temperature below the boiling point of water.

As mentioned above, a CVD reactor is typically used to grow a single-crystal semiconductor epitaxial layer on a substrate. This is the most critical and important step for fabricating various types of devices, especially in SiC, where doping control along with poly-type control and defect reduction must be obtained [5]. In general to epitaxially grow SiC, precursor gases such as silane and propane, which are the sources of silicon and carbon, are mixed in a carrier gas (typically hydrogen) and then injected into the reaction chamber. This is a technique popularly employed in the SiC field [6] and hence most of the SiC community is equipped with silane-based CVD reactors. Thus one of the motivations for this implant annealing research was the wide-spread applicability to the
SiC community. The cold-wall CVD reactor used in the research was built in-house at USF and a detailed explanation is given in the following section.

3.2 USF Cold-wall CVD Reactor

The reactor used for the implant annealing experiments during this research is shown in Figure 3.2. The cold-wall reactor was constructed using a 75mm inside diameter horizontal quartz tube, which could accommodate a susceptor that was designed to handle a maximum wafer size of two inch in diameter as shown in Figure 3.3. The overall length of the tube was 900 mm and was selected based upon practical heat transfer considerations and to ensure laminar flow in the growth zone [63].

Figure 3.2: Photograph of the 75 mm horizontal, cold-wall reactor. Gas inlet indicates the entrance of the gas into the reactor through a quarter-inch stainless steel gas line and exits out of the system through the 2-inch exhaust, as shown [64].
The front end of the quartz tube was clamped to the head plate via a quartz adapter and sealed with a Viton o-ring. The stainless-steel head plate was permanently clamped to the reactor housing. As shown in the picture above, the reactor was cooled with a water-cooled jacket. The graphite susceptor was supported by the ribs of a quartz boat, as shown, which was placed in the reactor in the center of the RF induction coil. The susceptor was heated by the RF generator via the induction coil, which was wrapped around the reaction tube. The graphite susceptor was coated with SiC to prevent contaminants present in the bare graphite from contaminating the growth chamber [65].

The temperature of the susceptor was measured by focusing an IR pyrometer at a circular indent in the back of the susceptor. A standard method for calibrating the temperature of the susceptor was by performing a Si-melt test. In this test, a piece of silicon was placed in the “sweet spot” of the hot zone (i.e., where the sample position during annealing and growth is) and the susceptor heated until the silicon melted, which is at 1410ºC under STP conditions. The pyrometer reading at the melt temperature was then recorded and the difference between the actual temperature (1410ºC) and the measured temperature, ΔT, noted. As shown in Figure 3.2, a mirror above the reactor was used to observe the silicon melt with the naked eye. ΔT was then used to determine the desired set point temperature used for all implant annealing experiments. The melt test was periodically repeated to ensure maximum temperature accuracy throughout this research.
Figure 3.3: Photograph of the SiC coated susceptor supported by ribs of a quartz boat.

The exhaust end of the tube was clamped to a quartz end cap, which also provided the transition from the reaction tube to the gas exhaust system. The exhaust system was connected to a dry pump via a pressure transducer and throttle valve. A programmable logic controller (PLC) and personal computer were designed and constructed to allow fail-safe safe operation of gases, reactor purging, gas metering, and temperature control [63]. Numerous sensors have been incorporated into the control system to ensure safe operation of the CVD reactor during processing. When the sensors are activated, the system shuts down all gases and the heating source, and Ar is purged through the reaction tube. The sensors for the control system include hydrogen and HCl gas sensors, a door sensor, and a cold water jacket flow sensor. The fault of any of these sensors results in immediate system shutdown as noted above. The details of the control system can be found in MS thesis from T. Schattner’s [66].

There were two basic modes of operation for the reactor system mentioned above; ‘purge’ mode and ‘process monitor’ mode. During reactor start-up the system is in purge mode and an initial vacuum test is first performed to ensure that there were no leaks in the system. This was done by pumping down the reactor to below 500 mTorr. The tube
was then brought back to atmospheric pressure by trickling a small flow of hydrogen into
the inlet (with the vent valve closed to prevent outside air from entering the system from
the exhaust port). Once the pressure reached near atmospheric pressure, the main
hydrogen purge was initiated which opens the vent valve and flows a high rate of
hydrogen through the reactor. This ensures positive pressure in the system so no air can
back fill the tube. After completion of the pump cycle, and to initiate the annealing
process schedule, the system is switched over to ‘process monitor’ mode. In this mode
the annealing process, which is explained in the following section, was performed. The
process was manually controlled by the operator with the help of the Labview™
computer interface [63]. This program enabled the operator to set desired gas flows and
the temperature set points required for the annealing process. Once the annealing process
was finished the system was brought into purge mode. In this mode, hydrogen was
purged through the reactor for 30 seconds, which purged the process gases from the
reactor. This was followed by a shut down of the RF generator under an Ar purge
resulting in a cool down of the sample for approximately 30 minutes.

The switches on the control panel open and close the valves for the various
process gases and mass flow controllers (MFC) regulate the gas flow. The flows were set
by the Labview™ program which also controls the RF generator power level. To operate
the system in low pressure; the pressure transducer was activated by opening the poppet
valve via a switch on the control panel. The transducer was connected to a pressure
controller, where the signal was compared to the set point pressure. The error signal is
received by the throttle valve, which then varies the angle of this butterfly valve to attain
the desired pressure. Details of this portion of the reactor system can be found in the MS thesis of M. Smith [63].

The gas handling system mixes the process gases in a gas manifold. A detailed layout of the overall system is given in reference [63]. The manifold allows for three basic functions: routing of process gases to the reaction tube, injection of purge gases to the reaction tube, and establishment of process gases to the vent. The vent side allowed the gases to be vented without having to flow them through the reaction tube, which allows the operator to establish steady-state gas flow prior to growth. In both purge and process monitor modes the venting of process gases is possible. But the routing of process gases to the reaction tube is enabled only when the system is in process monitor mode. This is done to avoid gas flow through the system when it was not properly configured.

A separate welded stainless steel line was used to connect each gas source to the gas manifold. Only the silane gas and hydrogen feeds had additional features incorporated. The silane source was connected to a separate purge system where Ar was used to purge the line to ensure that there was not any unwanted air in the line before or after silane flow was established. Also utmost care was taken to make sure proper start up and shut down procedures for handling silane gas. The silane line was purged with argon before the line was pressured with silane during the start up and vice-versa when the system was shutdown. In the case of the hydrogen source, hydrogen was fed through a palladium purifier, to purify the hydrogen above VLSI grade. Though this is of less relevance for implant annealing experiments, where argon is used as the carrier gas, nevertheless this again helps in the reduction of contaminants in the reactor prior to
annealing. A detailed explanation of the annealing process is given in the following section.

### 3.3 Post Implant Annealing Experiments

As mentioned in the previous chapter, high temperature annealing of ion implanted SiC samples must be performed to repair the crystal damage caused by the high intensity ion bombardment during implantation. Thermal annealing is needed to electrically activate the dopants by moving them from interstitial to substitutional lattice sites. It is well known that during high-temperature annealing of implanted SiC, Si atoms may evaporate from the wafer leading to a severe degradation of the surface called step bunching [67]. The silane overpressure model, which was explained in the previous chapter, is that this can be suppressed by the exchange of evaporating Si atoms with vapor phase Si supplied by the cracking of silane gas over the surface to be annealed. Earlier work presented by Saddow et al. discusses an implant annealing process under atmospheric pressure conditions in a similar cold-wall CVD system [68]. However, the formation of silicon droplets on the annealed surface was an issue. Based on the approach in this prior work, implant anneals were performed in a silane-based CVD reactor and carried out at low-pressure (around 150 Torr). This is because a shift in gas phase equilibrium occurs under low pressure, which helps to suppress Si cluster formation in the gas phase during sample annealing. Hence the probability of Si droplet formation should be reduced during implant annealing if the process is transferred to low-pressure process conditions.
3.3.1 Ion Implanted Samples

Two sets of wafers were used for this work. A 2”, high-purity, semi-insulating 4H-SiC wafer with an 8° miss-cut towards [11-20], designated W1, was implanted at Cree, Inc. with $^{27}\text{Al}^+$ at 650°C in dual doses of $2 \times 10^{13}$ cm$^{-2}$ at 200 keV and $4 \times 10^{13}$ cm$^{-2}$ at 360 keV. Implantation was performed through a thin 500Å passivating film of SiO$_2$. An SRIM simulation was performed to predict and to ensure a box profile for the doping profile. Secondary Ion Mass Spectrometry (SIMS) was also performed to monitor the actual profile of the implanted sample. SIMS for this particular sample was performed at Max Planck Institute, Stuttgart, Germany on a Time of Flight SIMS (TOF-SIMS) instrument. Figure 3.4 shows the doping profile predicted by SRIM and SIMS analysis done on the as-implanted sample.

![Figure 3.4: Comparison of doping profile vs depth predicted by SRIM and SIMS analysis done on the as-implanted sample.](image)

Figure 3.4: Comparison of doping profile vs depth predicted by SRIM and SIMS analysis done on the as-implanted sample.
The wafer was then diced into 8mm x 8mm samples and the samples cleaned in acetone and isopropanol and then RCA cleaned. All surface characterization reported in this research was performed on these samples (including hot-wall processing described in the next chapter). Since the implants were formed directly in the surface of a semi-insulating substrate, these samples were suitable for morphology study only and not for electrical activation assessment.

The second sets of samples implanted at CNR-IMM by Dr. Roberta Nipoti in Bologna, Italy, designated W2, were from a 4H-SiC (0001) Si-face Cree epitaxial wafer, with an 8° miss-cut towards the [11-20] direction. The doping concentration and thickness of the epilayer was $\sim 3 \times 10^{15}$ cm$^{-3}$ and $\sim 5$ μm, respectively. Aluminum was used as mask to protect the areas that were not supposed to be implanted. A 1.7 MV Tandetron accelerator was used to implant Al$^+$ into the unmasked regions. A thin oxide passivation layer was formed prior to implantation in order to place the peak of the implantation Gaussian profile at the surface of the sample. The implanted profile, as determined by SRIM, had a box shape with an ion concentration of $8 \times 10^{19}$ cm$^{-3}$ and an implant depth of 0.2 μm from an integrated dose of $1.75 \times 10^{15}$ cm$^{-2}$ as shown in Figure 3.5.
Figure 3.5: Predicted SRIM doping profile of the ion implantation performed on samples used for electrical characterization.

In spite of the high fluence value, the crystal damage was reduced because the implantation was done at the elevated temperature of 400°C. The implantation performed was a random implant in which the ion beam impinges on the 4H-SiC crystal at 15° with respect to the <0001> axis while remaining within a plane at 12° from the {11-20} crystal plane. After the implantation process the aluminum mask and passivating SiO₂ film were etched off from the sample surface. The wafer was then diced into pieces so that various sections of the wafer could be processed under differing annealing conditions. All electrical characterization for the cold-wall implant annealing process was performed on these samples.
3.3.2 Post Implantation Annealing Process

A silane based cold-wall CVD reactor described in the previous section was used for the work reported in this chapter. The samples were placed on a SiC-coated graphite susceptor as shown in Figure 3.6.

![Figure 3.6: Cross-sectional view of the graphite susceptor placed on the quartz boat. The sample was placed in the center of the two inch recessed groove as shown in the figure.](image)

The susceptor was heated up to the desired anneal temperature via an RF induction coil. In order to verify the silane overpressure process, preliminary annealing experiments called set 1 were performed to compare silane overpressure process with argon annealing process. These anneals were performed at 1600°C and 1650°C. After testing the process stability set 2 anneals at various temperatures from 1600 to 1700°C were performed at a process pressure of 150 Torr. The process schedule that was developed during this work is as shown in Figure 3.7.
Figure 3.7: Implant annealing process schedule for cold-wall CVD processing, indicating gas flow timing versus sample temperature. The silane flow indicated here is for the 1600°C annealing process and corresponds to 3% silane in 97% UHP Ar.

A 6 slm argon carrier gas flow was constantly flown in the reactor and the pressure maintained at 150 Torr until sample cool down. 3% silane premixed in ultra high purity (UHP) Ar was introduced into the reactor via an Ar carrier gas as shown in Figure 3.6, at a temperature of 1490°C, which is ~80°C above the Si melting point of 1410°C at standard temperature and pressure (STP). This was used to prevent the formation of Si droplets on the surface during the heating cycle. Depending on the desired anneal temperature, it took 6 to 8 min to reach the anneal set point temperature after turning on the RF source. Once the set-point temperature was reached a 30 min anneal was performed. To avoid Si droplet formation during cool down, the silane was turned off after 30 min of annealing and the temperature reduced to a surface temperature of
~1490°C. This was done to ensure that all silicon was purged from the reactor before cool
down to temperatures below 1410°C. After 1 min at this temperature the RF source was
turned off and the sample cooled in 5 slm of Ar flow until room temperature was reached.
The cool down time was approximately 45 min and determined by the annealing
temperature and Ar flow rate. The samples were then removed from the reactor and
surface characterization performed using SEM and AFM.

3.4 Experimental Results

In this section details concerning how the post implant annealing process was
characterized is given. The common problem with annealing SiC implants using other
methods is a degradation of the surface caused by the selective evaporation of Si from the
surface of the crystal. It was determined during this work that the most useful means to
characterize the annealing process was to first observe the surface under the optical
microscope to see if large defects, caused by the annealing process, were evident. Once a
sample appears to be smooth at this resolution, the sample was studied with Secondary
Electron Microscopy (SEM) and atomic force microscopy (AFM). AFM proved to be the
most useful technique since it can provide a quantitative measure of the surface
roughness. The experimental methodology used during this work was simply this –
anneal implanted samples in a silane ambient and observe for which flow rates the
resulting surface was smooth. Too little silane results in step-bunching, due to the high
evaporation rate of Si from the surface, and too much silane results in Si condensation on
the surface, which is easily observed as Si droplets. Details of this methodology are
provided after a discussion of the surface characterization methods used is completed.
3.4.1 Surface Characterization

The surface morphology of all annealed samples was studied with the help of optical microscopy, SEM and AFM. Most of the SEM images in this work were taken on a Hitachi 800 field emission SEM at USF. For all the SEM data collected, the sample was tilted away from the detector and slightly rotated. This was necessary because electronic scan lines from the SEM digital capture software made it hard to determine if step bunching was present on the surface, especially if the steps were aligned with the scan noise. More importantly the surface morphology was best revealed by tilting the sample away from the detector since this helps to reveal three-dimensional features compared with 90° incident plan-view micrographs. The AFM scans were performed on a Digital Instruments Nanoscope Dimension model 3000 AFM. It was operated in tapping mode which causes less damage to the cantilever tips. In the event that the cantilever scan direction completely coincides with the step bunching orientation, the scan image will be incorrect. Hence to ensure that the correct data on step bunched surfaces was obtained, scans were performed with the cantilever oscillating at two different angles (i.e., 0 and 90°). For all samples studied the AFM scans were performed on two-three different locations on the sample and an average RMS roughness noted to monitor any surface degradation caused by the high-temperature anneals.

As mentioned in section 3.3.2, for direct comparison between argon annealing and annealing with the silane overpressure process developed during this work, anneals were performed with both processes at 1600°C and 1650°C. Two samples with the same implantation profile were annealed in a J.I.P.ELEC™ annealing furnace at 1600°C and 1650°C for 30 min at a pressure of 1,000 Torr in a high purity Ar ambient. The surface
resulted in severe step-bunching as was evident from plan view SEM and AFM investigations. Figure 3.8 shows SEM and AFM data for the sample annealed in Ar at CNR-IMM at 1600°C. The RMS roughness was found to be 13.76nm.

Figure 3.8: J.I.P.ELEC™ furnace annealing performed at IMM in Bologna, at 1600°C for 30 min in high purity Ar: (a) Plan view SEM micrograph of the surface morphology. The step bunching on the sample surface is clearly evident. (b) AFM data of the surface morphology of the annealed surface had an RMS roughness of ~ 13.76 nm. The AFM scan area was 10 μm x 10 μm.

An identical implanted sample was annealed at 1600°C using the cold-wall CVD silane overpressure CVD process described here. No step bunching or any kind of surface morphology degradation was observed after annealing at this temperature. Figure 3.9 shows the SEM and AFM data after these silane overpressure anneals were performed. The RMS roughness of the surface obtained from AFM was 0.38 nm, compared to 13.76 nm in Ar.
Figure 3.9: Surface analysis after silane overpressure annealing at 1600°C for 30 min: (a) Plan view SEM micrograph of surface morphology at 5000x. (b) AFM data of the surface morphology. RMS roughness ~ 0.38 nm. The AFM scan area is 10 μm x 10 μm.

For the 1600°C process to produce a smooth surface, it was found empirically that 10 sccm of silane flow was required. The correct silane flow was determined by monitoring the surface with the SEM by ensuring that no step bunching or any surface morphology degradation was present after annealing at each temperature. Figure 3.10 illustrates the experimental methodology that was used for all of the research work reported in this dissertation. The surface morphology of samples annealed at 1650°C for various flow rates of silane are shown in this figure. SEM images of samples annealed with insufficient silane flow (10 sccm) had step bunching as shown in Figure 3.10 (a). When excessive silane flow was used (20 sccm) Si droplets were observed on the surface when viewed under the optical microscope (Figure 3.10 (c)). A smooth surface was obtained for an optimum flow of silane (15 sccm) as shown in Figure 3.10 (b). For each anneal conducted a similar set of data was taken and the annealing process for the smooth surface recorded along with its corresponding surface roughness as monitored via AFM.
Observed surface morphology of samples annealed at 1650°C for increasing silane flow values of (a) 10 sccm (step bunching) (b) 15 sccm (smooth, specular surface) and (c) 20 sccm (Si droplets). Data reported from this point forward corresponds to the process shown in image (b).

AFM analysis was then performed on the post-implant annealed samples to gather quantitative data and to make sure the SEM results were correct. A set of AFM data taken for each process temperature under optimized silane flow are shown in Figure 3.11 (minus the 1600°C data already shown in Fig. 3.9).

The AFM scan area was 10 μm x 10 μm. RMS values shown in Fig. 3.12.
The average RMS roughness obtained from the AFM scans was computed based on 3 surface scans per sample. The annealed surface showed an average RMS roughness of less than 0.69 nm (at 1700°C) indicating that the surface did not suffer any post-implantation annealing degradation. Figure 3.12 shows a plot of average RMS roughness vs. annealing temperature.

![Graph showing average RMS roughness vs. temperature after annealing in the cold-wall CVD configuration as measured with AFM. 10 μm x 10 μm scan size used for all data points.](image)

Figure 3.12: Plot of average RMS surface roughness vs. temperature after annealing in the cold-wall CVD configuration as measured with AFM. 10 μm x 10 μm scan size used for all data points.

As mentioned above, any further increase in the silane flow would normally result in Si droplet formation due to excess Si in the vapor phase. Occasionally these droplets were seen on the edges of the samples, most likely due to temperature gradients across the sample due to radiative cooling of the sample edge. Figure 3.13 shows an extreme example of such a situation. The SEM image shows that the droplet formation was mainly at the edges of the sample. A higher magnification image of a droplet is also shown for reference.
Si droplet formation, while reduced in occurrence under low pressure conditions, is one of the drawbacks of the cold-wall system. Also since it is believed that for maximum activation of Al dopants, it is better to anneal at temperatures up to 1800°C [67, 69] the maximum available power on the RF generator limited our cold-wall experiments to 1700°C. This limitation is due to the use of cold-wall reactor geometry and, hence, further implant annealing studies were conducted in a hot-wall CVD reactor, which is explained in detail in the next chapter.

3.4.2 Comparison with Theory

A plot of the experimentally determined silane flow rate, determined for different temperatures for the cold-wall CVD process, is shown in Figure 3.14. A comparison with
the theoretically computed silane flow rates (assuming \((PP)_{Si} = 10*(VP)_{Si}\)), as discussed in Chapter 2, is shown for comparison.

![Comparison of experimental and theoretical silane flow rates for the cold-wall CVD reactor configuration.](image)

Figure 3.14: Comparison of experimental and theoretical silane flow rates for the cold-wall CVD reactor configuration. An exponential curve fit was applied to the data and is also shown (lines in figure). Note the trend is exponential with increasing temperature.

Based on the data points shown in Figure 3.14, a exponential curve fit was applied to the data. The silane flow rate, \(\Phi\), expressed as an exponential function of the form

\[ y = ae^{bx} \]

for both the theoretical and experimental data is given as

\[ \Phi_{th} = 4.5 \times 10^{-14} \times e^{(1.9 \times 10^{-2} \times T)} \]

\[ \Phi_{exp} = 2.5 \times 10^{-6} \times e^{(9.5 \times 10^{-3} \times T)} \]

where \(\Phi_{th}\) is theoretical flow rate of silane and \(\Phi_{exp}\) is experimental flow rate of silane. As seen from the plot and equations, the assumption that the partial pressure of Si in the gas phase is an order magnitude higher than the Si vapor pressure is clearly not correct. There are several explanations for this large discrepancy, all of which will result in a larger flow
of silane being required to achieve the proper balance between Si partial pressure and Si vapor pressure. These are as follows:

a. **Reaction rate limitations:** The residence time of silane over the wafer is less than the time required for the reaction to occur, therefore incomplete cracking of Silane occurs.

b. **Mass transport limitations:** Si from cracked silane has to diffuse through the boundary layer in order to replace the evaporated Si. The time required for this to occur may be longer than the residence time of the silane over the wafer, thus resulting in less Si present at the wafer surface.

c. **Temperature gradients:** In cold-wall there is a large temperature gradient above the wafer surface, therefore only a small fraction of silane gas passing near the sample surface is cracked.

d. **The calculations assume thermodynamic equilibrium:** In order to compute the theoretical silane flow thermodynamic equilibrium was assumed. However, CVD is not an equilibrium process hence gross errors between experiment and theory are expected.

In order to explain the difference in the experimental and theoretical data and take into account all of the above possible mechanisms, a generic term called the cracking efficiency, $\eta$, was defined and is calculated as

$$\eta = \frac{\Phi_{th}}{\Phi_{exp}}$$  (3.3)
It was seen that cracking efficiency varied with temperature, with the cracking efficiency increasing with temperature, as expected. Further analysis and experiments are required to determine precisely what mechanisms are responsible for the observed discrepancy which is beyond the scope of this current research.

### 3.5 Electrical Characterization

Electrical device processing and characterization of the annealed samples were conducted at CNR-IMM under the direction of Dr. Roberta Nipoti by Dr. Fabio Bergamini [72]. As mentioned in the previous section electrical characterization was performed on the samples designated as W2. Before implantation, an Al mask was put down on top of a passivating oxide layer. Photolithography was used to pattern the Al mask to mask the region that was not to be implanted. The mask layout used for this process is shown in Figure 3.15 (a). After implantation and removal of the Al/SiO₂ mask, the samples were cleaned and then annealed with the silane overpressure process described already. Figure 3.15 (b) shows an SEM image of one of the patterned surfaces after annealing. Before the formation of the metal contacts on the W2 samples was performed, reactive ion etching (RIE) was used to remove ~40 nm from the wafer surface. The purpose of this etching step was to prepare the surface for better ohmic contact and to set the peak of the implantation profile at the surface. Contacts to form circular 150 μm and 350 μm diameter diodes, 400 μm square Van der Pauw (VdP) devices and Transmission Line Measurements (TLM) structures were defined by wet etching of a 420 nm thick sputtered Titanium/Aluminum (Ti/Al) film. A backside contact
was formed by evaporating 300 nm of Ni. Thermal annealing of both contacts was
carried out during the same process at 1000°C for 2 min in vacuum.

Figure 3.15: (a) Photolithographic mask layout of the device geometry used to form
electrical devices for characterization of the annealing process. (b) SEM micrograph of
etched mesa on the W2 surface after annealing and prior to metallization.

Current-voltage (I-V) measurements were performed at IMM Bologna on p⁺/n
diodes and Van der Paw (VdP) devices at 28°C using a computer controlled parametric
characterization system. The characterization unit was equipped with a Micromanipulator
MM6620 semiautomatic probe station, a Temptronic TP315B hot chuck, a Keithley
K707 switching matrix (equipped with 7072 and 7174 semiconductor cards) and a
Keithley K90 I-V measuring system, composed of a Keithley K2361 synchronism
controller and four Keithley K238 source measure units. Two sets of electrical
characterization were performed. First preliminary characterization was performed on
samples annealed at 1600°C and 1650°C (Set 1). For both of these anneals the silane flow
was held constant at 10 sccm. As mentioned in section 3.2.2 this was done to test the
process stability over a small (50°C) temperature range and it was expected that slight step bunching would be observed at the higher annealing temperature due to the increased vapor pressure of Si in the SiC lattice. However, the second set (Set 2) of electrical characterization was performed for a temperature range of 1600°C – 1700°C, where the silane flow was increased with increasing temperature so as to eliminate step-bunching as described earlier. The measured devices were homogeneously distributed on the sample surface.

Typical forward bias J-V characteristic curves for 350 μm diameter diodes on set 1 sample, annealed at 1600 C are as shown in Figure 3.16.

![Forward J-V characteristic curves](image)

Figure 3.16: Electrical characterization data taken on p⁺-n implanted diodes. Forward IV data shown from typical F1 (no excess current bump) and F2 (excess current bump) 350 μm diodes. F1 devices displayed a turn-on voltage of 1.75V with an ideality factor of less than 1.2.

Two significantly different trends on the forward J-V characteristics were observed. One trend, labeled F1, corresponds to a family of diodes with very weak generation-
recombination current and an almost exponential trend between current and voltage with an ideality factor of up to 1.2. The second trend, labeled F2, corresponds to diodes that showed an “excess current component” which is often observed in the case of ion implanted SiC diodes [70]. The excess current component is generally attributed to the presence of defects due to the ion implantation process in the junction depletion region [71]. The fact that at 1600°C a majority of the diodes did not show an excess current component, as shown in Table 3.1, is a promising result from the point of view of being able to reduce the formation of ion beam damage induced defects using the silane overpressure process. The trends F1 and F2 were observed for 97% of the 136 measured diodes. The percentage distribution of diodes that followed F1 and F2 is also given in Table 3.1.

Table 3.1: Summary of measured diode performance vs. anode size [72]

<table>
<thead>
<tr>
<th>Anneal Temp. (°C)</th>
<th>56 diodes</th>
<th>80 diodes</th>
<th>R_{sh} (Ω/□)</th>
<th>ρ (Ω-cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>∅ = 150 μm</td>
<td>∅ = 350 μm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>F1</td>
<td>F2</td>
<td>F1</td>
<td>F2</td>
</tr>
<tr>
<td>1600</td>
<td>93 %</td>
<td>5%</td>
<td>60%</td>
<td>35%</td>
</tr>
</tbody>
</table>

It was also observed that the turn-on voltage for the F1 diodes was about 1.75 V, which is a typical value for a good ion implanted diode [70]. Below this turn-on voltage both F1 and F2 diodes have a generation-recombination current a few orders of magnitude lower than the corresponding values published in the literature [70, 71]. This again was a promising result from the point of view of the energy dissipation when the
junction is in the off-state. For a forward bias voltage above 2.5 V the F1 and F2 curves overlapped and followed an exponential trend with an ideality factor up to 1.2.

The reverse bias trend for the F1 and F2 diodes did not, however, show any noticeable difference as shown in Figure 3.17 (a). The histogram of the grouped reverse bias characteristics for 350 μm diameter diodes at –100 V is as shown in Figure 3.17 (b). The spread of the values is very low and the average leakage current density was (9.7 ± 0.4) x 10^{-9} A/cm². A majority of the diodes displayed a leakage current of ~ 10 nA/cm².

![Figure 3.17: Electrical data taken on p⁺/n diodes annealed at 1600°C in silane. (a) Typical J-V reverse characteristics at -100V. (b) Histogram of the reverse current density values at –100 V for 75 diodes of 350 μm diameter. Average leakage current density was (9.7±0.4)×10^{-9} A/cm², and the spread of the values was very low.](image)

Table 3.1 also shows the sheet resistance and resistivity values of the implanted layer. An average sheet resistance on the order of 10^6 Ω/□ at room temperature was measured on the 400 μm x 400 μm VdP devices. A Cameca IMS-4f spectrometer SIMS
tool was used to measure the Al doping profile within the VdP area in the fully processed SiC wafer. An 8 keV O$_2^+$ primary beam having 150 nA total current was swept over a $125 \times 125 \, \mu m^2$ sputtering area. The secondary ion signal was collected from a central circular spot having 50 µm diameter as shown in Figure 3.18. From SIMS analysis using the half maximum width (HMW) the thickness of the implanted layer was found to be 110 nm with Al doping concentration of $5 \times 10^{19} \, cm^{-3}$. Using these values, the resistivity was calculated to be 11 Ω-cm, which is an order of magnitude higher than expected with respect to the best electrical activation results published in the literature [73]. The on-state forward voltage drop at 100 A/cm$^2$ was about 4.2 V, and the on resistance at the same current density was 12 mΩ-cm$^2$ diode which includes resistance contributions from the bulk, the epilayer, the implanted layer, and both front and back contacts.

![Figure 3.18: SIMS measurement of the Al profile on the full processed SiC wafer. Measurement was done inside the post-implant annealed sample inside the active area of a VdP device as shown in the inset.](image)
Forward and reverse characteristics, as well the breakdown voltage values, of these 
Al⁺ implanted p⁺/n diodes annealed in silane ambient were comparable with the best 
values obtained for similar implanted diodes but annealed in an Ar ambient [74, 75]. 
Moreover, the spread of the diode performances was very small, indicating a stable and 
robust process had been achieved. On the downside the high resistivity value of the 
implanted layer suggested the need to perform more studies to improve the electrical 
efficiency of the annealing process in silane ambient.

Electrical characterization was repeated on samples annealed using the cold-wall 
process at temperatures of 1600°C, 1650°C 1675°C and 1700°C (Set 2). Results obtained 
were similar to the Set 1 samples. The measurement statistics and process yield for this 
set of experiments are listed in Table 3.2 All electrical characterization was performed at 
room temperature and the experimental set-up has an instrumental current floor ranging 
from $10^{-13}$ to $10^{-12}$ A, depending on the measurement configuration.

Table 3.2: Statistics of the measured devices

<table>
<thead>
<tr>
<th>Annealing temperature (°C)</th>
<th>Measured diodes</th>
<th>diode yield</th>
<th>Measured VdP device</th>
</tr>
</thead>
<tbody>
<tr>
<td>1600</td>
<td>8</td>
<td>78%</td>
<td>2</td>
</tr>
<tr>
<td>1650</td>
<td>100</td>
<td>80%</td>
<td>10</td>
</tr>
<tr>
<td>1675</td>
<td>9</td>
<td>75%</td>
<td>8</td>
</tr>
<tr>
<td>1700</td>
<td>20</td>
<td>65%</td>
<td>2</td>
</tr>
</tbody>
</table>

Typical forward and reverse bias characteristics taken on the diodes are as shown 
in Figure 3.19(a) and (b), respectively. For temperatures $\geq 1675°C$ and a bias $\leq 1.65$ V
the diode forward current is below the instrument limitation (i.e. $10^{-13}$ A), while for a bias $> 1.6$ V the diode conduction could be modeled as an abrupt p$^+/n$ junction with a very low-level injection current and an ideality factor of $< 2$. For annealing temperatures $\leq 1650^\circ$C the forward current was generally higher than the instrument current floor at any bias value and could be modeled as that of an abrupt junction only for a bias of $\geq 2.1$ V, with an ideality factor of $\leq 2$. Figure 3.19 (a) also shows that the diode series resistance was more prominent for samples annealed at lower temperatures (i.e. $\leq 1650^\circ$C). The diode reverse conduction (Figure. 3.19 (b)) was on the order of the instrumental current floor (i.e. $10^{-12}$ A) for the samples annealed at temperatures $\geq 1675^\circ$C and increased for decreasing post-implantation annealing temperature. In summary these results indicated that as the annealing temperatures were increased, there was higher electrical activation of the implanted Al$^+$ ions, which corresponds to better electrical conduction of the p$^+/n$ junction.

Figure 3.19: Typical p$^+/n$ diode forward bias (left) and reverse bias (right) characteristics, measured for various post-implantation annealing temperatures in silane for Set 2 samples.
Figure 3.20 shows the trend of the sheet resistance values with respect to the post-implantation annealing temperature. As seen in the figure the sheet resistance value for samples annealed in non-optimized silane flow (Set 1) was slightly higher than the set 2 samples which correspond to optimized flow. Also the data shows that for increasing annealing temperature, the sheet resistance decreased to a minimum value of 70 kΩ.

Figure 3.20: Comparison of set 1 and set 2 sheet resistance of the implanted layer versus post-implantation annealing temperature. Set 2 data corresponds to optimized silane flow conditions.

As can be seen from Figure 3.20, high sheet resistance values remains an issue for the silane overpressure annealing process developed here. SIMS analysis of samples annealed in silane showed that there was some removal of the material from the surface. This could have occurred due to the presence of hydrogen, which results from the cracking of silane. This is just a preliminary hypothesis and more study on this was done during the hot-wall process development which is explained in detail in the next chapter.
3.4 Summary

Post-implantation anneals in an optimized silane ambient performed on Al\textsuperscript{+} implanted 4H-SiC samples in a cold-wall CVD reactor revealed no step bunching or surface morphology degradation up to 1700°C. Electrical characterization conducted on the annealed samples showed highly reproducible p\textsuperscript{+}/n diode performance and yield. Unfortunately the formation of silicon droplets was still an issue, especially at the edges of the sample, during some of the anneals. This could be due to the non-uniformity of the temperature profile across the sample in the cold-wall reactor because of higher cooling rates at the die edge due to radiation. This problem may be reduced by the development of a hot-wall CVD annealing process. Also there was an issue concerning the diodes studied having a higher than expected sheet resistance value of the implanted layer. Since this problem became evident at the end of the cold-wall research portion of this work, special attention was paid to this issue during hot-wall implantation annealing process development which is discussed in the next chapter.
CHAPTER 4
IMPLANT ANNEALING IN HOT-WALL CVD REACTOR

There are different types of CVD reactors based on their design and, in particular, orientation and hot zone environment. Chapter 3 focused on annealing research conducted in a cold-wall, low-pressure SiC CVD reactor. One of the major drawbacks of the cold-wall system is the difficulty in maintaining a uniform temperature across the entire wafer surface due to the high cooling rates at the susceptor edges compared with the central region. This was the main reason for the formation of Si droplets on the periphery of the many of the samples that were annealed in the cold-wall CVD reactor (Chapter 3). This temperature uniformity issue can be eliminated if the entire hot zone is maintained at a uniform temperature, which is possible in a hot-wall CVD configuration.

4.1 Hot Wall CVD

In the hot-wall CVD system, the susceptor completely surrounds the substrate to be annealed, thus eliminating any temperature gradients in the hot zone (or, at least, reducing them as much as possible to a minimum value). This is accomplished by supporting the susceptor by a carbon foam insulation material which encases the susceptor and provides adequate thermal insulation between the hot zone and the quartz tube wall. The insulation severely reduces radiation losses from the heated susceptor and
also providing an environment that decreases the particle nucleation in the gas phase [76]. Thus a hot-wall CVD system not only offers good uniform heating efficiency, but also a high cracking efficiency of the reactant gases [77].

Figure 4.1 shows a basic schematic of a horizontal-hot-wall CVD reactor. In this configuration, the ceiling, walls and the bottom of the susceptor, all of which are made of graphite, are heated with a radio frequency (RF) induction coil. The susceptor used consists of two pieces – a top part and a bottom part. The top part is SiC coated while the bottom part is TaC coated. The coating serves the purpose of preventing the leakage of C or other impurities from entering the growth system. After assembling the susceptor and placing it in the foam insulation, the components are slid into the quartz tube and the sample is placed on the bottom susceptor. The top susceptor is shown to have an angled ceiling, which will be explained in detail in section 4.2.

Figure 4.1: Schematic drawing of the horizontal hot-wall CVD reactor used in this research with an angled top ceiling.
A major advantage of the hot-wall CVD configuration is that the isothermal design of the susceptor assembly helps to reduce the RF power requirement. For example, in the hot wall system an RF power of 17 kW was required to achieve an annealing temperature of 1700°C versus 29 kW to obtain the same temperature in the cold-wall system, a 42% decrease in RF power. In addition to the advantages of an isothermal hot zone, where a reduction in Si-droplets at the periphery of the sample is expected, most SiC researchers have access to a silane-based hot-wall CVD reactor. Therefore research into the post-implantation annealing of SiC in hot-wall systems was undertaken and is reported in this chapter. The hot-wall CVD reactor used in the research was built in-house and a detailed explanation is given in the following section.

4.2 USF Hot-Wall CVD Reactor

The first hot-wall reactor used, designated as the “20 mm” reactor (based on the die size that can be processed) had the same tube design as the cold-wall CVD reactor. As explained in the last section a graphite foam insert containing the hot-wall susceptor was used as the hot zone instead of the susceptor sitting on the quartz boat as explained in the previous chapter. Initial implant annealing work at temperatures up to 1600°C was performed in this 20 mm hot-wall reactor. However, since the reactor was not designed for hot-wall operation but, rather, adapted to it, the quartz tube with the cooling water jacket cracked due to the thermal gradient at the high temperatures needed for implant annealing (indeed this was mostly due to a loss of insulation quality after excessive wear and tear on the system). In addition the “20 mm” reactor design was limited to a maximum die size of 2 cm, which is not suitable for a 2-inch or higher diameter wafer.
processing. Considering all these criteria, a new-large scale, 100 mm hot-wall reactor with an improved design (such as the elimination of the cooling water jacket, glass to glass seals, etc.) was built. Figure 4.2 shows a photograph of the “100 mm” hot-wall CVD reactor during high-temperature operation.

![Figure 4.2: Photograph of the “100 mm” horizontal hot-wall reactor during high-temperature operation. The graphite foam/susceptor insert shown here can hold up to a 2-inch wafer while use of a different insert can accommodate a 4-inch wafer.](image)

The front end of the quartz tube was clamped to a stainless-steel S. S. mounting hardware head plate via a steel ring and sealed with a Viton O-ring. The head plate was cooled with circulating chilled water. The back end of the quartz tube was clamped to a stainless-steel drum via an identical stainless-steel ring and also sealed with a Viton O-ring. The drum also comprises the exhaust port through which reactor by-products are
evacuated out of the system via a poppet value and dry pump where they are sent to a scrubber. A stainless-steel door was attached to the drum via hinges and was sealed with Viton O-rings and a C-clamp.

A photograph of the hot-wall susceptor is shown in Figure 4.3 (a). The SiC polyplate with recess sits on the bottom Tantalum Carbide (TaC) susceptor. Both susceptors were enclosed by insulating graphite foam as shown in Figure 4.3 (b).

Figure 4.3: Photograph of the (a) hot-wall susceptor: top susceptor is SiC coated and the bottom is TaC coated. (b) Front end of the graphite insulating foam after assembly (susceptor is inside) showing the hole used to sight the pyrometer for measurement of the susceptor temperature. Note that the samples are loaded on a polycrystalline plate with machined recesses as shown in (a).

The top susceptor, which was SiC coated, has an angled ceiling as was schematically shown in Figure 4.1. the angled ceiling was implemented because during epitaxial growth with the initial flat ceiling susceptor design reactants depleted at the inlet
of the susceptor due to the high cracking efficiency of the design. Since this is a well-known phenomenon in CVD growth a tilt in the ceiling was then incorporated as shown in the Figure 4.1 (in most CVD systems the floor is tilted but a titled ceiling will allow for wafer rotation, etc. which has advantages) [78]. The result was a reduction in the depletion of the reactants at the front of the susceptor hot zone inlet with more uniform deposition on the sample. The bottom susceptor was TaC coated graphite. It has been indicated that the lifetime of the susceptors and quality of the epitaxy has been improved by using TaC coated graphite since this coating is more durable than the conventional SiC coating [63]. The susceptor was enclosed in the graphite foam and inserted into a quartz liner as shown in Figure 4.2. The quartz liner not only held the insulating foam and graphite susceptor assembly together but also protected the outer tube from damage since hot graphite foam in contact with quartz generates COX which slowly degrades the quartz making it rough and difficult to clean. The liner was placed inside the horizontal quartz tube in such a way that the susceptor sat in the center of the RF induction coil, which heats the susceptor.

Initially there was a problem with the graphite foam which increased the coil inductance to such a high value that the RF generator source impedance could not be matched to the coil and, hence, the RF generator could not turn on. In order to overcome this issue the circular insulating foam was cut into the shape as shown in Figure 4.3, to reduce the RF load impedance so that the RF generator could turn on. Once this problem was solved the reactor was ready for initial growth process development. The samples were loaded on top of the TaC susceptor bottom part via a polycrystalline plate, which has machined recesses. The recesses were used to prevent sample movement during
growth and, in this case, post-implant annealing. In this way a repeatable sample temperature could be achieved thus allowing a more stable process to be developed.

The stainless-steel door was designed with a view port for the IR pyrometer and, after some difficulties with the window clouding during annealing, an Ar purge was implemented to keep the window clean. The temperature of the susceptor was measured by focusing the pyrometer at a circular indent on the back of the top susceptor which is SiC coated. The argon purge assembly was to minimize the coating of the view port with reactor byproducts during annealing, which would cause inaccurate reading of the actual temperature by the pyrometer. Also the view port was used to perform the Si melt test for calibrating the temperature of the susceptor. The idea and the method behind this test was the same as explained in Chapter 3, with the only difference that instead of the mirror the view port was used to monitor the peak of the solidified Si (which had been melted and solidified before). The temperature at which the peak disappeared is the Si melt temperature ($T_{Si}^{melt}$) which is 1410ºC under STP conditions. The corresponding reading on the pyrometer was then recorded ($T_{reading}^{melt}$) and $\Delta T = T_{reading}^{melt} - T_{Si}^{melt}$ computed. $\Delta T$ was then used to determine the desired set point temperature used for all implant annealing experiments. The melt test was periodically repeated to ensure maximum temperature accuracy throughout this research.

The gas handling system, the PLC and the pressure controlling unit was all similar to one used for cold-wall system, as explained in Chapter 3. A few changes were made to the control panel and the gas handling system. One improvement that directly impacted this research was the installation of a hydrogen purge stick on the main gas manifold. This was done to purge the gas manifold with purified hydrogen before and after the
introduction of process gases. In addition to the new hydrogen purge stick, since the cross-section of the hot-zone increased new mass flow controllers (MFC’s) capable of increased flow were installed for the carrier gases (H₂ and Ar) as well as the reactant gases (SiH₄ and C₃H₈).

The basic system operating modes, namely ‘purge’ mode and ‘process monitor’ mode, were identical to those explained in Chapter 3 for the cold-wall system. Several pump and purge cycles were performed before starting the annealing process. This was done to ensure reduction of contamination in the reactor prior to high-temperature annealing. The details of the annealing process are explained in the following section.

4.3 Post-Implant Annealing Experiments

In Chapter 2 the motivation for post-implantation annealing of SiC was explained while the cold-wall CVD process was described in Chapter 3. Although processes developed in a cold-wall CVD apparatus produced step-bunch free surfaces, there was still an occasional problem of silicon droplet formation, mostly at the edges of the sample. The reason behind this is the non-uniform temperature distribution across the samples. As explained in section 4.1, this problem can, in principle, be overcome in a hot-wall system which was the focus of the next phase of this research which is now described in detail.

4.3.1 Ion Implanted Samples

Similar to the cold-wall research described in Chapter 2, two sets of wafers were used for this work. A 2-inch, high-purity, semi-insulating 4H-SiC wafer with an 8° miss-
cut towards [11-20], designated W1, was implanted at Cree Inc. with $^{27}$Al$^+$ at 650°C in dual doses of $2 \times 10^{13}$ cm$^{-2}$ at 200 keV and $4 \times 10^{13}$ cm$^{-2}$ at 360 keV. Implantation was performed through a thin 500Å passivating film of SiO$_2$. SRIM simulation was performed to predict and to ensure a box profile for the doping profile. Secondary Ion Mass Spectroscopy (SIMS) was also performed to monitor the actual profile of the implanted sample. SIMS for this particular sample was performed by the surface analysis group of Prof. U. Starke at the Max-Planck Institute in Stuttgart, Germany using a Time of Flight SIMS (TOF-SIMS) instrument. Figure 4.4 shows the doping profile predicted by SRIM and the corresponding SIMS analysis performed on the as-implanted sample. From the figure it can be seen that the predicted and the measured peak Al doping concentration was $\sim 2.0e18$ cm$^{-3}$. Table 4.1 gives summary of the sample that was used for surface characterization.

The wafer was then diced into 8mm x 8mm and the samples cleaned in acetone and isopropanol and then RCA cleaned. All surface characterization reported in this research was performed on these samples. Since the implants were formed directly in the surface of a semi-insulating substrate, these samples were suitable for morphology study only and not for electrical activation assessment.
Figure 4.4: Comparison of doping profile vs. depth predicted by SRIM and the corresponding SIMS profile performed on the as-implanted W1 sample by the group of Prof. U. Starke of Max-Planck Institute, Stuttgart, Germany.

The second sets of samples were implanted at CNR-IMM by the group of Dr. Nipoti in Bologna, Italy, and are designated W3. These samples were from a 4H-SiC (0001) Si-face Cree epitaxial wafer, with an 8° mis-cut towards the [11-20] direction. The doping concentration and thickness of the epilayer was ~$1 \times 10^{16}$ cm$^{-3}$ and ~6 μm, respectively. Table 4.1 gives the implantation summary along with description of the sample W3.

**Table 4.1:** Summary of the samples used for both surface and electrical characterization.

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>Description</th>
<th>Implantation parameter</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1</td>
<td>4H-SiC semi-insulating</td>
<td>2e$13$ cm$^{-2}$, 200 keV</td>
<td>Surface</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4e$13$ cm$^{-2}$, 360 keV</td>
<td>Characterization</td>
</tr>
<tr>
<td>W3</td>
<td>4H-SiC, n-type, ~1e18 cm$^{-3}$</td>
<td>1.72e14, 250keV</td>
<td>Electrical</td>
</tr>
<tr>
<td></td>
<td>n’ epi, ~$1 \times 10^{16}$ cm$^{-3}$ &amp; 6μm</td>
<td>1.5e15, 360keV</td>
<td>Characterization</td>
</tr>
</tbody>
</table>
The samples were diced into 1 cm x 1.2 cm pieces prior to implantation. A 1.7 MV Tandetron accelerator was used to perform blanket implantation of Al\(^+\) ions into the SiC surface. A 4300 Å thick oxide passivating layer was deposited prior to implantation in order to place the peak of the implantation Gaussian profile at the surface of the sample. The implanted profile, as determined by SRIM, had a box shape with an Al ion concentration of \(8 \times 10^{19} \text{ cm}^{-3}\) and an implant depth of 0.2 \(\mu\text{m}\) from an integrated dose of \(1.75 \times 10^{15} \text{ cm}^{-2}\) as shown in Figure 4.5.

![Figure 4.5: Predicted SRIM doping profile of the Al ion implantation performed on W3 samples via 400Å deposited oxide and the inset shows the depth profile in the sample after etching the oxide. Implants performed by the group of Dr. R. Nipoti, CNR-IMM, Bologna, Italy.](image-url)
In order to reduce the crystal damage during implantation, ion implantation was done at the elevated temperature of 400°C. The implantation performed was a random implant in which the ion beam impinges on the 4H-SiC crystal at 15° with respect to the <0001> axis while remaining within a plane at 12° from the {11-20} crystal plane. Figure 4.6 shows the measured Al doping profile taken by a Cameca IMS-6f spectrometer SIMS tool, on one of these as-implanted samples at the Army Research Laboratory (ARL), MD USA by Dr. M. Wood. All non-contact electrical characterization (which is explained in section 4.5) for the hot-wall implant annealing process was performed on these samples.

Figure 4.6: SIMS measurement of the Al profile of the as-implanted sample. SIMS data taken by Dr. M. Wood of the Army Research Laboratory, Adelphi, MD.

4.3.2 **Post Implant Annealing Process**

After the samples were implanted and cleaned using the RCA process, the samples were loaded with the help of a polycrystalline plate with machined recess as
mentioned in section 4.2 and the plate loaded into the hot-zone of the CVD reactor. For initial implant annealing runs, the argon carrier gas flow was based on the carrier gas flow used for the baseline process for epitaxial growth. In the case of epitaxial growth in the cold-wall system 10 slm of hydrogen carrier gas was flown to obtain the baseline growth process for 4H-SiC [63]. This was raised to 40 slm [78] for the standard baseline process in the upgraded hot-wall system, which was four times the initial gas flow (this change makes sense since the hot-zone cross-section also increased by a factor of 4). Hence for initial implant annealing experiments 25 slm of argon was constantly flown in the reactor and the pressure maintained at 150 Torr until cool down. 100% silane was introduced into the reactor via the Ar carrier gas at a temperature of 1490°C, which is ~80°C above the Si melting point of 1410°C at standard temperature and pressure (STP). This was used to prevent the formation of Si droplets on the surface during the heating cycle. Due to limitations in the silane MFC, the minimum silane that could have been flown for the 1600°C process was 3 sccm (the MFC full-scale flow was 50 sccm and MFC’s are normally only accurate to within 10% of full-rated flow). The thermal ramp rate is also an important parameter to track during process development. It took approximately 15-16 minutes to reach temperature 1490°C after turning on the RF source. It took approximately another 3 minutes to reach the final anneal set point temperature of 1600°C. A total of 10 minutes of annealing in silane was performed from the time silane was turned on until the reactor was purged of silane prior to cool down. After 10 minutes the RF was turned off and, since the heat dissipation is much slower in the hot-wall system due to the insulating foam, the silane continued to flow until the temperature fell to 1490°C. This took approximately 2-3 minutes based on the annealing
set-point temperature. This was determined to be a necessary step in order to avoid any evaporation of silicon from the sample surface during this short cool down time.

To ensure that all silicon was purged from the reactor before cool down to temperatures below 1410°C, 35 slm of argon at the process pressure of 200 Torr was flown for 1 min after the silane was turned off. After 1 min of argon purging, the sample was cooled in 5 slm of Ar flow in atmospheric pressure until room temperature was reached. The cool down time was approximately 45 minutes. The sample was then removed and inspected under the optical microscope.

For a silane flow of 3 sccm in 25 slm of argon surface defects (craters), presumably made by silicon droplets, were observed on the samples when they were inspected under the optical microscope. Since this was the minimum stable flow possible from the silane MFC, the argon flow was increased by 10 slm to 35 slm. At 35 slm of argon flow, the lowest pressure that could be controlled by the pressure control system was 200 Torr. Annealing processes were repeated as mentioned above, but with 35 slm of argon and at 200 Torr with a silane flow of 3 sccm. The surface of the sample annealed at 1600°C did not contain any craters or step bunching and process development to higher temperatures was then conducted.

However at temperatures greater than 1700°C, a slight variation in the process had to be made in order to achieve a smooth surface morphology. When the same process as employed for temperatures less than 1650°C was implemented, the formation of Si-droplets was, even though the surface around the droplets was smooth. In the hot-wall system, the thermal ramp rate was much slower than in a cold-wall system and it took at least 3-5 minutes to reach the anneal temperature set point from 1490°C. The required
flow rate of silane for that particular anneal temperature could not be set at 1490°C as was the case for the cold-wall system. The silane flow was ramped along with the temperature in order to avoid the formation of Si droplets at temperatures above 1490°C but below the set point anneal temperature as shown in Figure 4.7. The thermodynamic simulations presented in Chapter 2 make this clear – one needs to flow ever increasing silane amounts as the process temperature increases. The need for variable silane flow during thermal ramping in the cold-wall system is not necessary due to the short ramp rates involved.

After several experiments conducted at temperatures greater than 1700°C, it was observed that trickling a very small amount of hydrogen (1 slm) into the reactor resulted in improved morphology than without hydrogen. The hydrogen was turned on only for the short duration after the anneal set point temperature had been attained. The most plausible reason for this process improvement was that the hydrogen prevented Si cluster formations while also performing a light etch on the surface of the implanted crystal. The later hypothesis was confirmed when SIMS was performed on these samples after non-contact electrical characterization and a slight removal of the implanted layer was detected. These results are presented in section 4.5.

Similarly during sample cool down, the silane flow rate was ramped down and turned off when the temperature of 1490°C was reached. As an illustration of the hot-wall implant annealing process developed during this research, the process schedule for the 1700°C run is shown in Figure 4.7.
Figure 4.7: Implant annealing process schedule for $T_1 = 1700\,^\circ C$ hot-wall CVD processing, indicating gas flow timing versus sample temperature. Note the silane flow is ramped along with the temperature. This was found to be necessary to achieve specular surface morphology for all temperatures above $1700\,^\circ C$.

After post-implantation annealing, the samples were removed from the reactor and surface characterization performed using the SEM and AFM, as described in section 4.4

### 4.4 Experimental Results

#### 4.4.1 Surface Characterization

The surface of all annealed samples was studied by optical microscopy and AFM. Optical microscopy is the fastest and the easiest method for obtaining a rough idea about
the surface morphology. Samples can be analyzed in air and the images display their natural color. For the Leitz Ergolux optical microscope in the NNRC cleanroom, the highest power objective was 100X. For e.g. Figure 4.8 (a) shows an optical micrograph of a sample annealed at 1750°C under non-optimized silane flow. The surface morphology is clearly observed to be poor and it would therefore be a waste of resources to do further extensive surface characterization on such a sample. Figure 4.8 (b) shows a different type of defect observable under the optical microscope. This sample contains surface craters that most probably were formed by the evaporation of Si-droplets which formed on the surface early in the 1600°C annealing process development.

Figure 4.8: Optical micrograph of (a) sample annealed at 1750°C under a non-optimized silane flow rate which is highly damaged. (b) Crater formation on a sample annealed at 1600°C, probably due to the formation of Si-droplets followed by etch removal. The magnification for both images is 50X.

In the case of optical microscopy (and, for that matter, electron microscopy), the depth of focus is the distance above and below the image plane over which the image
appears in focus. Thus, as the magnification increases the depth of focus decreases. In such a situation the SEM is a better choice of microscope because of its shallow depth of focus and higher resolution capability. However SEM analysis is qualitative and can be at times misleading, because of the detector positioning with respect to the sample as shown in Figure 4.9 (a) and (b). In this figure, the SEM and AFM images were taken on the same sample. Note that the SEM image shows a very smooth morphology, where as the RMS roughness determined by the AFM scan is 4.6 nm.

Figure 4.9: Surface morphology after annealing at 1650°C in a hot-wall system: (a) Plan view SEM micrograph of surface morphology at 10,000X. (b) AFM data of the surface morphology. RMS roughness ~ 4.6 nm The AFM scan area is 10μm x 10μm. Note the SEM did not reveal surface step-bunching whereas the ARM clearly shows the steps.

Considering this factor, only AFM scans were performed on the post-implant annealed samples, after a quick initial examination under the optical microscope. As explained in Chapter 3, the AFM was operated in tapping mode and scans performed in
two scan directions, at 0° and at 90° angles. This would avoid incorrect scan data in case the cantilever scan direction completely coincides with the step bunching orientation. For all samples studied the RMS roughness was noted to monitor any surface degradation caused by the high-temperature anneals.

For the 1600°C and 1650°C processes to result in smooth surfaces it was found empirically that 3 sccm and 3.75 sccm of 100% silane was required, respectively. The AFM scans were performed on the samples annealed at 1600°C and 1650°C and are as shown in Figure 4.10.

![AFM scans](image)

**Figure 4.10:** AFM data taken on post-implant annealed surfaces at temperatures of (a) 1600°C and (b) 1650°C. The AFM scan area was 10 μm x 10 μm. RMS roughness vs. process temperature is plotted in Fig. 4.12.

As per the thermodynamic calculations discussed in Chapter 2 as the annealing temperature is increased the silane flow rate should also be increased. Thus the silane flow was varied for each process temperature until step bunching was eliminated. It was also noticed that further increase in silane flow caused the formation of Si-droplets as seen in the cold-wall process.
As mentioned in the section 4.3.2, a slight variation in the process had to be made for samples annealed at temperatures greater than 1700°C in order to obtain a smooth morphology. Figure 4.11 (a) and (b) shows the AFM scan data taken on samples annealed at 1700°C and 1750°C, respectively. The RMS roughness was found to be 0.56 nm and 0.65 nm for 1700°C and 1750°C, respectively.

![AFM data taken on post-implant annealed surfaces at temperatures of (a) 1700°C and (b) 1750°C. The AFM scan area was 10 μm x 10 μm. RMS roughness vs. process temperature is plotted in Fig. 4.12.](image)

The average RMS roughness was obtained from the AFM scanned data. Figure 4.13 shows the plot of average RMS roughness vs. temperature.
Figure 4.12: Plot of average RMS surface roughness as a function of temperature after annealing in the hot-wall CVD configuration as measured with AFM. 10 μm x 10 μm scan size used for all data points.

The data of Figure 4.12 shows the surface roughness vs. temperature for the optimized processes. The optimized process flow was selected based on the observed surface roughness at each temperature. An example of this selection criterion is illustrated in Figure 4.13 for a single process temperature. For silane flows of 3.8 and 4.2 sccm severe step bunching was observed with a surface roughness of ~6 nm RMS. For silane flow of 4.5 sccm the step bunching was greatly reduced but still present with a roughness of ~2 nm. The step bunching was completely eliminated for silane flow of 4.7 sccm, which was confirmed by AFM where a roughness of less than 0.6 nm RMS. Thus using AFM as a quantitative measure of the surface roughness is valid.
Figure 4.13: Plot of average RMS surface roughness as a function of silane flow rate at 1700°C as measured with AFM. 10 μm x 10 μm scan size used for all data points. Severe step bunching was observed for silane flows less than 4.2 sccm, slight step bunching for 4.5 sccm and no step bunching was observed for 4.7 sccm.

Several preliminary experiments were conducted to obtain an optimized 1800°C process, since it is believed to be necessary to anneal Al implants at temperatures up to 1800°C [14]. Unfortunately due to the lack of sufficient resources and a non-availability of samples during the period of this research, this process temperature could not be established and will be part of the future work. Due to the same reason extensive electrical characterization could not be performed on the samples annealed in hot-wall system. Preliminary non-contact electrical measurements was performed for this work is presented in the following section.
4.4.2 Comparison with Theory

The process silane flow determined experimentally vs. temperature for the hot-wall CVD process is shown in Figure 4.14 along with the comparison with the theoretical silane flow rates.

Based on the data points shown in Figure 4.14, an exponential curve fit was applied to the data. The silane flow rate, $\Phi$, expressed as an exponential function of the form $y = ae^{bx}$ for both the theoretical and experimental data is given as

$$\Phi_{th} = 2.02 \times 10^{-14} \times e^{(1.9 \times 10^{-3}T)}$$  \hspace{1cm} (4.1)

$$\Phi_{exp} = 2.6 \times 10^{-6} \times e^{(8.6 \times 10^{-3}T)}$$  \hspace{1cm} (4.2)
From the figure and the equations it can be seen that there is difference between the experimental and theoretical flow rates. In addition to the possible mechanisms explained in Chapter 3, section 3.4, another probable reason could be because of depletion of Si near the graphite adapters before the silane reaches the hot zone. This is based on the observation of Si deposition on these graphite parts: clearly Si is being consumed upstream of the hot zone and, therefore, more silane is needed to compensate for this loss.

4.5 Electrical Characterization

Non-contact Electrical measurements were conducted on the n'/'n+ 4H-SiC epi samples designated as W3, by Dr. E. Oborina and Dr. A. M. Hoff based on their prior work performed on non-contact doping profiling on epitaxial SiC [79]. The purpose of this was to develop an in-process metrology technique for SiC processing, whereby characterization of annealed layers could be conducted during processing without the need for destructive test structure fabrication.

This technique is based on $Q^2$-V method, an earlier work done on doping profile extraction from dielectrics [80]. The basic idea is that a surface depletion layer is created by placing corona charge $Q_C$ of opposite polarity (compared to semiconductor surface) on the semiconductor surface. The doping $N_D$ (or $N_A$) of the depletion layer of width $W$ is then obtained from equations 4.3 and 4.4.

$$Q_C = qAWN_D \quad (4.3)$$

where $A$ is the area of the device area and $q$ is the elemental (electron) charge

$$Q_C^2 = 2q\varepsilon_0\varepsilon_sN_D \left[ V_D - V_o - \frac{kT}{q} \right] \quad (4.4)$$
where $\varepsilon_o$ and $\varepsilon_s$ are permittivity of free space and of the semiconductor, respectively, $V_D$ is the voltage drop, $V_0$ is the potential of the semiconductor Fermi level with respect to the conduction band and $kT$ is the thermal energy. This is similar to extraction of doping by C-V measurement of a Schottky barrier diode. The detailed explanation of the process and the parameters extracted is given by A. Savtchouk et al. [79]. The main advantage of this technique is that it is non-contact, non-destructive and preparation-free; hence we were able to perform electrical measurements efficiently and effectively on the same sample after sequential annealing processing steps.

The doping profile of the $n^-$ epitaxial layer ($N_D$) (sample W3) on an $n^+$ 4H-SiC substrate that were diced into 1cm x 1.2cm, was determined using this method before implantation and is shown in Figure 4.15. The doping concentration of the $n^-$ epitaxial layer was found to be in the upper $10^{16}$ cm$^{-3}$ range.

![Doping profile of W3 epitaxial film before implantation](image)

Figure 4.15: Doping profile of W3 epitaxial film before implantation, obtained by non-contact $Q^2-V$ measurement. Nd1, Nd2 and Nd3 are doping profiles of three different 1cm x 1.2 cm W3 samples. Data provided by Dr.’s E. Oborina and A. Hoff.
After Al implantation, non-contact C-V measurement was again performed to check if there was any difference in the doping profile. A very slight change was noticed in the corona discharge, which indicated a very small shift in the net doping concentration of the as-implanted surface. Post-implantation annealing was performed on samples for two different annealing temperatures at 1600°C and 1700°C. For each sample three sets of anneals were performed at the same temperature. In set 1 sample A and B were ramped up to anneal temperature of 1600°C and 1700°C, respectively. Once the set point temperature was reached the RF was turned off and the samples were cooled down as shown in Figure 4.16 (a). After non-contact electrical measurements of the sample were performed and doping profiles were extracted the samples were cleaned and annealing was performed on the same samples at same temperatures but for longer duration. In set 2 and set 3 the samples were annealed at the desired temperatures for 5 minutes each as shown in the schematic in Figure 4.16 (b). For set 3 the total annealing time at the desired anneal temperature was 10 minutes, excluding the ramp up and ramp down time for these temperatures.

![Figure 4.16: Annealing process schedule for the (a) set 1 and (b) sets 2 and 3 sequential annealing experiments. Two annealing temperatures were studied and the samples A and B, were annealed at temperature (D_T) of 1600°C and 1700°C, respectively.](image-url)
The non-contact measurement provided fast feedback of the degree of electrical activation achieved after each process step. The net doping concentration $N_A - N_D$ was extracted from the measured contact potential difference shown in Figure 4.17 and a histogram of the doping concentration data was plotted as shown in Figure 4.18. It can be seen that, in the case of sample A that was annealed at 1600°C, the net doping profile increased after each anneal process. Also as expected, electrical activation of the Al dopants increased with the temperature (sample B, which was annealed at 1700°C).

Figure 4.17: Measured contact potential difference (VCPD) during non-contact metrology of the samples annealed as per Fig. 4.16. Note that a qualitative difference in doping type, from n-type to p-type, was observed after the initial annealing step (Set 1).
Figure 4.18: Measured doping density vs. annealing sequence measured using non-contact electrical measurements developed by Hoff et al [79]. Note that the Set 1 anneal at 1700°C (sample B) yielded a higher degree of dopant activation than 3 successive anneals conducted at 1600°C (sample A). This outcome indicates that rapid annealing may be preferable to long thermal soak anneals.

One of the clearest outcomes of this first set of non-contact measurements was that the single process step at 1700°C appears to result in superior activation compared to 3 successive anneals at 1600°C. This seems to indicate that a more rapid thermal process is preferable over longer thermal soaking. This data is preliminary and is the subject of future work that is described in Chapter 5. An additional point was the processing trend seen on sample A. For this sample a gradual increase in electrical activation with the anneal time was observed, as expected. However this was not seen for sample B, which was annealed at the higher temperature of 1700°C. As the anneal time was increased further for 1700°C process, raw data obtained from non-contact measurement showed no
presence of Al dopants in the sample. The sample behaved more n-type than p-type, which led this conclusion to be drawn. In order to further investigate this issue, SIMS measurement was performed on both the samples (A and B) by Dr. M. Wood at the ARL. From the SIMS data it was confirmed that the surface of the sample was being etched during the annealing as shown in Figure 4.19 (a) and (b) for 1600°C and 1700°C, respectively.

![Figure 4.19: SIMS measurement of the Al profile on the samples annealed after 3 annealing steps (Set 1, 2, 3) at temperatures of (a) 1600°C and (b) 1700°C. Note that the sample annealed successively at 1700°C appears to no longer contain an Al implanted layer, most likely due to material removal during processing.](image)

Both the samples were annealed for the same time duration, i.e. sets 1, 2 and 3. Since the etch rate of SiC in hydrogen increases with temperature [81] the most likely
explanation is that the small amount of hydrogen introduced to ‘clean up the surface’ may be etching the implanted layer, but this is only speculation as this time. Clearly for the hot-wall silane overpressure implant annealing process to be of value to the community this issue must be resolved. Hence additional experiments and a few alternative solutions have been proposed and will be described in the next chapter.

4.6 Summary

Post-implantation anneals were performed on Al⁺ implanted 4H-SiC samples in a hot-wall CVD reactor using the silane overpressure method for temperatures up to 1750°C. Surface characterization of the implant annealed samples revealed no step bunching or surface morphology degradation. Preliminary electrical measurements done by non-contact technique showed successful electrical activation of the dopants. However from these preliminary results, it was also observed that there was slight etching of the surface material and hence removal of the implanted layer for long process runs at higher temperatures (i.e., 1700°C). SIMS analysis done on the samples confirmed the removal of the material. This could explain the higher sheet resistance of the implanted layer seen in the samples annealed in cold-wall CVD reactor (Chapter 3). To study this further and to solve this issue a few ideas have been developed and will be explained in the future work section of Chapter 5.
CHAPTER 5
SUMMARY AND FUTURE WORK

5.1 Summary

Post-implantation annealing process development of 4H-SiC implanted with Al ions was completed during this research work in both cold-wall and hot-wall CVD reactors. The primary goal of this research was to establish a silane over pressure annealing process so that the crystal damage caused during implantation, as well as dopant activation, could be performed while returning the surface morphology to the pre-implanted state. Therefore the process development conducted was focused on the improvement of the surface morphology during this research work, with full-activation of the dopants taking on a secondary role. As a consequence detailed surface characterizations of annealed films were performed using plan-view SEM and AFM. These characterization techniques showed that samples annealed with the silane over pressure process had a better surface morphology than the samples annealed with the conventional argon anneal process.

Empirical thermodynamic gas-phase chemistry models for the silane over pressure annealing process, both for cold and hot-wall reactors, were also developed during the course of this work. The thermodynamic calculations were performed to obtain theoretical silane flow rates as a function of annealing temperature. The basis for
this modeling was to ensure that the partial pressure of Si, derived from the cracking of silane in the gas phase, was greater than the vapor pressure of Si in the SiC substrate. If this condition is met then the principle behind the silane overpressure process would be valid, i.e. the suppression of preferential evaporation of Si from the SiC lattice is reduced and, hopefully, eliminated.

Based on the earlier work done in an atmospheric-pressure cold-wall CVD reactor, the new processes developed during this research were for low pressure operation. In the APCVD process the formation of Si droplets was an issue, hence shifting this process to low-pressure was desirable to reduce homogenous nucleation of Si in the gas phase. The annealing temperature was varied between 1600°C to 1700°C and the 3% silane premixed in UHP argon was introduced into the reactor via an argon carrier gas in such a concentration that step bunching of the surface, which is known to be caused by the selective evaporation of Si from the SiC lattice, was eliminated. Electrical characterization of cold-wall CVD annealed samples showed reproducible p+/n diode performance and yield. However the sheet resistance was found to be an order of magnitude higher than what was expected based on the ion dose and implant profile. In addition there was occasional issue of the Si droplets at the edges of the sample due to the non-uniform temperature distribution across the die. This is mainly to be expected in a cold-wall reactor due to the fact that only the substrate is heated and not the annealing zone around the sample. In addition, due to this high cooling rate of the sample in cold wall, the RF generator power required to do higher temperature anneals (above 1700°C) was more than our system could provide. Therefore cold-wall annealing has both a temperature uniformity problem and a limitation in annealing temperature that results in
annealed layers that are not fully activated (it is widely believed that Al implants require thermal anneals to be performed at temperatures approaching 1800°C !)

To overcome these limitations, research into post-implantation annealing in a hot-wall CVD reactor for anneal temperatures between 1600°C to 1750°C was conducted and a process developed. The process was similar to the process developed in the cold-wall reactor, except that 100% silane was used. The resulting surface after annealing was again found to be step-bunch free and smooth if the proper process procedure was followed. The issue of Si-droplet was completely eliminated. Preliminary electrical measurements taken by non-contact measurement methods showed an increase in electrical activation of the dopants with anneal temperature, as expected. However the electrical and SIMS measurements showed that there was slight etching of the surface material during annealing for longer duration anneals at the higher temperatures. Hence the process needs additional research and refinement, which will be the subject of the future work section of this chapter.

Due to the lack of resources, such as implanted samples, fresh graphite susceptors, adequate electrical characterization tools, and an in-house SIMS measurement capability no further research was possible to research solutions for these important issues. However further work based on some of the ideas developed for the improvement of the process are mentioned in the following sections. Indeed some of this work has already been started and is explained in detail in the following section.
5.2 Future Work

The goal of future research in the area of post-implant ion annealing of SiC layers should be to look into the issue regarding the partial removal of the implanted layer which resulted in a higher than expected sheet resistance. Etching could be occurring because of the presence of hydrogen due to cracking of silane. In order to confirm this hypothesis, high temperature anneals should be performed in Ar only (where there is no hydrogen present) and electrical characterization followed by SIMS measurements performed on the samples. This is perhaps the only experimental approach to understanding the etching mechanism in play here. A theoretical study, based on known hydrogen etch rates of SiC and using the partial pressure of hydrogen during silane overpressure processing should also be performed. This would be based on the model developed during this work whereby the Si and H partial pressures in the gas phased are calculated based on thermodynamics. While this approach cannot stand on its own merits, simulations coupled with the Ar annealing experiments described above should provide sufficient insight into the material removal issue.

While the slight removal of material is a concern it has been seen that the developed silane overpressure processes yield smooth, step-bunch free surfaces which is something that annealing in Ar simply cannot do. Therefore one approach to overcome the issue of material removal is to perform ion implantation through very thin passivating oxide layers. This would shift the peak of the implant Gaussian profile deeper inside the sample surface, thus ensuring that an adequate volume of the implanted layer remains after annealing. From the SIMS measurement it was estimated that approximately 300nm of the material was etched away after post-implantation annealing with silane
overpressure method at 1700°C and for 15 min. In order to test this idea out, a 400Å of oxide was deposited on a 4H-SiC sample with a 6 μm epilayer of doping density in mid $10^{16}$ cm$^{-3}$. The samples were shipped to Dr Nipoti at Bologna, Italy for implantation. Figure 5.1 shows the predicted SRIM implantation profile.

Figure 5.1: Predicted SRIMs profile of the Al$^+$ implantation preformed through 400Å of deposited oxide. The position of the sample surface after annealing is shown by a vertical line. Note that this would result in a peak of the implant profile residing on the sample surface after annealing at 1700°C for 15 min.

Non-contact electrical measurements, followed by SIMS analysis, should be performed on each of these samples. Once the process has been established, p$^+$/n diodes
should be fabricated and sheet resistance, as well as the doping profile of the annealed samples, extracted. Dr Nipoti’s group at CNR-IMM in Bologna, Italy, has kindly offered to perform the necessary electrical measurements and the samples should be shipped to her when they are ready. Prior to shipping the samples to Bologna, a thermal oxide could also be grown on the post-implanted annealed samples to realize metal oxide semiconductor capacitors (MOSCAP’s). This is to check the oxide-semiconductor interface for any kind of defects, which is very vital step in fabrication of metal oxide field effect transistor (MOSFET). The latter step of fabrication of MOSCAP’s can be performed at USF and the electrical measurements conducted by Dr. Hoff’s group using the non-contact measurement method described earlier in this dissertation.

Other than the conventional argon annealing process, which leads to severe surface degradation, samples annealed in silane overpressure process should also be compared with the samples annealed using a graphite cap. As explained in chapter 1, a graphite capping layer is formed by hard baking the photoresist [21]. This process could lead to contamination of the surface unlike silane overpressure process. The samples annealed by the graphite cap method, along with as-implanted SiC, will be supplied by Dr. Karl Hobart of Naval Research Laboratory (NRL), USA. The testing and comparison of both surface and electrical characterization can then be done at both USF and NRL.
References


[44]. SRIM download at the web page: [http://www.srim.org/SRIM](http://www.srim.org/SRIM)


[66]. Thomas Schattner, Homoepitaxial Growth of 4H and 6H-SiC in a 75mm Reactor, Master’s Thesis, Mississippi State University, Starkville, MS, May 2000.


Appendix A:

CEA: Chemical Equilibrium with Application software code

The NASA CEA program can calculate chemical equilibrium compositions for assigned thermodynamic states, which in the case of this research work is temperature and pressure. Chemical equilibrium can be expressed either in terms of equilibrium constants or minimization of the system free energy. The equilibrium constant relates to a chemical reaction which occurs under equilibrium conditions and free energy is a measure of the amount of work that can be extracted from the system. From the second law of thermodynamics the minimization of free energy is a requirement for any system to reach equilibrium. These methods can be generalized. However, in the case of the equilibrium constant approach, it is not suitable for a large chemical system since each species cannot be treated independently, unless a set of known reactions is specified a priori. Taking into consideration this factor, NASA implemented the minimization of free energy approach when they developed the CEA program.

The equilibrium condition can be stated in terms of several thermodynamic functions, such as the minimization of the Gibbs or Helmholtz energy. In order to characterize the thermodynamic state of the system, which is at constant pressure and temperature, the Gibbs energy is most easily minimized. Minimization of the Gibbs free energy can be obtained from both the first and second laws of thermodynamics. The first law of thermodynamics is the application of conservation of energy. It states that energy cannot be created or destroyed, but can be changed from one form to another. The second law of thermodynamics states that in all energy exchanges, if no energy enters or leaves
the system, the potential energy of the state will always be less than that of the initial state. A detailed derivation of minimization of Gibbs energy can be found in ref [57].

Initially the CEA program was written in ANSI standard FORTRAN 77. With the original NASA Lewis code running on a PC platform, a user friendly, graphical user interface, or GUI, “front end” was developed by Zeleznik and Gordon in 1961. Various versions of the equilibrium program or modifications of the program have been incorporated since then. The CEA library of thermodynamic data contains data for both reaction products and reactants. Thermodynamic data are provided with the program on a separate file, called thermo.inp (which is an input file) and the processed data are stored in thermo.lib for subsequent use by the CEA program. Another type of input is prepared by the user, which contains the specific problem to be solved and is stored as the “user-defined-filename”.inp file. A particular problem is specified initially by assigning a thermodynamic state such as temperature and pressure, as shown in Figure A.1

Figure A.1: Graphical screen capture from the CEA program. A problem is initiated in the CEA program by first assigning a thermodynamic state of the system.
To assign particular values for temperature and pressure, one needs to double click on the Assigning Temperature and Pressure – tab in Figure A.1. A window, as shown in Figure A.2, then comes up where a user can choose up to 16 temperature and pressure values via a GUI. Both temperature and pressure can be defined with four different systems of units system, as shown. The inputted values are saved and the window is closed by clicking on the save button.

![Figure A.2: Graphical screen capture from the CEA program. Window for inputting temperature and pressure values for a specific problem. Note four different options for units are provided for both temperature and pressure.](image)

After assigning the temperature and pressure values, the next tab, “Reactant,” is chosen. In this window the reactants for which the thermodynamic calculations are to be performed are entered, as shown in Figure A.3. For e.g. in Figure A.3 the reactants used for a 1600°C cold-wall implant annealing process are shown. Flow rates of argon, and silane were input as number of moles. The SiC substrate was also taken into
consideration in moles by adding SiC (b) to the reactants. A value much higher than the number of moles of argon and silane was assigned to SiC(b), to take into account the large amount of SiC present in the form of the solid substrate. Only the reactant that was available in the thermodynamic library could be chosen and beta-SiC was the only available polytype available to the user in the condensed form. However, from a thermodynamic point of view it does not matter which polytype of SiC is chosen so this does not lead to any errors in the calculation.

Figure A.3: Graphical screen capture from the CEA program. A snapshot of the window which shows reactants and corresponding values in number of moles is input.

Based on the reactants entered in the window shown in Figure A.3, CEA generates all possible complex solid, liquid and gaseous species. Figure A.4 shows all of the possible species for the reactants entered in the window shown in Figure A.3. The tabs that follow the reactant tabs “Only,” “Omit,” and “Insert,” allow the user to either
list only those species from the thermodynamic data file that are to be considered for the current problem, if not all, or omit certain species or must include certain species, respectively. If none of these three tabs are specified, CEA performs calculations on all the available species for the reactants entered in Figure A.3. Calculations of the condensed species are usually optional and CEA includes these species occasionally if they are required to obtain convergence. On the “insert” tab, condensed species to be included can be specified as possible product from the start of the calculations.

Figure A.4: Graphical screen capture from the CEA program. Gaseous and condensed species generated by CEA for the reactants shown in Figure A.3. Note in “only” tab one can choose whatever specie that is most probable can be chosen if not all.
The last tab is the “output” tab and is shown in Figure A.5. As shown in the figure, after the iteration is performed, there is an option to omit species with mole fractions lesser than user defined values (which in this case is 1e-10).

Figure A.5: Graphical screen capture from the CEA program. The window for the output tab. The thermodynamic state of the system along with the mole fractions of the species that are to be plotted are specified in this window.
The input file “user-defined-filename”.inp is saved and upon execution generates an output file with filename “user-defined-filename”.out and a plot file with filename “user-defined-filename”.plt. A plot file for specified thermodynamic states (temperature and pressure) and mole fractions of the species obtained after performing iterations on the reactant species is generated by choosing the thermodynamic state and list of species on the output tab shown in Figure A.5. All these files .inp, .out and .plt are in the ASCII format and can be opened in a notepad or word pad. The plot file is the most convenient file to access the processed data.

A sample of the both output file followed by the plot file for a problem with reactants shown in Figure A.3 at temperature of 1600°C and pressure of 150 Torr and 760 Torr is shown below

**Output file:**

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NASA-GLENN CHEMICAL EQUILIBRIUM PROGRAM CEA2, MAY 21, 2004
BY BONNIE MCBRIDE AND SANFORD GORDON
************************************************************************

problem
  tp t,c=1600, p,mmhg=150,760,
react
  name=Ar moles=6000
  name=SiC(b) moles=10000
  name=SiH4 moles=0.32
only
  Ar C CH CH2 CH3 CH4 C2H H H2 Si SiC SiC2 SiH SiH2 SiH3 SiH4 Si2 Si2C Si3
  Si(cr) Si(L) SiC(b)
output trace=1e-10
  plot p t Ar H H2 Si SiC2 SiH SiH2 Si2 Si2C Si3 Si(L) SiC(b)
end

OPTIONS: TP=T HP=F SP=F TV=F UV=F SV=F DETN=F SHOCK=F REFL=F INCD=F
RKT=F FROZ=F EQL=F IONS=F SIUNIT=T DEBUGF=F SHKDBG=F DETDBG=F TRNSPT=F
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ADD Si(L)
1 2 1873.150 -22.726 -5.507 -5.982 -15.049
2 4 1873.150 -21.103 -5.507 -5.982 -14.218

THERMODYNAMIC EQUILIBRIUM PROPERTIES AT ASSIGNED TEMPERATURE AND PRESSURE

CASE =

<table>
<thead>
<tr>
<th>REACTANT</th>
<th>MOLES</th>
<th>ENERGY</th>
<th>TEMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>Ar</td>
<td>6000.000000</td>
<td>0.000</td>
</tr>
<tr>
<td>NAME</td>
<td>SiC(b)</td>
<td>***********</td>
<td>0.000</td>
</tr>
<tr>
<td>--------</td>
<td>--------</td>
<td>-------------</td>
<td>-------</td>
</tr>
<tr>
<td>NAME</td>
<td>SiH4</td>
<td>0.3200000</td>
<td>0.000</td>
</tr>
</tbody>
</table>

O/F = 0.00000  %FUEL = 0.000000  R_EQ_RATIO = 0.000000  PHI_EQ_RATIO = 0.000000

**THERMODYNAMIC PROPERTIES**

| P, BAR   | 0.19998 | 1.0132 |
| T, K     | 1873.15 | 1873.15 |
| RHO, KG/CU M | 1.3709-1 | 6.9460-1 |
| H, KJ/KG | 306.96  | 306.80  |
| U, KJ/KG | 161.07  | 160.92  |
| G, KJ/KG | -6108.25 | -5871.53 |
| S, KJ/(KG)(K) | 3.4248 | 3.2984 |
| M, (1/n) | 106.759 | 106.764 |
| MW, MOL WT | 40.039 | 40.039 |
| (dLV/dLP)t | -1.00005 | -1.00001 |
| (dLV/dLT)p | 1.0013  | 1.0003  |
| Cp, KJ/(KG)(K) | 1.0115 | 1.0094 |
| GAMMAa | 1.0836  | 1.0836  |
| SON VEL,M/SEC | 397.6 | 397.6 |

**MOLE FRACTIONS**

| *Ar     | 3.7498-1 | 3.7498-1 |
| *H      | 5.4079-6 | 2.4507-6 |
| *H2     | 3.7235-5 | 3.8746-5 |
| *Si     | 1.6566-5 | 3.2694-6 |
| SiC2    | 9.178-10 | 1.811-10 |
| SiH     | 1.1590-7 | 5.2522-8 |
| SiH2    | 1.796-10 | 1.869-10 |
| Si2     | 4.8460-7 | 9.5641-8 |
| Si2C    | 6.5241-7 | 1.2876-7 |
| Si3     | 1.4964-7 | 2.9533-8 |
| Si(L)   | 1.2473-6 | 1.6268-5 |
| SiC(b)  | 6.2496-1 | 6.2496-1 |

* THERMODYNAMIC PROPERTIES FITTED TO 20000.K

PRODUCTS WHICH WERE CONSIDERED BUT WHOSE MOLE FRACTIONS WERE LESS THAN 1.000000E-10 FOR ALL ASSIGNED CONDITIONS

<table>
<thead>
<tr>
<th>*C</th>
<th>*CH</th>
<th>CH2</th>
<th>CH3</th>
<th>CH4</th>
<th>*C2</th>
<th>C2H</th>
<th>SiC</th>
<th>SiH3</th>
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<tbody>
<tr>
<td>SiH4</td>
<td>Si(cr)</td>
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<td></td>
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122
**Plot File:**

<table>
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<tr>
<th>p</th>
<th>t</th>
<th>H</th>
<th>H2</th>
<th>Si</th>
<th>SiC2</th>
<th>SiH</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.00E-01</td>
<td>1.87E+03</td>
<td>5.41E-06</td>
<td>3.72E-05</td>
<td>1.66E-05</td>
<td>9.18E-10</td>
<td>1.16E-07</td>
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<tr>
<td>1.01E+00</td>
<td>1.87E+03</td>
<td>2.45E-06</td>
<td>3.87E-05</td>
<td>3.27E-06</td>
<td>1.81E-10</td>
<td>5.25E-08</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>p</th>
<th>t</th>
<th>H</th>
<th>H2</th>
<th>Si</th>
<th>SiC2</th>
<th>SiH</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiH2</td>
<td>Si2</td>
<td>Si2C</td>
<td>Si3</td>
<td>Si(L)</td>
<td>SiC(b)</td>
<td></td>
</tr>
<tr>
<td>1.80E-10</td>
<td>4.85E-07</td>
<td>6.52E-07</td>
<td>1.50E-07</td>
<td>1.25E-06</td>
<td>6.25E-01</td>
<td></td>
</tr>
<tr>
<td>1.87E-10</td>
<td>9.56E-08</td>
<td>1.29E-07</td>
<td>2.95E-08</td>
<td>1.63E-05</td>
<td>6.25E-01</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SiH2</th>
<th>Si2</th>
<th>Si2C</th>
<th>Si3</th>
<th>Si(L)</th>
<th>SiC(b)</th>
<th></th>
</tr>
</thead>
</table>

The plot file is used to analyze the computed data and as mentioned in Chapter 2, section 2.4 further computation was performed to obtain the final plots shown in Figure 2.8 and 2.9.
About the Author

Shailaja Rao received the Master of Science degree in Electrical Engineering from the University of South Florida in 2002 where she completed research on SiC based transistors. Prior to her Master’s studies, she completed the Bachelors degree in Electrical Engineering from the Mangalore University, Mangalore, India. She has been pursuing her PhD in Electrical Engineering since that time and has been active in all aspects of the research work being conducted in the USF SiC Group, in which she is the first student to earn the PhD degree. Her research has focused on novel SiC device processing, including the work reported here, and she has actively supported industry and federal government sponsors through her work. Dr. Rao plans to continue working for the USF SiC Group after graduation as a post-doctoral researcher focusing in the area of SiC epitaxy and bulk crystal growth.