November 2018

Duty-Cycle Based Physical Unclonable Functions (PUFs) for Hardware Security Applications

Mahmood Javed Azhar
University of South Florida, mahazh@gmail.com

Follow this and additional works at: https://scholarcommons.usf.edu/etd

Part of the Electrical and Computer Engineering Commons

Scholar Commons Citation
Azhar, Mahmood Javed, "Duty-Cycle Based Physical Unclonable Functions (PUFs) for Hardware Security Applications" (2018). Graduate Theses and Dissertations. https://scholarcommons.usf.edu/etd/7470

This Dissertation is brought to you for free and open access by the Graduate School at Scholar Commons. It has been accepted for inclusion in Graduate Theses and Dissertations by an authorized administrator of Scholar Commons. For more information, please contact scholarcommons@usf.edu.
Duty-Cycle Based Physical Unclonable Functions (PUFs) for Hardware Security Applications

by

Mahmood Javed Azhar

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy
Department of Electrical Engineering
College of Engineering
University of South Florida

Major Professor: Selçuk Köse, Ph.D.
Sanjukta Bhanja, Ph.D.
Ismail Uysal, Ph.D.
Mehran Kermani, Ph.D.
Fathi Amsaad, Ph.D.

Date of Approval:
October 29, 2018

Keywords: Regulator, Process, Voltage, Temperature, (PVT), Current, Control

Copyright © 2018, Mahmood Javed Azhar
DEDICATION

To my parents, all of my immediate and extended family members, specifically my son, Ebraheem Ali Azhar, Ph.D. Electrical Engineering, Arizona State University, and all the supporting members of academia and my long time colleagues in business and industry.
ACKNOWLEDGMENTS

I would like to thank my major Professor Dr. Selçuk Köse, and the advisory committee members, Dr. Sanjukta Bhanja, Dr Ismail Uysal, Dr. Mehran Kermani, and Dr. Fathi Amsaad for their help and support during my Ph.D. work.

I would also like to thank Dr. Tom Weller, Dr. Christos Ferekides, Dr. Huseyn Arslan, Dr. Wilfrido Moreno, Dr. Ravi Sankar, Dr. Nasir Ghani, Dr. Jing Wang, Dr. Lawrence Dunleavy, Dr. Alexandar Castellanos, Dr. Richard Gitlin, Dr. Arthur Snider, and Dr. Drew Hoff, the management and teaching staff at the University of South Florida (USF), Tampa, Florida, for providing support to me during my studies at the USF.

I would also like to thank Dr. Zafar Qureshi, Dean, College of Engineering, Air University in Islamabad Pakistan for his encouragement to finish my Ph.D. studies. I would like to thank my family, friends and fellow student colleagues, Longfei Wang, Wieze Wu, Orhun Aras Uzun, Mohammad Ali Vosoughi, and Ahmad Khan for their encouragement, help and support. I would like to also thank other colleagues, teaching assistants at USF who participated with me in my studies in academic classes at USF.

I am also thankful to the staff at USF Graduate School and Department of Electrical Engineering, Kristin Brandt, Diana Hamilton, and Catherine Burton for helping me with guidance to complete necessary documentation including this dissertation and other administrative paperwork for my graduate work. Finally yet importantly, I am thankful to National Science Foundation for providing the funding for part of the research work.
# TABLE OF CONTENTS

LIST OF TABLES iii

LIST OF FIGURES iv

ABSTRACT vii

CHAPTER 1: INTRODUCTION 1
  1.1 Overview of Duty Cycle Based Applications in Engineering 1
  1.2 Voltage Regulation Methods and Applications of Variable Duty Cycle 4
  1.3 Voltage Regulators and On-chip Security Consideration 7
  1.4 Pulse Width Modulation 8
  1.5 Motivation for a New PWM Architecture 9
  1.6 Controlled Oscillator Circuit 10
  1.7 Hardware Security and On-chip Physical Unclonable Function 11
  1.8 Organization 12

CHAPTER 2: NOVEL DIGITALLY CONTROLLED PULSE WIDTH MODULATOR 13
  2.1 Introduction 13
  2.2 Controlled Ring Oscillator Architecture 16
  2.3 Ring Oscillator Topology 16
  2.4 Controlled Duty Cycle and Frequency Analytical Details 18
  2.5 Details of PWM Circuit Components 24
    2.5.1 Duty Cycle to Voltage Converter 24
    2.5.2 Header and Footer Current Sources 24
  2.6 Controlled Duty Cycle and Frequency Simulation Results 26
    2.6.1 Digitally Controlled Variable Duty Cycle Ring Oscillator 26
    2.6.2 Digitally Controlled Constant Frequency Ring Oscillator 26
    2.6.3 PVT Compensated Ring Oscillator 27
  2.7 PWM Performance Summary Comparisons 28
  2.8 PWM Conclusions 29

CHAPTER 3: DUTY CYCLE BASED PHYSICAL UNCLONEABLE FUNCTION 30
  3.1 Introduction 30
    3.1.1 Contributions to PUF Work 32
    3.1.2 Background Work Comparisons and Organization 33
  3.2 Frequency versus Duty Cycle Based PUF 34
    3.2.1 Impact of Number of Inverter Stages 35
    3.2.2 Impact of Inverter Rise and Fall Time Variance 36
3.2.3 Improving Duty Cycle Spread Over Process Corners 37
3.2.4 Mismatched RO Circuit Analysis and Simulation Results 39

3.3 Prior Relevant Work
3.3.1 Duty Cycle Sensitivity Analysis 40

3.4 Proposed Duty Cycle PUF Circuit Architecture
3.4.1 Header Current Source Variability Analysis 42
3.4.2 Mismatched Header Current Source Analysis 44
3.4.3 Duty Cycle Spread Enhancement with Source Gate Voltage 46
3.4.4 Proposed PUF Environmental Stability Enhancement 47

3.5 Proposed PUF Simulation Results 48

3.6 Reconfigurable PUF Operation and Simulation 50

3.7 PUF Qualitative Characteristics and Measures
3.7.1 Uniqueness 51
3.7.2 Reliability 52

3.8 PUF Quality Measure Comparisons 53

3.9 Derivation of Equations
3.9.1 Duty Cycle Sensitivity with Respect to Header Currents 54
3.9.2 Source Gate Voltage Impact on Current Variability 55
3.9.3 Source to Drain Voltage Mismatch 56

3.10 Duty Cycle Based PUF Conclusions 58

3.11 PVT Stable Adaptable Duty Cycle Based PUF
3.11.1 PWM Preliminaries Recapped 60
3.11.2 PWM Based Adaptable Duty Cycle PUF Primitive 62

3.12 Adaptable Duty Cycle Based PUF Details
3.12.1 Adaptable PUF Unique Outputs 64
3.12.2 Adaptable PUF PVT Stability Simulation Results 64

3.13 Adaptable Duty Cycle PUF Reliability Simulation Results 65
3.14 Adaptable Duty Cycle Based PUF Conclusions 66

CHAPTER 4: FINAL CONCLUSIONS 68

CHAPTER 5: FUTURE WORK 69

REFERENCES 71

APPENDIX A: COPYRIGHT PERMISSIONS 84
A.1 Copyright Permission Page 84
A.2 Copyright Permission Page 85
A.3 Copyright Permission Page 86
A.4 Copyright Permission Page 87
A.5 Copyright Permission Page 88

ABOUT THE AUTHOR END PAGE
### LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 2.1</td>
<td>Duty cycle and frequency changes with header and footer currents</td>
<td>17</td>
</tr>
<tr>
<td>Table 2.2</td>
<td>Duty cycle PVT variations</td>
<td>28</td>
</tr>
<tr>
<td>Table 2.3</td>
<td>PWM comparisons with other state-of-the art implementations</td>
<td>29</td>
</tr>
<tr>
<td>Table 3.1</td>
<td>Proposed PUF comparisons with other state-of-the art on-chip PUF implementations</td>
<td>54</td>
</tr>
</tbody>
</table>
**LIST OF FIGURES**

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Inductive switching voltage regulator</td>
<td>5</td>
</tr>
<tr>
<td>1.2</td>
<td>Hybrid voltage regulator</td>
<td>6</td>
</tr>
<tr>
<td>2.1</td>
<td>Conventional ring oscillator</td>
<td>13</td>
</tr>
<tr>
<td>2.2</td>
<td>Inductive switching voltage regulator</td>
<td>15</td>
</tr>
<tr>
<td>2.3</td>
<td>Block diagram of the pulse width modulator</td>
<td>16</td>
</tr>
<tr>
<td>2.4</td>
<td>Seven stage ring oscillator circuit topology</td>
<td>17</td>
</tr>
<tr>
<td>2.5</td>
<td>Typical ((2m+1)) stage ring oscillator circuit with header control</td>
<td>18</td>
</tr>
<tr>
<td>2.6</td>
<td>((2m+1)) stage ring oscillator with two headers</td>
<td>20</td>
</tr>
<tr>
<td>2.7</td>
<td>Simplified schematic of DC2V</td>
<td>24</td>
</tr>
<tr>
<td>2.8</td>
<td>Header current source circuit</td>
<td>25</td>
</tr>
<tr>
<td>2.9</td>
<td>Footer current source circuit</td>
<td>25</td>
</tr>
<tr>
<td>2.10</td>
<td>Duty cycle variation with header current (IA, IB) and (IC, ID) variation</td>
<td>26</td>
</tr>
<tr>
<td>2.11</td>
<td>Constant frequency simulation and theoretical comparison</td>
<td>27</td>
</tr>
<tr>
<td>3.1</td>
<td>Architecture of a conventional ring oscillator PUF</td>
<td>31</td>
</tr>
<tr>
<td>3.2</td>
<td>Typical ring oscillator circuit (a) Ring oscillator circuit with ((2m+1)) inverter stages (b) Transistor level schematic of a ((2m+1)) stage ring oscillator</td>
<td>34</td>
</tr>
<tr>
<td>3.3</td>
<td>Standard deviation variations of the frequency and duty cycle with number of inverters</td>
<td>36</td>
</tr>
<tr>
<td>3.4</td>
<td>Standard deviation variations of the duty cycle and frequency of the ring oscillator under varying standard deviations of the inverter rise time</td>
<td>37</td>
</tr>
</tbody>
</table>
Figure 3.5  Frequency and duty cycle spread versus rise time spread  38
Figure 3.6  Duty cycle variations versus voltage and temperature with
a) no mismatch and b) mismatch c) no mismatch and d) mismatch  39
Figure 3.7  Mismatched RO circuit output duty cycle histogram  39
Figure 3.8  Block diagram of pulse width modulator  41
Figure 3.9  Duty cycle controlled ROPUF architecture  41
Figure 3.10  Digitally controlled current source  42
Figure 3.11  Variation of duty cycle with source drain mismatch factor K  45
Figure 3.12  Impact of source gate voltage $v_{sg}$ and K on duty cycle spread  47
Figure 3.13  PUF circuit simulation a) duty cycle versus temperature
b) duty cycle versus supply voltage  48
Figure 3.14  Proposed PUF circuit output duty cycle histogram  49
Figure 3.15  Standard deviation reliability of the duty cycle a) with temperature
b) with supply voltage  49
Figure 3.16  Re-configured PUF circuit simulation a) duty cycle versus
temperature b) duty cycle versus supply voltage  50
Figure 3.17  Duty cycle controlled PUF challenge response blocks  51
Figure 3.18  a) Temperature reliability b) Supply voltage reliability  52
Figure 3.19  Ring oscillator circuit with $2m+1$ inverter stages  60
Figure 3.20  Duty cycle at the nodes $N1-N7$ under different delay ratio $K$-factor  61
Figure 3.21  Block diagram of the header and footer based pulse width modulator  61
Figure 3.22  Seven-stage current controlled ring oscillator circuit  61
Figure 3.23  Redesigned seven-stage current controlled ring oscillator  62
Figure 3.24  Duty cycle at nodes $N1-N7$ under different current ratio K-factor  63
Figure 3.25  Duty cycle histogram for $(\alpha/\beta) > 1$ (top) $(\alpha/\beta) < 1$ (bottom)  64
Figure 3.26  Temperature versus duty cycle for output nodes N1-N7  
Figure 3.27  Supply voltage versus duty cycle for output nodes N1-N7  
Figure 3.28  Standard deviation (left) and mean (right) values of the duty cycle under temperature variations.  
Figure 3.29  Standard deviation (left) and mean (right) values of the duty cycle under supply voltage variations
ABSTRACT

Duty cycle and frequency are important characteristics of periodic signals that are exploited to develop a variety of application circuits in IC design. Controlling the duty cycle and frequency provides a method to develop adaptable circuits for a variety of applications. These applications range from stable on-chip clock generation circuits, on-chip voltage regulation circuits, and Physical unclonable functions for hardware security applications. Ring oscillator circuits that are developed with CMOS inverter circuits provide a simple, versatile flexible method to generated periodic signals on an IC chip. A digitally controlled ring oscillator circuit can be adapted to control its duty cycle and frequency. This work describes a novel current starved ring oscillator, with digitally controlled current source based headers and footers, that is used to provide a versatile duty cycle and a precise frequency control. Using this novel circuit, the duty cycle and frequency can be adapted to a wide range of values. The proposed circuit achieves i) a controlled duty cycle that can vary between 20% and 90% with a high granularity and ii) a compensation circuit that guarantees a constant duty cycle under process, voltage, and temperature (PVT) variations.

A novel application of the proposed PWM circuit is the design and demonstration of a reliable and reconfigurable Duty-cycle based Physical unclonable function (PUF). The proposed PWM based PUF circuit is demonstrated to work in a reliable and stable operation for a variety of process, voltage and temperature conditions with circuit implementations using 22nm and 32nm CMOS technologies. A comparative presentation of the duty cycle based PUF are provided using standard PUF figures of merits.
CHAPTER 1:

INTRODUCTION

1.1 Overview of Duty Cycle Based Applications in Engineering

The use of controlled duty cycle factor in systems varies in applications ranging from power engineering, to integrated circuit design. In power engineering and mechanical engineering, the activity of systems, machines and equipment is controlled over duty cycle periods to enhance the lifetime and to provide protection from excessive overloading conditions that may result in failure while achieving a high performance of fuel efficiency [1, 2, 3]. An example is the use in automotive fuel injection systems where pulse width modulation is adapted to adjust the amount of time injectors are turned on for achieving a high combustion fuel efficiency within the reasonable limits of speed and output power control [4].

In other applications such as laser pulse generation, a duty cycle adjustment of laser sources is used to produce precisely timed laser pulses. Laser sources are operated with a variable duty cycle to improve efficiency and to control the temperature and power consumption during pulse generations [5, 6]. In a variety of digital control based applications, such as robotics, the duty cycle of the control signals helps to regulate the amount of time the control signal are used to provide control activity [7].

In wireless applications, duty cycle is used in a variety of applications to enhance the performance of the system. In wireless sensory networks, duty cycle is used extensively to achieve power conservation of the system for maximum throughput [8].
On the level of physical layer, several wireless applications have been proposed that use duty cycle modulation methods for software-defined radios [9, 10]. Duty cycle based multiplexing schemes are used in coaxial wireless communication links to achieve optimum throughput through the use of shared hardware resources for multiple data streams [11].

In semiconductor applications, duty cycle is used in numerous domains to provide control and performance improvement and achieve optimization goals. During semiconductor device characterization, input signals are applied with variable duty cycles to control the heat dissipation and measure stable and accurate device characteristics [12, 13]. In low power sampling integrated circuits, offset voltage control and noise reduction depends on precise control of the duty cycle of sampling [14]. The long-term life of an IC depends on the characteristics of the duty cycle of signals on the chip. Long term device failures due to hot carrier mobility effects [15], negative bias temperature instability (NBTI), positive bias temperature instability (PBTI) [16, 17], in digital and analog circuits can be considerably reduced by balancing the time the devices are subjected to high and low voltage levels on the device active terminals [18]. The impact of NBTI and PBTI on device characteristics can impact the performance of the circuit long before the devices completely fail. Dynamic circuit analysis of the conditions under which the NBTI and PBTI impact, becomes serious, is analyzed as a part of robust design process [19]. The impact of performance can be controlled by adjusting the duty cycle of the signals under normal operation or by subjecting the terminals to a periodic cycle of low voltage, preferably ground potential, in a relaxation phase.

The duty cycle of the logic signals on digital integrated circuit are maintained within a set of safety guard-bands to prevent indeterminate states either due to violations due to active period requirements (minimum pulse width) [20, 21] or due to timing delay violation of signal in its relationship with the intrinsic gate delay [22]. Hazards and glitches in combinational logic circuits
and indeterminate states in synchronous logic circuits are a common source of failure and high power consumption [23, 24]. Multi-threshold logic circuits further exacerbate the issues of requirements of signal integrity on-chip and requires a careful design consideration to help reduce the glitch power [25-27].

The clock pulse width plays an important role in evaluation of synchronous logic and memory circuits [21]. In order to maintain a constant duty cycle of clock signals, for synchronous logic and memory circuits several methods have been proposed and adopted in the industry. [28, 29]. Power, ground substrate coupling noise can be considerably reduced on chip by randomizing the clock signal [30]. The proposed method [30], randomly varies the duty cycle of the clock before applying to sequential digital circuits. The proposed method describes a technique to use a synchronizer to synchronize data and periodic clocks. The proposed scheme demonstrated a considerable reduction in harmonic power in clock signals. During integrated circuit layout, shielding methods are adopted to suppress power ground noise propagation into the critical circuits.[31].

Hardware resources inside the computer chips are duty cycle scheduled in time and resource domain to enhance system performance (power consumption and speed) and are combined with techniques such as pipelining and parallel processing in a manner to provide maximum system throughput for a given set of resources [32]. The scheduling, pipelining and parallel processing circuits use frequency and duty cycle stable clock sources [33, 34].

In modern integrated geometrically scaled circuits used in portable applications, performance and power conservation trade-offs are achieved using frequency and voltage scaling methods [35, 36]. High operating frequency results in complications of circuit design and results in significant power loss in circuits [35]. Variable frequency and duty cycle control circuits assist
to provide optimum voltage regulation and frequency regulation on the integrated circuits for achieving power/performance trade-off [36]. The clock frequency, duty cycle and voltage regulation has to be maintained over wide range of process voltage and temperature conditions [37-39]. Additionally, voltage regulation and clock circuits must be adaptable to spatially and environmentally changing electrical parameter distribution on the chip [40-43]. Extensive analysis and simulation of parasitic capacitance and resistance of interconnects allows to implement safe band guards for the clock and power circuit designs to work under varying conditions [44 - 46].

1.2 Voltage Regulation Methods and Applications of Variable Duty Cycle

With the advent of scaled multi-voltage, multi-threshold CMOS transistors over the last decade and a half, the possibility of low power and high performance integrated circuit design applications have become a reality. The need for high performance and high efficiency voltage regulators that provide the stable voltage to an integrated circuit has become a necessity. Point of the load, on-chip voltage regulators have become an important component in integrated circuits as a means to achieve the goal of low power and high performance circuit design [47-50]. Co-design of the power network and the voltage regulation strategy relies heavily on the proper placement of decoupling capacitors in the network [51, 52]. Various architectures have been reported in the literature that can be optimized for variety of parameters to benefit the voltage and power scaling. New architectures and design styles continue to emerge every year as the need for voltage regulation and on-chip security is taking an important role in future integrated circuit designs.

Low-drop out (LDO) voltage regulators are the most popular architecture used in integrated circuits due to traditional practices of distributed voltage regulation on an integrated circuit. However, LDO based voltage regulator suffer seriously from power conversion efficiency and

---

1 This part of this section was published in IEEE Publications [70, 71]. Permission is included in Appendix A, Section A1
large circuit area and are prone to stability and reliability after manufacturing [53 - 55]. Process, voltage and temperature (PVT) changes further degrade the performance and reliability of the converters [56 - 59]. Digital control techniques have been proposed to improve efficiency of an LDO by controlling the quiescent operating current for low duty-cycle loads [60 - 63].

As an alternative to LDO, switching voltage regulators with inductive, capacitive filters have been proposed that can provide better efficiency at heavy load conditions and also provide an acceptable response time [64]. The switching regulator uses a set of switching power transistors whose switching time is controlled using a feedback signal based on power supply voltage variations due to loading conditions. The voltage variation at the output of the regulator due to load changes is converted to a time signal using a voltage to pulse width modulation conversion block.

![Figure 1.1 Inductive switching voltage regulator](image)

A typical circuit of an inductive switching voltage regulator is shown in Figure 1.1 [65, 66]. Inductance (L), capacitance (C) based filter are used to filter the high frequency components in the output to provide a low ripple DC voltage. The disadvantages are large size of inductors and capacitor based filter circuit on integrated circuits that limit the use of regulators at the point of load applications. The filter component (L/C) size are reduced by using higher operating frequencies, however the power consumption increases thus reducing the efficiency. Techniques have been proposed using multi-phase regulators that allow high frequency application with a reduced size of components providing an overall improved efficiency of the regulator [67]. Use of
resonant circuits allows operation at higher frequencies with a smaller inductance and capacitance with an improved efficiency [68]. Other techniques propose zero-voltage switching to enhance efficiency at higher frequency operation [69]. A hybrid regulator is proposed in [70, 71], that combines the characteristics of switching voltage regulator and LDO in the same design. The architecture of the regulator is shown in Figure 1.2.

![Figure 1.2 Hybrid voltage regulator](image)

The proposed regulator replaces the LC filter with a versatile active filter that has small on-chip foot-print. The proposed regulator presents a small area and high efficiency for on-chip implementation. The proposed regulator uses duty cycle block to adjust the switching time of the power transistors for voltage regulation. Other combinations of linear regulators (LDO) and switching voltage regulators have been proposed for enhancing performance and efficiency [72, 73]. Voltage regulation in a distributed on-chip grid requires an optimal allocation of LDO’s and decoupling capacitors to achieve high performance and efficiency [74].

As an alternative to LDO and inductive switched voltage regulator, the switched capacitor (SC) voltage regulator has been proposed as a method for on-chip voltage conversion and regulation. [75 - 77]. This regulator provides a flexible point of load voltage regulation method with a variety of circuit architectures and can be implemented easily on a chip in a small area compared to inductance capacitance based switched voltage regulator. The efficiency of typical LDO, switching voltage regulator and switching capacitor voltage regulators drops considerably
at light loads due to high quiescent current [78 - 80]. Although several techniques have been proposed to mitigate the problem of low efficiency in LDO regulators, switching voltage regulators and switched capacitor circuits, they all require an increased overhead of support circuits [81- 85]. Additionally, the regulator efficiency is further degraded by voltage conversion ratios. However, switched capacitor regulators have been found to be well suited to be configured to achieve improved efficiency under wide range of load conditions. The converter gating technique [84] is found to be more adaptable for on-chip application under varying load conditions, compared to other switched capacitor techniques that use duty cycle modulation techniques [85].

In order to provide a comprehensive voltage conversion and regulation, the complete power delivery network grid, on-chip, has to be taken into consideration. In a distributed load configuration on a chip, point of the load voltage regulator can provide an efficient solution. Switched capacitor converters have been configured and demonstrated to show a superior performance in distributed power grid network compared to LDO’s [84, 85].

Efficient analysis and design of the power distribution network on chip can assist with the proper selection and distribution of voltage regulators on chip [87, 88]. The power network noise and EMI produce effects that have to be taken into consideration for proper application and organization of voltage regulators in a distributed voltage and power management environment [86]. Emerging 3D integrated design methods for IC layout provide a challenging case for optimization of on-chip power distribution, voltage conversion and regulation and power noise reduction on a chip [89].

1.3 Voltage Regulators and On-chip Security Consideration

Power analysis attacks on integrated circuits in the form of side channel-attacks have become a preferred process by attackers to obtain information about circuit activity that leads to
deciphering the hidden signature in security circuits [90]. The attacks can come in many forms such as simple power consumption profiling [91, 92], differential power analysis attacks [93], and leakage power analysis attacks [94, 95]. Additional covert channel attacks have been recently identified [96]. Since the power supply network and point of the load voltage regulator circuit’s on-chip are directly connected to external power supply pins of a chip, voltage regulators provide a novel opportunity to implement circuit techniques to provide resistance against power profiling and other attacks on integrated circuits. Exploiting voltage regulators with additional enhancements to introduce measures that disturb the correlation between control and data flow on a chip and power consumption profile has been introduced recently to thwart power attacks [97 - 101].

1.4 Pulse Width Modulation

Pulse width modulation (PWM) is a method to change the duty cycle of a periodic signal. Pulse width modulated signals are widely used in voltage and power management circuits, in power amplification and control circuit and in class D audio amplification circuits [102 - 104]. The ability to vary the pulse width in a controlled manner and over a wide range of values is required for the aforementioned applications. In addition, the ability to control of period of a periodic signal while the duty cycle is varied is a desired characteristic for many applications. PLL based PWM circuits have been proposed in [105]. Other architectures have been proposed for PWM circuits in [106, 107]. Most of these circuit architectures suffer from large circuit area and limited stability under process voltage and temperature variations.
1.5 Motivation for a New PWM Architecture

By far the most noted applications of PWM is in the area of switching voltage regulators [108]. However, as noted above in section 1.2, the efficiency of the regulator drops considerably at light load conditions, the pulse frequency modulation (PFM) is applied to reduce the frequency and regulator losses at light load conditions [109]. Several architectures have been proposed that suffer from large area on the integrated circuits and unstable operation under process, voltage and temperature variations. A voltage controlled oscillator, a counter, a digital to analog converter, and a comparator are used as the building blocks of a PWM [110]. This counter based PWM requires additional clock and reference signals and therefore suffers from large power consumption. PWMs based on either a delay line multiplexor and a ring oscillator multiplexor are described, respectively, in [111] and [112] which consume less power but occupy a large chip area due to the large multiplexor circuits. PWMs based on a delay line multiplexor and a ring oscillator counter provides a means to control area/power tradeoffs [111]. Other architectures are based on analog techniques that require an analog comparator and a saw-tooth waveform generator [113, 114]. The PWM architectures used in the regulators [113, 114] provide a limited range of duty cycle adjustment, non-linearity in operation and, little or no control for compensation of circuit operation under a variety of operating conditions with varying load conditions. Several analog and digital work around methods have been proposed in literature to overcome the issues of control and non-linearity but require additional support circuits [115, 116].

To overcome the aforementioned weaknesses of the PWM, the proposed PWM circuit architecture in this work is developed and described in Chapter 2. The proposed architecture [66,

---

1 This part of this section was published in IEEE proceedings of ISCAS 2014, pp. 958–961, Melbourne Australia 2014, as “An enhanced pulse width modulator with adaptive duty cycle and frequency control”. Permission is included in Appendix A, Section A2.
117, 118] provides an external control capability with a fine granularity of duty cycle variations over 20%-90% with a small circuit implementation foot-print. The proposed method provides a facility to maintain duty-cycle and frequency of operation of the PWM with digital control. In addition, circuit techniques are used to achieve a stable PVT operation over a wide temperature, voltage and process varying conditions. The proposed PWM is implemented and verified with 22nm CMOS models [139].

1.6 Controlled Oscillator Circuit

The heart of the PWM is a controlled periodic signal source whose duty cycle and/or frequency is controlled based on application requirements. Free running oscillator are augmented with control circuits to generate and control periodic signals. Voltage controlled oscillators (VCOs) are primarily used in high performance integrated circuits for stable clock frequency generation and control with PLL circuits. Inductor-capacitor based (LC) can operate at high frequencies and exhibit low noise performance. Alternatively, ring oscillators occupy smaller area on a chip and exhibit a wide range of frequency tuning for variable frequency applications. Ring oscillators applications have been widely used in modern Integrated circuits [119, 120].

Most of the circuit designs of controlled ring oscillators have focused on applications in wireless domain, where frequency control and stability is of paramount importance. The main figure of merit (FOM) for comparisons is phase noise of the frequency source at the desired frequency of interest [120-122]. Due to the large variation of frequency of the typical conventional ring oscillator, the application of a ring oscillator is found in use as process, voltage and temperature sensor [123]. Temperature stable frequency source using traditional bandgap reference circuits has been reported in [124]. Other methods to achieve a PVT stable frequency source has been discussed in [125].
As referenced in above section, several works on PVT stable frequency sources are found in literature. However, the scope of work on the subject of PVT stable variable duty cycle and a stable frequency source is limited. The work described in Chapter 2 is focused on PVT stable controlled duty cycle and stable frequency source. This work has successfully reached new milestones over the last few years [66, 117, 118]. Details of the proposed PVT stable variable duty cycle, stable frequency source are described and demonstrated in detail in Chapter 2.

1.7 Hardware Security and On-chip Physical Unclonable Function

Hardware security encompasses a wide area of subjects that deal with authentication of systems and circuits, ensure protection and validity of information stored in integrated circuits, provide facility for validity authentication of users of a system and configure a hardware system for resilience against external attacks. Physical Unclonable Functions (PUF’s) are circuits that are implemented on integrated circuit chips for facilitating hardware security applications [126 - 128]. PUF’s provide facility to validate an IC chip as a valid IP from the digital signature produced by the PUF circuit. PUF’s are also used for generating cryptographic signatures that can be dynamically configured. PUF circuits exploit manufacturing process variations to create a random output response that is produced as a result of input stimuli. Statistical inference estimates of the circuits output responses, are used to provide the authentication information. The output response has to be reliable over temperature and supply voltage variations. A variety of PUF architectures have been proposed and explored over the years [129 - 131]. PUF circuits are compared with respect to each other based on a set of figures of merit [133]. The main challenges of on-chip PUF circuits are randomness, environmental reliability, circuit size and power consumption. Other issues under research are machine learning based attacks and other forms of attacks on the PUF [133, 134].
The proposed pulse width modulator developed in this research and demonstrated in Chapter 2, is designed to work as a duty-cycle based PUF primitive. With extensive analysis and simulation work, the duty-cycle based PUF is demonstrated to be superior to the state of the art implementations. The proposed PUF and the comparative Figures of merits (FOMs) with other state-of-the art implementations are described in detail in Chapter 3.

### 1.8 Organization

The dissertation is organized as follows. Chapter 2 describes the details of the novel PWM architecture, circuit features, capabilities and demonstrations with circuit simulation results. Chapter 3 describes the details of the proposed novel duty cycle based Physical Unclonable Function demonstrated with extensive analytical details and simulation results. Chapter 3, Section 3.11 and subsections describes the extension of the duty cycle based Physical Unclonable Function to an adaptable Physical Unclonable Function enhanced to provide additional duty cycle outputs with goal of enhancing the PUF entropy. Final comments are offered in Chapter 4 and extensions for future work are offered in Chapter 5. An extensive list of references are provided at the end.
CHAPTER 2:
NOVEL DIGITALLY CONTROLLED PULSE WIDTH MODULATOR

2.1 Introduction

A digitally controlled ring oscillator circuit can be adapted to control its duty cycle and frequency. Oscillators are circuits that are used to generate periodic waveforms of signals at their output based on circuit implementation characteristics. A variety of oscillator circuits have been developed over the years that are used to generate autonomously or semi-autonomously periodic waveforms. Inductance (L) capacitance(C) based voltage controlled oscillator circuits can be used to produce periodic signals, however they suffer from large circuit size and high power consumption. Conventional autonomous ring oscillators consist of a set of circuit blocks that are connected in a feedback mode of operation to provide a $2\pi$ phase shift that causes the circuit to oscillate and provide a periodic waveform at the circuit nodes. A simple implementation of a ring oscillator consists of using an odd number of inverters in a feedback loop as shown in Figure 2.1.

Figure 2.1 Conventional ring oscillator

---

This parts of this chapter was published in IEEE proceedings of ISCAS 2014, pp. 958–961, Melbourne Australia 2014, as “An enhanced pulse width modulator with adaptive duty cycle and frequency control” and in IEEE Transactions on VLSI Systems, Vol. 22, pp. 2527-2534, 2014, “Digitally Controlled Pulse width modulator for on-chip power management”. Permissions are included in Appendix A, Sections A2 and A3.
The number of inverters in the loop provide a delay that determines the frequency of the output waveform [135]. The supply voltage and circuit capacitance values can affect the circuit delay. Controlled oscillators use either the control of supply voltage or the current into the circuit to control the frequency of oscillation. The quality of the periodic waveform is measured in terms of frequency and phase noise and is a critical measure for applications that require low jitter and or low phase noise.

The duty cycle of a balanced ring oscillator is 50%. In addition to frequency the time phase relationship between time periods of the output high and low parts of a periodic output of the ring oscillator determines the duty cycle. The duty cycle of the ring oscillator is affected by the imbalance in the stage delay between odd and even inverter stages. For the case of inverter based ring oscillator, the delay of the inverter can be affected by either geometrical size variations, or supply voltage or current control from the supply voltage. The use of supply current provides a flexible and precise control of the delay of the inverter stages. The current control can be implemented with header and footer current source circuits and can be controlled with digital inputs. A novel method is proposed in this work to control the frequency and duty cycle of the ring oscillator with digital input controls. PVT variations affect the delay characteristics of the stages resulting in duty cycle variations. Several methods have been proposed to compensate the effects of PVT variations on the performance of sensitive analog circuits. A novel feedback mechanism is used to control the duty cycle and frequency of the ring oscillator under PVT variations.
A typical application of duty cycle controlled oscillator can be a Pulse width modulator (PWM). An application of PWM shown in Figure 1.1 is reproduced here in Figure 2.2 for an inductive switching DC-DC voltage regulator [65, 136].

![Figure 2.2 Inductive switching voltage regulator](image)

The pulse width modulated signal from (PWM) block is applied to pass transistors (M1, M2), providing a stable load current. LC filter provides a stable output voltage (Vout) at the output of LC filter. An ideal analysis of the circuit shown in Figure 2.2 is as follows [65]. The output voltage (Vout) is a sum of DC voltage and ripple component.

\[ V_{out} = V_{dc} + V_r(t) \]  

(2.1)

where, \( V_{dc} \) is the DC component and \( V_r(t) \) is the AC ripple component. For a duty cycle \( D \) and frequency \( f \) of the output signal of PWM, the voltage \( V_{dc} \) is

\[ V_{dc} = f \int_0^{1/f} V_n(t) \, dt = D \cdot V_{np} \]  

(2.2)

where, \( V_n(t) \) is the transient square wave voltage at the transistor outputs before the LC filter and \( V_{np} \) is the peak value of \( V_n(t) \).

The peak value of ripple voltage \( V_r(t) \), \( \Delta V_r \) above the DC voltage \( V_{dc} \) is given by

\[ \Delta V_r = \frac{(V_{np} - V_{out}) \cdot D}{16LC \cdot f^2} \]  

(2.3)

where \( L, C \) are the values of inductance and capacitance in the circuit, \( D \) is the duty cycle and \( f \) is the frequency of the PWM. Equation (2.2 and 2.3) show that the output voltage \( V_{dc} \) can be
regulated with the duty cycle $D$ of the PWM and the magnitude of ripple is a function of size of $L$, $C$ and the frequency of the PWM.

### 2.2 Controlled Ring Oscillator Architecture

An architectural level block diagram of the proposed circuit based on a ring oscillator is shown in Figure 2.3. The output of the ring oscillator $CLK$ is fed to the duty cycle to voltage converter (DC2V) block to generate a control signal. DC2V provides an analog control signal for the headers and footers to ensure a stable duty cycle under PVT variations. Digital control provides signals for the header and footer circuits to dynamically change the duty cycle and frequency of the ring oscillator. Details of individual blocks and operational aspects are described in the following sections.

![Block diagram of the pulse width modulator](image)

**Figure 2.3** Block diagram of the pulse width modulator

### 2.3 Ring Oscillator Topology

A seven stage ring oscillator is used for the proposed circuit is shown in Figure 2.4. The odd inverter stages 1, 3, 5, and 7 are connected to header circuit $I_a$ and footer circuit $I_c$. The even inverter stages 2, 4, and 6 are connected to header circuit $I_b$ and footer circuit $I_d$. An increase in the source current supplied to the ring oscillator by header $I_a$ or $I_b$ increases the current supplied to PMOS devices within the inverters, enhancing the pull-up capability and resulting in a faster rise time at the outputs.
Conversely, an increase of the sink current through the footer \( I_c \) or \( I_d \) increases the current through the NMOS devices of the inverters, enhancing the pull down capability and resulting in a faster fall time at the output. The relative increase or decrease in the source and sink currents therefore changes the duty cycle and frequency of the ring oscillator output.

An analysis of the effect of increasing and decreasing the current in the header and footer circuits is provided in Table 2.1.

Table 2.1 Duty cycle and frequency changes with header and footer currents.

<table>
<thead>
<tr>
<th>Header or Footer Current</th>
<th>Duty cycle</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_a )</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>( I_a )</td>
<td>↓</td>
<td>↑</td>
</tr>
<tr>
<td>( I_b )</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>( I_b )</td>
<td>↓</td>
<td>↓</td>
</tr>
<tr>
<td>( I_c )</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>( I_c )</td>
<td>↓</td>
<td>↓</td>
</tr>
<tr>
<td>( I_d )</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>( I_d )</td>
<td>↓</td>
<td>↑</td>
</tr>
</tbody>
</table>
2.4 Controlled Duty Cycle and Frequency Analytical Details

For a conventional ring oscillator shown in Figure 2.1, the period and duty cycle can be defined as follows

\[ P = T_{\text{high}} + T_{\text{low}} \]  
\[ D = \frac{T_{\text{high}}}{T_{\text{high}} + T_{\text{low}}} \]

where \( T_{\text{high}} \) = width of logic high part of the cycle and \( T_{\text{low}} \) equal to the width of logic low part of the cycle. For 50% duty cycle \( T_{\text{high}} = T_{\text{low}} = T_0 \) for conventional ring oscillator. Here we assume that the average current supply to the inverter stages is \( I_{\text{ave}} \) at 50% duty cycle.

To create a single period of oscillation, the signal traverses twice through the ring oscillator. This fact is clarified by tracing the signal transitions through the odd and even stages of the inverter. Consider a ring oscillator circuit shown in Figure 2.5 with \((2m+1)\) identical inverter stages. The \( I_{\text{bias}} \) current is supplied to NMOS transistors in \((m+1)\) odd stages while the remaining \( m \) stages are supplied by vdd.

![Figure 2.5 Typical (2m+1) stage ring oscillator circuit with header control](image)
The duty cycle and the period of oscillation can be described as

\[ T_{bias,high} = T_{bias} + T_{bias,affected} \]  \hspace{1cm} (2.6)

where \( T_{bias,high} \) is the new value of \( Thigh \). \( T_{bias} \) is the variation in the value of logic high time period due to current flowing into the PMOS devices of \( (m+1) \) odd inverters stages, while \( T_{bias,affected} \) represents variation in the logic high time period due to current flowing into the PMOS devices of \( m \) even inverters. Changes in \( I_{bias} \) affects \( T_{bias,high} \) as a result changes in values of \( T_{bias} \) thus changing the duty cycle and the frequency of the ring oscillator. For a given inverter stage the value of rise delay due to PMOS pull-up can be approximated to a first degree as the product of total output node capacitance, changes of output voltage and the average current flow through the PMOS device. Thus \( T_{bias} \) changes as a result of \( (m+1) \) stages can be approximated as follows

\[ T_{bias} = (m + 1)[C_g \Delta V_{out}/I_{bias}] \]  \hspace{1cm} (2.7)

where \( C_g \) is the gate load capacitance and \( \Delta V_{out} \) is the output voltage change, \( I_{bias} \) is average supply current.

In a conventional ring oscillator all \( (2m+1) \) stages are active and by analogy with (2.7) the delay \( T_0 \) due to \( (2m+1) \) stages can be written as follows

\[ T_0 = (2m + 1)[(C_g \Delta V_{out})/I_{ave}] \]  \hspace{1cm} (2.8)

Dividing (2.7) with (2.8) and defining \( \alpha = I_{bias}/I_{ave} \), we get

\[ T_{bias} = (m + 1)/(2m+1) \left[ \left( \frac{T_0}{\alpha} \right) \right] \]  \hspace{1cm} (2.9)
Now consider the case in which current to \( m \) even inverters is changed while current to odd inverters is kept constant. The corresponding impact on \( T_{bias,high} \) can be deduced in a similar manner as above as

\[
T_{bias,affected} = m / (2m + 1)[T_0/\alpha] \tag{2.10}
\]

Adding (2.9) and (2.10) yields, \( T_{bias,high} = T_0/\alpha \).

The duty cycle \( D \) can be expressed as

\[
D = T_{bias,high}/(T_{bias,high} + T_{low}) = 1/(\alpha + 1) \tag{2.11}
\]

In case the \( I_{bias} \) current is applied to \( m \) even inverters, it can be shown through an analysis as above that that the duty cycle \( D \) is given by, \((1-D) = 1/(1+ \alpha)\), which reduces to,

\[
D = \alpha/(1 + \alpha) \tag{2.12}
\]

From (2.11) it can further be deduced that the current ratio \( \alpha \) required to establish a duty cycle \( D \) can be obtained as

\[
\alpha = (1-D)/D \tag{2.13}
\]

Now consider the case in which two header circuits are used one (HA) supplying the odd inverters and the other (HB) supplying the even inverters as shown in Figure 2.6.

Figure 2.6 \((2m+1)\) stage ring oscillator with two headers
In this case the \( I_{bias,A} \) current is supplied to odd \((m+1)\) inverters changes the \( T_{high} \) period as described above, while the \( I_{bias,B} \) current to \( m \) even inverters affect the \( T_{low} \) period at the output. Performing an analysis similar to above for the one header case, the following expression can be deduced by analytical induction for the duty cycle and period changes for the ring oscillator with two headers.

\[
T_{bias,high} = \frac{T_0}{\alpha} \quad (2.14)
\]

\[
T_{bias,low} = \frac{T_0}{\beta} \quad (2.15)
\]

where

\[
\alpha = \frac{I_{bias,A}}{I_{ave}} \quad (2.16)
\]

\[
\beta = \frac{I_{bias,B}}{I_{ave}} \quad (2.17)
\]

The duty cycle and the period of oscillation is described with the following expressions

\[
D = \frac{T_{bias,high}}{(T_{bias,high} + T_{bias,low})} \quad (2.18)
\]

where \( D \) is the duty cycle. Substituting the values of \( T_{bias,high} \) and \( T_{bias,low} \) from equations (2.14) and (2.15), we have

\[
D = \frac{T_0/\alpha}{(T_0/\alpha + T_0/\beta)} = \frac{1}{(1 + \alpha/\beta)} \quad (2.19)
\]

and the period \( P \) can be expressed as

\[
P = T_{bias,high} + T_{bias,low} = T_0(1/\alpha + 1/\beta) \quad (2.20)
\]

From (2.17) it is clear that if we fix the period \( P = 2T_0 \) and evaluate,

\[
\beta = 1/(2 - 1/\alpha) \quad (2.21)
\]

gives the condition for constant period ring oscillator.
From (2.19), (2.20), and (2.21) the PWM frequency can be deduced as

\[ F_{\text{new}} = 2 \times (1 - D) \times F_0 \]  

(2.22)

where \( D \) is the duty cycle of proposed circuit, \( F_0 \) is the frequency of proposed circuit at \( D \) equal to 0.5, and \( F_{\text{new}} \) is the new frequency of the circuit. Substituting \( \beta \) from (2.21) into (2.19) gives

\[ \alpha = \frac{1}{2D} \]  

(2.23)

A similar analysis by calculating \( \alpha \) in terms of \( \beta \) gives

\[ \beta = \frac{1}{2(1-D)} \]  

(2.24)

Dividing (2.23) by (2.24) gives the relationship for current ratios \( I_{\text{bias},A} \) and \( I_{\text{bias},B} \) constant frequency ring oscillator for a given duty cycle \( D \).

\[ I_{\text{bias},A} / I_{\text{bias},B} = (1-D)/D \]  

(2.25)

Thus by adjusting the current ratios properly a constant frequency, variable duty cycle ring oscillator is obtained.

Now consider the case of ring oscillator with header and footer circuits as shown in Figure 2.4. Here \((m+1)\) odd stages are connected to header current source \( I_a \) and footer current source \( I_c \) and \( m \) even stages are connected to header current source \( I_b \) and footer current source \( I_d \).

Let \( I_A, I_B, I_C, I_D \) are the currents flowing through the headers \( I_a, I_b \) and footers \( I_c, I_d \) respectively. Analyzing this circuit for duty cycle and period in a manner similar to the 2 header circuit leads to the following results

\[ T_{\text{bias,high}} = T_0/\alpha \gamma \]  

(2.26)

\[ T_{\text{bias,low}} = T_0/\beta \delta \]  

(2.27)

where \( \alpha, \beta, \gamma \) and \( \delta \) are defined as.
\[ \alpha = I_A/I_{A5}, \beta = I_B/I_{B5}, \gamma = I_C/I_{C5}, \text{ and } \delta = I_D/I_{D5}, \] and \( I_A, I_B, I_C \) and \( I_D \) are the currents passing through, respectively, \( I_a, I_b, I_c, \) and \( I_d \). \( I_{A5}, I_{B5}, I_{C5}, \) and \( I_{D5} \) are the currents passing through \( I_a, I_b, I_c, \) and \( I_d \) respectively, to provide a 50% duty cycle.

The Duty cycle \( D \) and period \( P \) can be written as

\[ D = \left( \frac{T_0}{\alpha \gamma} \right) \left( \frac{T_0}{\alpha \gamma + T_0/\beta \delta} \right) \]  
\[ D = \frac{1}{\alpha \gamma} \left( \frac{1}{\alpha \gamma} + \frac{1}{\beta \delta} \right) \]  
\[ D = 1/(1+(\alpha/\beta)*(\gamma/\delta)) \]  
\[ P = T_0 \left( \frac{1}{\alpha \gamma} + \frac{1}{\beta \delta} \right) \]

Setting \( P = 2T_0 \), for constant frequency variable duty cycle ring oscillator we can write

(analysis similar to equation (2.21))

\[ \beta \delta = \frac{1}{2 \alpha \gamma} \]  

Equation (2.32) establishes exactly the relationship between current ratios \( \alpha, \beta, \gamma \) and \( \delta \) for a constant frequency ring oscillator for the circuit shown in Figure 2.4. When the header circuits and footer circuits are changed independently as in two header case, by analogy the following equations for current relationship can be established for a constant frequency ring oscillator.

\[ \frac{I_B}{I_A} = \frac{D}{1-D} \]  
\[ \frac{I_C}{I_D} = \frac{D}{1-D} \]

From equation (2.33) and (2.34), it is clear that by controlling and maintaining the current ratio of header and footer currents a constant frequency for the duty cycle can be maintained. A comparison of theoretical results expressed in (2.33) and (2.34), to maintain constant frequency are compared with circuit level simulations and are presented in Section 2.6.1.
2.5 Details of PWM Circuit Components

The circuit level details of the PWM blocks shown in Figure 2.3 are explained in the following sub-sections.

2.5.1 Duty Cycle to Voltage Converter

Figure 2.7 Simplified schematic of DC2V

The duty cycle to voltage converter (DC2V) has been adopted from [137]. A simplified diagram of the circuit is shown in Figure 2.7 and has the following cycles of operation. A high \(CLK\) input charges capacitor \(C_1\) from \(Vdd\) through transistor \(DM_0\). When \(CLK\) goes low, a high pulse \(P_2\) turns on \(DM_2\) transferring charge from capacitor \(C_1\) to \(C_2\). After \(P_2\) goes low while \(CLK\) is still low, \(P_1\) goes high and discharges \(C_1\) to ground through \(DM_1\). Resistor \(R_1\) and PMOS transistor \(DM_3\) establish the range of \(DC2VO_{Out}\) voltage. After a few cycles, the voltage on \(C_2\) stabilizes to a constant value. The output of DC2V “\(DC2VO_{Out}\)” is used as the input “\(dc2vin\)” in the header and footer circuits.

2.5.2 Header and Footer Current Sources

The circuit schematics for headers Ia, Ib, and footers Ic, Id are shown in Figures 2.8 and 2.9, respectively. Addition based current sources and sinks are proposed in [125] to ensure stable and robust current delivery under PVT variations.
A modified addition based current source has been used within the header circuit using PMOS transistors PM₀, PM₂, PM₃, and PM₄. PMOS transistors PM₅, PM₆, and PM₇ in series with PM₂, PM₃, and PM₄ respectively control the header currents with digital inputs bx₀, bx₁... bxₙ. A modified addition based current sink has been used within the footer circuit using NMOS transistors NM₁, NM₃, NM₄, and NM₅. NMOS transistors NM₆, NM₇ and NM₈ in series with NM₃, NM₄, and NM₅, respectively, control the footer currents with digital input by₀, by₁...byn. The analog input dc₂vin received from output of DC2V block provides current control for the header and footer circuits to maintain a constant current over a wide range of PVT variations. Under PVT variations, the bias voltage for transistors PM₂, PM₃, and PM₄ in the header circuit and transistors NM₃, NM₄, and NM₅ in the footer circuits respectively are adjusted to maintain current values that ensure a constant duty cycle for the circuit. Device PM₀₀ and resistor RN₁ within the footer circuits provide a level shift circuit for dc₂vin. Devices PM₀ and NM₁ within the header and footer circuits are configured as long channel devices as compared to other transistors within the header and footer circuits to mitigate leakage current variations [138].
2.6 Controlled Duty Cycle and Frequency Simulation Results

The proposed circuit has been implemented with 22 nm CMOS predictive technology model [139]. Simulation results of the circuit are compared with expressions defined in Section 2.4. Simulation results characterizing the performance of the proposed circuit are shown in Sections 2.6.1 and 2.6.2 respectively.

2.6.1 Digitally Controlled Variable Duty Cycle Ring Oscillator

Simulations of the circuit shown in Figure 2.3, performed over a wide range of duty cycle (20%-90%) by changing the digital control inputs. The results are compared with (2.30). Duty cycle versus normalized header and footer currents $\alpha$, $\beta$, $\gamma$, and $\delta$ are shown in Figure 2.10. Analytic and simulation results show good agreement within 5% of error.

![Duty cycle variation with header current IA, IB and IC, ID variation](image)

2.6.2 Digitally Controlled Constant Frequency Ring Oscillator

Described in Section 2.4, through analytical analysis, are the relations for header and footer currents under which the a constant frequency of ring oscillator can be maintained. Theoretical results are compared in this section with circuit simulation of the PWM. The ratio of the header currents $IB$ to $IA$ are changed to achieve a constant frequency of 1.66 GHz, over a wide range of duty cycles.
With reference to equation (2.33) and (2.34), the header current ratio $IB/IA$ versus duty cycle and frequency with and without frequency compensation are shown in Figure 2.11. Theoretical duty cycle and frequency plots based on (2.30) and (2.22) defined in Section 2.4 are also shown. The circuit simulation results are obtained with circuit implementation of the PWM with 22nm CMOS technology models.

![Figure 2.11 Constant frequency simulation and theoretical comparison](image)

### 2.6.3 PVT Compensated Ring Oscillator

The robustness of proposed circuit under PVT variations has been analyzed for a duty cycle range of 20%-90%. A circuit level simulation of the proposed two header and two footer circuit shown in architectural block diagram in Figure 2.3 with an implementation in 22nm CMOS node, over a wide range of process corners, temperature, and voltage values is demonstrated. The results of the duty cycle values are listed in Table 2.2. The results demonstrate a worst case error of less than 1% for duty cycle values between 50%-90% and less than 2% for duty cycle values between 20%-50%. The results demonstrate an improvement of duty cycle error, over PVT variations, as compared to implementation with two-header design, by the author, in [117].
Table 2.2 Duty cycle PVT variations

<table>
<thead>
<tr>
<th>P/V/T</th>
<th>Duty cycle (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT/1V/27</td>
<td>90.00 80.00 70.00 60.00 50.00 40.00 30.00 20.00</td>
</tr>
<tr>
<td>TT/1V/80</td>
<td>90.32 80.27 69.54 59.77 49.91 40.05 29.61 19.58</td>
</tr>
<tr>
<td>FF/1V/27</td>
<td>89.83 79.64 69.91 60.08 50.04 39.56 29.52 19.43</td>
</tr>
<tr>
<td>FF/1V/80</td>
<td>90.27 79.77 69.54 59.55 49.97 39.53 29.10 19.97</td>
</tr>
<tr>
<td>SS/1V/27</td>
<td>90.01 80.29 70.09 60.03 50.03 40.37 30.45 20.23</td>
</tr>
<tr>
<td>SS/1V/80</td>
<td>90.30 80.50 70.14 59.70 50.12 40.49 30.22 19.91</td>
</tr>
<tr>
<td>TT/0.9V/27</td>
<td>89.60 79.77 69.40 59.48 49.99 40.57 31.20 21.09</td>
</tr>
<tr>
<td>TT/0.9V/80</td>
<td>89.89 79.97 69.47 59.51 50.08 40.73 31.00 19.98</td>
</tr>
<tr>
<td>FF/0.9V/27</td>
<td>89.56 79.38 69.20 59.40 49.95 40.15 30.67 20.88</td>
</tr>
<tr>
<td>FF/0.9V/80</td>
<td>89.84 79.48 69.10 59.18 49.69 40.15 30.22 20.48</td>
</tr>
<tr>
<td>SS/0.9V/27</td>
<td>90.11 79.98 69.46 59.54 50.16 41.07 32.00 21.65</td>
</tr>
<tr>
<td>SS/0.9V/80</td>
<td>89.84 80.22 69.60 59.70 50.11 41.26 31.80 21.32</td>
</tr>
</tbody>
</table>

Process (P) SS= slow, FF= Fast, TT=Typical, Voltage (V) = 0.9V – 1V, Temperature (T) = 27 °C - 80 °C
Process parameters generated as specified in [138, 139].

2.7 PWM Performance Summary Comparisons

Performance comparison of the proposed circuit with state-of-the-art circuits is provided in Table 2.3. Proposed PWM is compared in terms of area, power, frequency of operation, and technology implementation node. The state-of-the art PWM implementations used for comparison have a wide range of applications and are listed in the references section of this work. As compared to other state-of-the art PWM implementations, the proposed circuit can be implemented in a small area and consumes significantly less power over a wide frequency range. As compared to other state-of-the-art PWM implementation, the proposed PWM also excels in other factors of performance that are described in Sections 1.4 and 1.5.
Table 2.3 PWM comparisons with other state-of-the art implementations.

<table>
<thead>
<tr>
<th>Design</th>
<th>Area</th>
<th>Power/Frequency</th>
<th>Technology (CMOS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[111]</td>
<td>5.52 mm²</td>
<td>10.5 uW / 330 KHz</td>
<td>0.60 um</td>
</tr>
<tr>
<td>[140]</td>
<td>1.00 mm²</td>
<td>11.2 mW / 1.25 GHz</td>
<td>0.13 um</td>
</tr>
<tr>
<td>[141]</td>
<td>1.20 mm²</td>
<td>19.2 mW / 2.45GHz</td>
<td>0.25 um</td>
</tr>
<tr>
<td>[124]</td>
<td>3.20 mm²</td>
<td>1.0 mW / 200 KHz</td>
<td>0.35 um</td>
</tr>
<tr>
<td>[142]</td>
<td>2.00 mm²</td>
<td>0.15 mW / 278 MHz</td>
<td>65 nm</td>
</tr>
<tr>
<td>This work*</td>
<td>0.6 mm²</td>
<td>0.2 mW (16uW DC) / 1.66 GHz</td>
<td>22 nm</td>
</tr>
</tbody>
</table>

Estimated area = device area x5, power = estimated using circuit simulation

2.8 PWM Conclusions

A digitally controlled PWM is designed that adaptively changes the header and footer current profiles to maintain a constant duty cycle under PVT variations. The circuit can adaptively control the duty cycle and the frequency at runtime. A DC2V converter and novel header and footer circuits are employed to achieve a stable duty cycle operation under PVT variation. The proposed footer and header circuits improve the error margin of duty cycle variations over a wide PVT range. The proposed PWM is flexible to be used in many applications that can leveraged by digital control. A major application of the proposed PWM in the area of hardware security as a controlled and reconfigurable physical unclonable function (PUF) is discussed in Chapter 3 of this work.
CHAPTER 3:
DUTY CYCLE BASED PHYSICAL UNCLONEABLE FUNCTION

3.1 Introduction

Physical unclonable functions (PUFs) are widely used as hardware security primitives to provide a unique signature [143] for device authentication and secret key generation. PUFs have been utilized as an alternative to improve the security of the secret hardware keys stored in non-volatile memory blocks in integrated circuits (ICs) that are potentially vulnerable to external attacks [126, 128, 144]. Additionally, PUFs offer dynamic circuit architectures that generate a device signature based on the random nature of circuit delay variations determined by the random manufacturing process variations as an alternative to fixed identification signatures stored within ICs [126, 127] [144]. A list of process parameter variations that may impact the delay and leakage characteristics of CMOS based digital circuits, and accordingly utilized in PUFs, is provided in [146, 147]. The two primary delay-based PUF topologies are the arbiter PUF and ring oscillator PUF (ROPUF) [126, 127]. An arbiter PUF provides a rich set of challenge and response pairs as compared to an ROPUF, but suffers from higher vulnerability to attacks such as the model development through machine learning techniques [150 - 157].

---

1 This chapter was published in IEEE Transactions [175]. Permission is included in Appendix A, Section A4.
Alternatively, a conventional ROPUF, as shown in Figure 3.1, utilizes a group of electrically and geometrically identical ring oscillators that are randomly distributed throughout an IC. The frequency of the oscillation is used for comparison to generate the output response bits which may suffer from reliability issues due to temperature and voltage variations [128, 145, 148, 149].

![Figure 3.1 Architecture of a conventional ring oscillator PUF](image)

Several techniques and algorithms have previously been proposed to ensure a distinct selection of frequency pairs with a separation that is greater than the noise threshold [158, 159]. A conventional PUF that allows direct user access is potentially vulnerable to man in the middle attacks [136]. A controlled PUF has been proposed in [160], where the PUF is used to generate random responses through a dedicated secure programming interface. The PUF challenges and responses are controlled through a secure CPU interface using one-way hash functions, isolating the PUF from a possible direct external attack by an adversary. An important requirement of a controlled PUF is the ability to accept digital inputs and produce random outputs bits. Typical applications of controlled PUF are explored in [160, 161].

A variety of reconfigurable PUFs have been proposed in [148, 156, 163, 164] to re-use PUF architecture for enhancing security either by increasing the number of challenge response pairs or enhancing the security against certain attacks with a new PUF configuration. Additionally, reconfigurable PUFs may also offer power consumption and speed trade-off [163, 164].
The proposed duty cycle based controlled PUF primitive can be used as a controlled and reconfigurable PUF. The controllability and reconfigurability properties of the proposed PUF is extensively studied both theoretically and with circuit analysis and simulations. The proposed PUF primitive provides the features of reconfigurable operation [165] that enables the generation of additional challenge response pairs, thus optimizing the area and enhancing security. The analysis of the proposed PUF primitive to demonstrate resistance to man-in-the-middle attacks [150-152], side-channel attacks [127, 153, 154] and fault injection attacks [155] is not in the scope of this work.

3.1.1 Contributions to PUF Work

The proposed controlled PUF primitive utilizes a ring oscillator with current-starved pull-up stages [93, 94]. This controlled ring oscillator generates a wide range of frequencies and duty-cycles with the digital control and is shown to be stable under process, voltage, and temperature (PVT) variations. The contributions to this work are based upon extensive circuit design enhancements to the prior work [66, 117, 118].

The novel contributions of this work are summarized as follows and are demonstrated with detailed mathematical analysis and extensive simulations. A duty cycle comparison based PUF primitive is proposed and demonstrated to be reliable over voltage and temperature (VT) variations. The proposed PUF primitive provides enhanced random duty cycle spread based on process variability and circuit features on the chip, and has a potential to provide an increased number of challenge/response pairs with negligible area and power overhead. The proposed PUF primitive may be digitally reconfigured to provide a new set of random duty cycle values.
3.1.2 Background Work Comparisons and Organization

Using the delay mismatch in ring oscillators as a basis to develop a duty cycle based PUF has previously been proposed in [162]. This technique relies on the mismatch of the transistor width-to-length ratio between inverter stages and uses 15 inverter stages in the ring oscillator for PUF implementation. Using a long chain of inverters in a ring oscillator produces a lower random statistical duty cycle spread and leads to higher power consumption and area due to the large MOS transistor widths as described in Section 3.2.1. The PUF proposed in [162], uses the duty cycle at the intermediate nodes of a mismatched inverter chain. The duty cycle values have a non-uniform intersecting temperature profile, which can result in low entropy and reduced reliability due to flip bit errors [128, 145, 149].

Alternatively, the proposed duty cycle-based PUF can be digitally configured to operate over a wide range of duty cycle values from 20%-90% with a high granularity and is demonstrated to provide a voltage and temperature (VT) stable output. Uniform sized seven inverter stages are incorporated in a circuit topology to amplify the statistical spread of random distribution of the duty cycle using a feedback circuit. The increased statistical variations of the duty cycle provide a wider range of distinct duty cycle values. The digital inputs are used to mitigate for the temperature and voltage variations. The current starved inverters enable a low power operation.

A detailed comparison between different PUF topologies that utilize either duty cycle or frequency is offered in Section 3.2. The redesign of prior work on PVT-stable pulse width modulator that is used as a foundation for implementing the proposed duty cycle PUF is described in Section 3.3. The proposed duty cycle based ring oscillator (DCRO) PUF primitive and the techniques to enhance the statistical duty cycle spread over process variations are explained with analytical and simulation results in Section 3.4. Section 3.5 presents the proposed PUF simulation
results. In Section 3.6 operation of the PUF in a reconfigured mode is presented with simulation results. In Section 3.7, quality figures of merits are evaluated and presented with simulation results for the proposed PUF scheme. In Section 3.8, a comparison of the proposed PUF with the state-of-the-art PUFs is provided. Derivation of equations used in previous sections are presented in Section 3.9. Duty cycle PUF conclusions are offered in Section 3.10. In Section 3.11 an enhanced version of the duty cycle based PUF that is adapted to exploit the use of duty cycle values at intermediate nodes of the PWM is presented.

3.2 Frequency versus Duty Cycle Based PUF

A conventional ring oscillator (RO) with $2m+1$ inverter stages, where $m$ is an even integer, is shown in Figures 3.2a) and 3.2b).

![Figure 3.2 Typical ring oscillator circuit](image)

(a)

![Figure 3.2 Typical ring oscillator circuit](image)

(b)

Figure 3.2 Typical ring oscillator circuit (a) Ring oscillator circuit with $(2m+1)$ inverter stages (b) Transistor level schematic of a $(2m+1)$ stage ring oscillator
For this ring oscillator, the total active high and low time periods of oscillation, $t_{ph}$ and $t_{pl}$ can be expressed, respectively, as

$$t_{ph} = \sum_{i=1}^{m+1} td_{f}(i) + \sum_{i=1}^{m} td_{r}(i)$$

(3.1)

$$t_{pl} = \sum_{i=1}^{m+1} td_{r}(i) + \sum_{i=1}^{m} td_{f}(i)$$

(3.2)

where $td_{f}(i)$ and $td_{r}(i)$ are, respectively, the fall and rise propagation delay of each inverter stage.

The results of the Monte Carlo simulations provide an insight into the upper and lower bound estimates of the device process parameters for the variability spread of frequency and duty cycle over the $\pm 3\sigma$ standard deviation.

A Monte Carlo analysis of the frequency and duty cycle of a ring oscillator is performed based on a set of Gaussian distributed inverter rise and fall times. The standard deviations of the inverter rise and fall times are obtained through Monte Carlo simulations using 22nm-LP CMOS predictive technology models (PTM) [139]. The models are extended to $\pm 3\sigma$ (6 sigma) FF (fast-fast) and SS (slow-slow) process corners and the corresponding Gaussian device parameter statistical models [139]. The standard deviations of the inverter rise and fall times obtained through 500 inverter samples are, respectively, 0.055 and 0.042, normalized over a mean value of 1.

### 3.2.1 Impact of Number of Inverter Stages

The reduction in the standard deviation of the frequency with larger number of ring oscillator stages has been addressed and discussed in [165]. The impact on the standard deviation of the duty cycle and frequency is examined by varying the number of inverter stages from three to thirteen for the corresponding values of $m=1$ to 6 using (3.1) and (3.2). Monte Carlo analysis of 10,000 samples of ring oscillators are performed using the inverter standard deviation values of 0.055 for the rise time and 0.042 for the fall time to obtain the standard deviation of the frequency and duty cycle.
The results are shown in Figure 3.3, which are scaled to the value of a three-stage ring oscillator.

![Figure 3.3 Standard deviation variations of the frequency and duty cycle with number of inverters](image)

The relative decrease in the standard deviation of the frequency is greater than that of the duty cycle when the number of stages increases. The decrease in the standard deviation of duty cycle and frequency is approximately 43% and 75%, respectively. The result suggests that using a smaller number of stages in an ROPUF can lead to higher variability.

The oscillation frequency of a ring oscillator is inversely proportional to the number of stages [145]. Assuming that each inverter stage has the same rise and fall times, the frequency of oscillation of a five-stage and seven-stage oscillator is, respectively, reduced by approximately 60% and 40% as compared to the frequency of a three-stage ring oscillator. Although, three- and five-stage ring oscillators are smaller in area, a higher frequency of operation may require on-chip shielding techniques that would increase the area and power consumption [166]. A seven-stage ring oscillator is therefore used in this work.

**3.2.2 Impact of Inverter Rise and Fall Time Variance**

Using (3.1) and (3.2), the standard deviation of frequency and duty cycle are determined as a function of the standard deviation of rise time of an inverter stage. A Monte Carlo analysis of duty cycle and frequency is performed using 100,000 Gaussian samples of rise time delay for each inverter stage. The standard deviation of the rise time of an inverter stage is changed from 0.055 to 0.9 over uniform steps with a mean value of 1. The standard deviation of the fall time is 0.042
with a mean value of 1. The results are shown in Figure 3.4. The standard deviation of the duty cycle increases more than the frequency with an increase in the standard deviation of the rise time of the inverter stages.

![Figure 3.4 Standard deviation variations of the duty cycle and frequency of the ring oscillator under varying standard deviations of the inverter rise time](image)

### 3.2.3 Improving Duty Cycle Spread Over Process Corners

Increasing the standard deviation of the rise and fall delay mismatch between the inverter stages, leads to a higher standard deviation of the duty cycle compared to a matched ring oscillator, as explained in Section 3.2.2. Assuming a Gaussian distribution for the duty cycle, the increase in the standard deviation of the duty cycle corresponds to an increase in the spread between the upper and lower bounds of (±3σ), SS (slow) and FF (fast), process corner limits. The increased duty cycle spread over the process corners reduces the probability of intersection of duty cycle values under voltage and temperature variations, thus improving reliability. The hypothesis is demonstrated with ideal Monte Carlo simulation of the ring oscillator for a modified periodic delay model presented in (3.1) and (3.2) respectively. The standard deviation of the rise time of an inverter stage is 0.055 with a mean value of 1. The standard deviation of the fall time is 0.042 with a mean value of 1. A seven-stage ring oscillator based in ideal inverters delay with Gaussian delay distribution spread is used for the Monte Carlo analysis.
When the rise delay is mismatched by a factor of $k_1$ for FF corner and fall delay is mismatched by a factor of $k_2$ for SS corner, (3.1), (3.2) and the corresponding duty cycle and frequency, spread, $DS$ and $FS$ respectively, in terms of duty cycle $D$ and frequency $F$ can be written as

$$tpl_{ff} = 4 \times tdr_{ff}(k1) + 3 \times tdf_{ff}$$  \hspace{1cm} (3.3) \\
tph_{ff} = 4 \times tdf_{ff} + 3 \times tdr_{ff}(k1)$$  \hspace{1cm} (3.4) \\
tpl_{ss} = 4 \times tdr_{ss}(k2) + 3 \times tdf_{ss}$$  \hspace{1cm} (3.5) \\
tph_{ss} = 4 \times tdf_{ss} + 3 \times tdr_{ss}(k2)$$  \hspace{1cm} (3.6) \\
$$DS = D_{ss} - D_{ff}$$  \hspace{1cm} (3.7) \\
$$FS = F_{ss} - F_{ff}$$  \hspace{1cm} (3.8)

where the subscripts $ff$ and $ss$, respectively, refer to FF and SS corner. For $k_1=1.0$ and $k_2$ variation from 1.0 to 2.0 in (3.3), (3.4), (3.5), and (3.6), the variation of the duty cycle and frequency spread between SS and FF corners (i.e., $DS$ and $FS$) is shown in Figure 3.5.

Figure 3.5 Frequency and duty cycle spread versus rise time spread

The duty cycle spread increases considerably whereas the frequency spread reduces as the delay mismatch increases over the process corners. The rapid increase in the duty cycle spread of ring oscillator over FF and SS corners suggests that the mismatched ring oscillator can provide a higher entropy of duty cycle values at the output that can be used to develop a large set of challenge response pairs compare to a frequency comparison based PUF.
3.2.4 Mismatched RO Circuit Analysis and Simulation Results

The circuit simulation of a seven-stage ring oscillator with the width and length ratio of the PMOS transistors for even stages set to be 7x compared to the transistors in odd stages is performed over SS and FF corners. The results are shown in Figures 3.6 a) and b) for the supply voltage variations from 0.9V to 1V at 27°C and in Figures 3.6 c) and d) for the temperature variations from 0°C to 100°C at 0.95V.

![Figure 3.6 Duty cycle variations versus voltage and temperature with a) no mismatch and b) mismatch c) no mismatch and d) mismatch](image)

As compared to a ring oscillator with equal width to length ratio for all transistors, a 4% higher duty cycle spread (DS) can be achieved. An improved voltage and temperature reliability is achieved for mismatched ring oscillator with non-intersecting curves for SS and FF corners.

![Figure 3.7 Mismatched RO circuit output duty cycle histogram](image)

The results of Monte Carlo circuit simulations of 200 mismatched ring oscillator samples at 0.95V and 25°C is shown in Figure 3.7 where a standard deviation of 0.514% with a mean value
of 75.3% is observed. The standard deviation of the duty cycle is enhanced additionally using dynamic control techniques proposed in Sections 3.4.1, 3.4.2, 3.4.3, and 3.4.4.

### 3.3 Prior Relevant Work

A digitally controlled pulse width modulator (PWM) with a current starved ring oscillator described in Chapter 2 is tailored as the duty cycle-based PUF primitive. The details of the architecture of the PWM are provided in Chapter 2. An analytical basis for modifying and using PWM as a PUF primitive is offered in Section 3.3.1.

#### 3.3.1 Duty Cycle Sensitivity Analysis

The relationship between duty cycle and header currents from (2.19) is expressed as

\[
D = \frac{1}{(1 + \alpha/\beta)}
\]

(3.9)

Mathematical analysis of the sensitivity of the duty cycle with respect to currents \(i_x\) and \(i_y\), provides a basis to achieve the goals for the proposed circuit to be used as a PUF. Taking partial derivative of the duty cycle \(D\) with respect to \(i_x\) and \(i_y\) and simplifying the results

\[
\Delta D = \frac{1}{i_y(1 + (i_x/i_y)^2)} \left\{(i_x/i_y) \Delta i_y - \Delta i_x\right\}
\]

(3.10)

\[
\Delta D = \frac{1}{i_x(1 + (i_y/i_x)^2)} \left\{\Delta i_y - (i_y/i_x) \Delta i_x\right\}
\]

(3.11)

where, \(\Delta D\) is the change in duty cycle as a result of changes \(\Delta i_x\) and \(\Delta i_y\) in current \(i_x\) or \(i_y\) respectively. Details of the derivation are shown in Section 3.9.1.

From (3.10), if \(\Delta i_y\) is not changed then the change in duty cycle \(\Delta D\) is proportional to \(\Delta i_x\) scaled by a factor depending on the \((i_x/i_y)\) ratio and the absolute value of \(i_y\). The scaling factor has a maximum value of 1 if \((i_x/i_y)\) is small as compared to 1 and \(i_y\) is close to 1. To achieve a small \((i_x/i_y)\) when \(i_y\) is equal to 1, \(i_x\) has to be close to 0. Under these conditions, the changes in \(D\) are proportional to the change in \(i_x\), \((-\Delta i_x)\). A small \((i_x/i_y)\) implies that the duty cycle \(D\) is
large relative to 50% value. For the circuit shown in Figure 8, the value of current coming from X is a small fraction of current coming from source Y for achieving a high duty cycle variability. A similar analysis of (3.11) leads to the conclusion that the value of current coming from Y is a small fraction of current coming from X for obtaining high duty cycle variability.

3.4 Proposed Duty Cycle PUF Circuit Architecture

The circuit architecture of PWM, shown in Figure 3.8, is designed to implement the proposed controllable and re-configurable PUF and is shown in Figure 3.9.

---

3.4.1 Headers X and Y

Headers X and Y are made up of geometrically mismatched and matched branches. The mismatched and matched branches are made up of transistors with different width to length ratios. The mismatched header branches for X and Y are turned on in a mutually exclusive manner for PUF configuration and operation.
The rest of the circuit behaves similar to PWM described in Chapter 2. The proposed PUF circuit is dynamically configured to produce a wide range of random duty cycle values at its output using digital control and feedback signal from Duty cycle to Analog Converter (D2A) block.

The circuit schematic of the header current source is shown in Figure 3.10 for \((n+1)\) branches, where \(n\) is a positive integer. The circuit is designed and configured to achieve the following goals.

1) Provide a uniform dynamic control of output current supplied to the odd and even inverter stages with digital control.

2) Amplify the output current variation spread over FF and SS process corners.

3) Achieve reliable current control operation over a wide range of mismatched circuit sizes.

![Figure 3.10 Digitally controlled current source](image)

### 3.4.1 Header Current Source Variability Analysis

The header current source shown in Figure 3.10 is designed to provide a uniform dynamic control with a minimum current variation over FF and SS process corners, temperature, and supply voltage variations [93, 94]. For a PUF application, the circuit is designed to provide an amplified variation of the current at the source output. The details of the work to achieve goals 2) and 3) using the new current source shown in Figure 3.10 are described in this section and Sections 3.4.2,
3.4.3 and 3.4.4. The new circuit operates in a similar manner as the PWM with widely different output characteristics.

Detailed mathematical analysis to determine the conditions to enhance the entropy of the duty cycle under statistical variations in the device model parameters and circuit operating conditions is presented. In Figure 3.10, transistors $P_5, P_7, P_9, \ldots P_{n+3}$ operate in saturation region when digital inputs $bx0 \ldots bxn$ are turned on. Transistors $P2, P4, P6, \ldots P_n$ are biased to operate in linear region using transistor $P_0$ and resistor $RPI$ and input signal from $D2A$. The total current $I$ flowing through output port $Outp$ is

$$I = I_0 + I_1 + I_2 + I_3 + \cdots + I_n$$ (3.12)

where $I_0, I_1, I_2, I_3 \ldots I_n$ are currents flowing through transistors $P_5, P_7, P_9, \ldots P_{n+3}$ respectively, when $bx0, bx1, bx2, \ldots bxn$ are set to active. The total variation of current $\Delta I$ at output port $Outp$ will be the sum of the variation for each component in $I$ and is

$$\Delta I = \Delta I_0 + \Delta I_1 + \Delta I_2 + \Delta I_3 + \cdots + \Delta I_n$$ (3.13)

where, $\Delta I_0$ is the total variation in current $I_0$ and $\Delta I_1$ is the total variation of current $I_1 \ldots$ and $\Delta I_n$ is the current variation in $I_n$.

The total variation of branch current $\Delta I_0$, through transistors $P_2$ and $P_5$, is due the combined effect of random variations of model parameters, restricted to mobility and threshold voltage, and to the source to gate voltage is expressed as

$$\Delta I_0 = \left[ (-2\sqrt{I_0} - I_0) \Delta vth + 2 \frac{\Delta \beta}{\beta} I_0 + [2\sqrt{I_0} \sqrt{\beta} \Delta vsg_{p5} + I_0 \Delta vsg_{p2}] \right]$$ (3.14)

where $\Delta vth$ is the change in device threshold voltage, $\Delta \beta$ is the transconductance factor changes due to device mobility, $\Delta vsg_{p5}$ and $\Delta vsg_{p2}$ are respectively, source to gate voltages on transistor $P_5$ and $P_2$. Details of derivation are shown in Section 3.9.2
From (3.14), the variation in $\Delta I_0$ due to transistor process parameters threshold voltage and mobility variation, $\Delta I_{0(p)}$ is

$$\Delta I_{0(p)} = (-2\sqrt{I_0 - I_n})\Delta vth + 2 \frac{\Delta \beta}{\beta} I_0$$  \hspace{1cm} (3.15)

The variation in $\Delta I_0$ due to source gate voltage $\Delta vsg_{p5}$ and $\Delta vsg_{p2}$ respectively $\Delta I_{0(vsg)}$ in (3.16) is

$$\Delta I_{0(vsg)} = 2\sqrt{I_0} \Delta vsg_{p5} + I_0 \Delta vsg_{p2}$$  \hspace{1cm} (3.16)

For identical header branches, the cumulative variation of output current $I$, $\Delta I$, for the header with $(n+1)$ branches is

$$\Delta I = \sum_0^n(-2\sqrt{I_n - I_n})\Delta vth + 2 \frac{\Delta \beta}{\beta} I_n) + \sum_0^n(2\sqrt{I_n}\Delta vsgs_{P(n+3)} + I_n \Delta vsg_{P_n})$$ \hspace{1cm} (3.17)

3.4.2 Mismatched Header Current Source Analysis

Referring to current source in Figure 3.10, (3.9), and (3.16) the variation of the source to gate voltage on transistor $P_2$ amplifies the current variation $\Delta I$ and correspondingly the duty cycle variation at the output. The amplified current variation allows a method to develop a circuit with a higher duty cycle variation over process corners and correspondingly a high duty cycle spread of random values at the PUF output.

Designating transistor $P_2$ in Figure 3.10 as $P_{2x}$ and $P_{2y}$ respectively and the transistor $P_5$ as $P_{5x}$ and $P_{5y}$ for header $X$ and $Y$ shown in Figure 3.9. The transistors $P_{5x}$ and $P_{5y}$ are mismatched for their width to length ratio to produce source to drain voltage mismatch.
Under these conditions, the ratio of the current flowing through transistor $P_{2x}$ and $P_{2y}$, operating in linear region, is

$$\frac{I_{P_{2x}}}{I_{P_{2y}}} = \frac{\left[\left(\frac{v_{sg} - v_{th}}{v_{sd_{y}}}\right)\left(\frac{1}{K}\right) - \left(\frac{1}{2K^2}\right)\right]}{\left[\left(\frac{v_{sg} - v_{th}}{v_{sd_{y}}}\right)^{-1/2}\right]}$$ \hspace{1cm} (3.18)

where $I_{P_{2x}}$ and $I_{P_{2y}}$ are the currents flowing through transistors $P_{2x}$ and $P_{2y}$ respectively, $v_{sd_{y}}$ is the source to drain voltage of transistor $P_{2y}$, and $v_{sd_{x}}$ is the source to drain voltage of transistor $P_{2x}$, $K = (v_{sd_{y}}/v_{sd_{x}})$ is the mismatch factor, $v_{sg}$ and $v_{th}$ are transistor source gate and threshold voltage respectively. Details of derivation are shown in Section 3.9.3. For $P_{2x}$ and $P_{2y}$ operating in the linear region, i.e $\left[(v_{sg} - v_{th})/v_{sd_{y}}\right] \geq 1$, the maximum value for (3.17) is

$$\text{Max} \left|\frac{I_{P_{2x}}}{I_{P_{2y}}}\right| = \frac{\left[\left(\frac{1}{K}\right) - \left(\frac{1}{2K^2}\right)\right]}{0.5}$$ \hspace{1cm} (3.19)

For large $K$, (3.19) reduces to $(2/K)$ and for small $K$ it approximates to $(1/K^2)$. Since the duty cycle has a reciprocal relationship with the ratio of currents $(I_{P_{2x}}/I_{P_{2y}})$, the duty cycle varies as a square law for small $K$ values and linearly for large $K$ values seen from (3.18). For large values of $K$, duty cycle converges to maximum value between 90% – 100%. Using (3.9), (3.18), and (3.19), the variation of duty cycle with factor $K$ is shown in Figure 3.11.

![Figure 3.11 Variation of duty cycle with source drain mismatch factor K](image-url)
3.4.3 Duty Cycle Spread Enhancement with Source Gate Voltage

The upper and lower limits of the current ratio expressed in (3.18), under process corner conditions, is determined by the upper and lower limits of threshold voltage variations over process corners, value of $K$, and source gate voltage of transistors $P_{2x}$ and $P_{2y}$. In order to achieve high duty cycle spread over process corners, the difference of the ratio of currents expressed in (3.18) has to be maximized over the SS and FF corners. Designating $(IP_{2xf}/IP_{2yf})$ as the ratio expressed in (3.19) under FF corner and $(IP_{2xs}/IP_{2ys})$ under SS corner respectively, the conditions for maximizing duty cycle spread is

$$DS = Max \left\{ \left( IP_{2xf}/IP_{2yf} \right) - \left( IP_{2xs}/IP_{2ys} \right) \right\}$$

(3.20)

where $DS$ represents the maximized duty cycle spread over FF and SS corners. Substituting (3.17) in (3.19) for FF and SS corner the simplified result is

$$DS = Max \left\{ \left[ \frac{(v_{sgf}-v_{thf})}{v_{sdys}} \right] \left( \frac{1}{K} \right) - \left( \frac{1}{2K^2} \right) \right\}$$

(3.21)

where, the subscript $f, s$ refer to FF and SS corner respectively. Assuming that the source drain voltages $v_{sd_y}$ is approximately kept constant under process varying conditions, for a large value of $K$, inspection of numerators and denominators in (3.21), shows that either a large value of $v_{sgf}$ compared to $v_{thf}$ and simultaneously, a small value of $v_{sgs}$ close to $v_{ths}$ or vice versa ensures that $DS$ is maximized. The impact of changes on duty cycle spread for various combinations of $v_{sgf}$ and $v_{sgs}$ using (3.21) and a circuit simulation of Figure 3.9, over SS and FF process corners is shown in Figure 3.12. Shown in Figure 3.12 a), b) are theoretical results using (3.20) and shown in Figure 3.12 c), d) are simulation results for various values of mismatch factor $K$. 

46
Duty cycle spread between SS and FF process corners is amplified from 4% to 10% with the appropriate selection of source gate voltage $v_{sg}$ for the headers transistors $P_{2x}$, $P_{2y}$ and the source drain voltage mismatch factor $K$.

![Figure 3.12](image)

Figure 3.12 Impact of source gate voltage $v_{sg}$ and $K$ on duty cycle spread. a) Theory - low $v_{sg}$ impact b) Theory - high $v_{sg}$ impact c) Simulation - low $v_{sg}$ impact d) Simulation - high $v_{sg}$ impact

### 3.4.4 Proposed PUF Environmental Stability Enhancement

For a reliable operation of a PUF, the duty cycle of PUF under SS and FF process conditions should not become equal over the designed temperature and voltage range and stay distinctly separated to avoid flip bit error [128, 145]. Defining the following factors from (3.21) as $G$ and $H$, where

$$G = \left( \frac{v_{sg} - v_{th}}{v_{sd, yf}} \right)$$  \hspace{1cm} (3.22)

$$H = \left( \frac{v_{sgs} - v_{ths}}{v_{sd, ys}} \right)$$  \hspace{1cm} (3.23)

Assuming that the denominator in (3.22) and (3.23) $(v_{sd, yf}, v_{sd, ys})$ is approximately equal over process conditions, by selecting appropriate value of $K$, the values of $G$ and $H$ are determined by numerators. The value of $K$ is chosen such that both quantities $G$, $H$ are greater than one and that one quantity is significantly different from the other. The values of source to gate
voltages $v_{sgf}$ and $v_{sgs}$, in (3.22) and (3.23) are set-up to ensure that the duty cycle monotonically increases or decreases and is significantly different to produce a wide spread over the operating temperature and voltage range.

### 3.5 Proposed PUF Simulation Results

Following the guidelines in previous subsections, a PUF circuit is implemented with 22nm CMOS. A circuit simulation of proposed PUF over SS and FF corners is performed. Results are shown in Figure 3.13 a) for supply voltage of 0.95V and over a temperature between 0°C-100°C and in Figure 3.13 b) over supply voltage between 0.9V-1V at a temperature of 25°C respectively. The duty cycle spread over process corners is as high as 10% over the temperature and voltage ranges.

![Figure 3.13 PUF circuit simulation](image)

Figure 3.13 PUF circuit simulation a) duty cycle versus temperature b) duty cycle versus supply voltage

Results of Monte Carlo simulation of 200 instances of the proposed PUF circuit, at 0.95V and 25°C are shown in histogram plot in Figure 3.14. A standard deviation of 0.95% at a mean value of 36% is observed. The standard deviation increases approximately by a factor of two compared to simulation result of mismatched ring oscillator without feedback shown in Figure 3.14.
Utilizing a scheme for digital compensation, the proposed PUF circuit is configured to provide a stable standard deviation over temperature and supply voltage variations. The digital inputs are configured to control the current ratio of the header current source $X$ and $Y$ to establish a stable and reliable duty cycle standard deviation over temperature and supply voltage variation. Monte Carlo circuit simulation of 100 samples of the circuit is performed between 0°C-100°C, 0.95V and 0.9V-1V, 25°C respectively. The reliability of standard deviation of duty cycle is compared with the reference value of 100% at nominal conditions of 0.95V supply voltage, 25°C temperature.

The results are shown in Figure 3.15 a) and b), respectively, for un-compensated and digitally compensated PUF circuit. The compensated PUF circuit has a duty cycle standard deviation reliability greater than 95% over the specified temperature and voltage range.
3.6 Reconfigurable PUF Operation and Simulation

The proposed PUF can be used as a re-configurable PUF [166]. A new PUF configuration is formed when the header current source X and Y, in Figure 3.9, for mismatched and matched branches are swapped with digital control. The resulting reconfigured PUF generates a different response output bit pattern. The duty cycle response over temperature and supply voltage variations, under SS and FF corners with the mismatch header current sources X and Y are swapped digitally, is shown in Figure 3.16 a) and b) respectively. The duty cycle spread of the reconfigured PUF has a maximum of 10% spread over temperature and supply voltage variations. The increased duty cycle spread ensures an increased entropy level and a reduced possibility of flip-bit errors thus increasing the PUF reliability.

![Figure 3.16 Re-configured PUF circuit simulation a) duty cycle versus temperature b) duty cycle versus supply voltage](image)

The inter-configuration PUF metric ($I_C$) defined in [166] to compare different PUF configurations is defined as

$$I_C = \frac{1}{c(c-1)} \left[ \sum_{s=1}^{c} \sum_{t=0, s\neq t}^{c-1} \frac{Hamm_d(U_s, U_t)}{(r-1)} \right] \times 100 \tag{3.24}$$

where $c$ is number of configurations, $r$ is the number of response bits, and $Hamm_d(U_s, U_t)$ is the Hamming distance between configurations $s$ and $t$. Monte Carlo circuit simulations of two PUF
configurations producing 200 response bits at nominal conditions of 0.95V and 25°C are performed. The corresponding $I_C$ value determined with (3.24) is 40%.

### 3.7 PUF Qualitative Characteristics and Measures

The details of the implementation of the challenge response pair generation logic is shown in Figure 3.17. The challenge is the selection of the multiplexer bits that are used to determine the pairs of duty cycle controlled ring oscillator (DCRO) PUF primitives for duty cycle comparison. The duty cycle comparison is accomplished with counters that generate response bits. The digital inputs of the header current are dedicated to control and configure the PUF. Monte Carlo statistical circuit simulations of proposed PUF circuit are performed using 22nm PTM statistical models to measure the qualitative figures of merits.

![Figure 3.17 Duty cycle controlled PUF challenge response blocks](image)

**Figure 3.17** Duty cycle controlled PUF challenge response blocks

#### 3.7.1 Uniqueness

The average inter-die Hamming distance measured as a percentage value, called uniqueness $R$, of the proposed PUF over $n$ instances is calculated as [169].

$$ R = \frac{2}{n(n-1)} \left[ \sum_{x=1}^{x=(n-1)} \sum_{y=(x+1)}^{y=n} \frac{\text{Hammd}(U_x, U_y)}{nb} \right] \times 100 $$  \hspace{1cm} (3.25)

where, $n$ is the number of PUF instances, $U_x$, $U_y$ are output response vectors for PUF instance number $x$ and $y$, $\text{Hammd}$ is the Hamming distance function, and $nb$ is the number of PUF response bits. Monte Carlo simulations on $n=12$ instances of the proposed PUF at nominal conditions of
supply voltage of 0.95V, temperature of 25°C, \( nb = 200 \) response bits gives a uniqueness value of 49.3%.

### 3.7.2 Reliability

Reliability of the proposed PUF under temperature and voltage variations is determined by estimating the bit error rate (BER) of output response bit pattern. The BER and percentage reliability \( R_b \) is calculated as [167].

\[
R_b = 1 - BER = 1 - \left( \frac{1}{m} \sum_{y=1}^{m} \frac{Hammd(U_x, U_{xy})}{nb} \right) \times 100
\]

(3.26)

where, \( U_x \) is the response of the PUF under nominal operating conditions, \( m \) is the number of times the challenge is repeated on an instance of the PUF other than nominal conditions, \( U_{xy} \) is the response of PUF under other than nominal operating conditions, \( Hammd \) is the Hamming distance function, and \( nb \) is the number of bits in the response.

Monte Carlo statistical simulations performed on the proposed PUF circuit over a temperature range of 0°C-100°C with 5°C increments at 0.95V supply voltage for \( nb=200 \) bit response with same challenge to determine the temperature reliability. The results are shown in Figure 3.18 a). The proposed PUF is more than 92% reliable over the operating temperature range of 0°C-100°C.

![Figure 3.18 a) Temperature reliability b) Supply voltage reliability](image)

Supply voltage reliability is determined by performing Monte Carlo simulation at 25°C temperature, a voltage range of 0.9V-1V, with 0.025V increments for \( nb=200 \) bit response, with
the same challenge. The results are shown in Figure 3.18 b). The proposed PUF supply voltage reliability is greater than 96% over the operating voltage range.

**3.8 PUF Quality Measures Comparisons**

A comparison of the proposed PUF with the state of the art PUF implementations reported in literature for the characteristics of uniqueness, reliability, power consumption and circuit area is presented in Table 3.1. The comparison is limited to PUF circuits implemented on integrated circuits. In the absence of actual layout implementation for a chip design, the layout area estimate of the proposed PUF is based on area of number of devices in a typical architectural description shown in Figure 3.9 with an added overhead of 3 times the area allocated for interconnects and placement of circuit blocks in a typical IC layout. The area is estimated to be 15 μM². A power consumption estimate of the proposed PUF is based on transistor level simulation of an instance of circuit architecturally represented in Figure 3.9. The power consumption of the proposed PUF is determined based on the average current consumption that is determined with transistor level simulations represented in Figure 3.9. The estimated power consumption is 3.75 μW. Please note that the estimated power consumption and area for each design in Table 3.1 is ideal-scaled to 22nm CMOS technology to provide a fair comparison [173, 174]. The proposed design provides reliable operation over a wide range of temperatures and supply voltages.
Table 3.1 Proposed PUF comparisons with other state-of-the art on-chip PUF implementations.

<table>
<thead>
<tr>
<th>Design</th>
<th>R</th>
<th>TRB⁰</th>
<th>VRB⁰</th>
<th>P/(Pₙ)</th>
<th>A/(Aₙ)</th>
<th>Te</th>
</tr>
</thead>
<tbody>
<tr>
<td>[168]</td>
<td>50.42</td>
<td>98.25</td>
<td>97.22</td>
<td>32.3/(3.7)</td>
<td>250/(28.6)</td>
<td>65</td>
</tr>
<tr>
<td>[169]</td>
<td>51</td>
<td>85</td>
<td>92</td>
<td>134/(32)</td>
<td>N/A</td>
<td>45</td>
</tr>
<tr>
<td>[170]</td>
<td>50.11</td>
<td>97.8</td>
<td>97.8</td>
<td>N/A</td>
<td>825/(12.3)</td>
<td>180</td>
</tr>
<tr>
<td>[171]</td>
<td>49.5</td>
<td>97.2</td>
<td>N/A</td>
<td>N/A</td>
<td>58.8/(6.73)</td>
<td>65</td>
</tr>
<tr>
<td>[128]</td>
<td>46.15</td>
<td>99.5⁰</td>
<td>99.5⁰</td>
<td>N/A</td>
<td>N/A</td>
<td>90</td>
</tr>
<tr>
<td>[162]</td>
<td>49.8²</td>
<td>95</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>40</td>
</tr>
<tr>
<td>TW</td>
<td>49.3</td>
<td>92</td>
<td>96</td>
<td>3.75³</td>
<td>15⁴</td>
<td>22</td>
</tr>
</tbody>
</table>

R = Uniqueness %age, TRB = Temperature Reliability percentage, VRB = Voltage Reliability percentage, P = Power IN (μW), Pₙ = Power normalized to 22nm scaling in (μW), A = Area in (μM²), Aₙ = Area normalized to 22nm scaling in (μM²), Te = CMOS technology node in nanometer, N/A=Not available, TW=This work

⁰Reliability conditions for temperature and voltage variations are different for each case. Worst case values reported unless otherwise noted.

¹ Average reliability value over 128 instances under temperature range of -20⁰C-120⁰C and supply voltage range of 1.2V-1.08V.

² Estimated from data plot provided in the corresponding work.

³ Power results for TW under nominal operating conditions at 27⁰C, 0.95V, and FF process corner at 32MHz.

⁴ Estimated area based on the circuit shown in Figure 3.9 with an added overhead of 3X allocated for interconnects and placement [174].

3.9 Derivation of Equations

The following subsections describe the details of derivations of equations used in Sections 3.3.1, 3.4.1 and 3.4.2.

3.9.1 Duty Cycle Sensitivity with Respect to Header Currents

The details of the sensitivity of duty cycle variation with respect to header source currents iₓ and iᵧ defined in Section 3.3.1 with equations (3.10) and (3.11) are derived here. Referring to (3.9)

\[ D = \frac{1}{(1 + \frac{i_x}{i_y})} = \frac{i_y}{(i_x+i_y)} \]  

(3.27)

Taking partial derivative of (3.27) with respect to iᵧ gives
\[
\frac{\partial D}{\partial i_y} = \frac{i_x}{(i_x+i_y)^2} \tag{3.28}
\]

Rearranging terms and substituting, \(\Delta D=\partial D\), and \(\Delta i_y=\partial i_y\) gives

\[
\Delta D_y = \frac{i_x}{(i_x+i_y)^2} \Delta i_y \tag{3.29}
\]

Taking partial derivative of (3.27) with respect to \(i_x\) gives,

\[
\Delta D_x = \frac{-i_y}{(i_x+i_y)^2} \Delta i_x \tag{3.30}
\]

Combining (3.29) and (3.30) to determine the total variation in \(\Delta D\)

\[
\Delta D = \frac{i_x}{(i_x+i_y)^2} \Delta i_y - \frac{i_y}{(i_x+i_y)^2} \Delta i_x \tag{3.31}
\]

Factoring \(i_x\) in (3.31) gives

\[
\Delta D = \frac{1}{i_x(1+i_y/i_x)} \left\{ \Delta i_y - \left( \frac{i_y}{i_x} \right) \Delta i_x \right\} \tag{3.32}
\]

Factoring \(i_y\) in (3.31) \(\Delta D\) can be written as

\[
\Delta D = \frac{1}{i_y(1+i_x/i_y)} \left\{ \left( \frac{i_x}{i_y} \right) \Delta i_y - \Delta i_x \right\} \tag{3.33}
\]

### 3.9.2 Source to Gate Voltage Impact on Current Variability

The equation (3.14) describing the impact of source to gate voltage to amplify the variation of the header source currents due to process parameter variations, used in Section 3.4.1 is derived in this section. The transistor \(P_5\) shown in Figure 3.10 is biased in saturation region. The current \(I_{p5}\) through \(P_5\) is approximated using the MOS square law as

\[
I_{p5} = \beta_0 (v_{sg0} - v_{th0})^2 \tag{3.34}
\]

where, \(\beta_0\) is the nominal mobility transconductance factor for MOS transistors \(P_5\) and \(v_{sg0}\) is the source to gate voltage. Taking partial derivatives of (3.34) with respect to transconductance factors \(\beta_0\), threshold voltage \(v_{th0}\), and gate to source voltage \(v_{sg0}\),
\[ \Delta I_{p5} = -2 \beta_0 (vsg_0 - vth_0) \Delta vth_0 + \Delta \beta_0 (vsg_0 - vth_0)^2 + 2 \beta_0 (vsg_0 - vth_0) \Delta vsg_0 \] (3.35)

where, \( P_2 \) is operating in linear region, ignoring the square term for small value of source to drain voltage, the current \( I_{p2} \) through \( P_2 \) can be approximated as

\[ I_{p2} = \beta_3 (vsg_3 - vth_3) vsd \] (3.36)

where \( vsg_3 \) is the source to gate voltage, \( vth_3 \) is threshold voltage \( vsd \) is the source to drain voltage. Ignoring small changes in \( vsd \) and taking the partial differentials of \( I_{p2} \) with respect to \( \beta_3 \), and \( vth_3 \), \( \Delta I_{p2} \) can be written as

\[ \Delta I_{p2} = -\beta_3 (vsg_3 - vth_3) \Delta vth_3 + \Delta \beta_3 (vsg_3 - vth_3) + \beta_3 (vsg_3 - vth_3) \Delta vsg_3 \] (3.37)

Assuming that \( \beta_0 \) that and \( \beta_3 \) are equal to \( \beta \) and threshold voltages \( vth_0, vth_2, vth_3 \) are equal to \( vth \), and by substituting \( \beta \) and \( vth \) in (3.37), and (3.34) in (3.35) and (3.36) respectively results in

\[ \Delta I_{p5} = -2 \sqrt{I_{p5}} \Delta vth + \frac{\Delta \beta}{\beta} I_{p5} + 2 \sqrt{I_{p5}} \Delta vsg_1 \] (3.38)

\[ \Delta I_{p2} = I_{p2} \left( \frac{\Delta \beta}{\beta} - \Delta vth + \Delta vsg_3 \right) \] (3.39)

Since \( I_{p2} \) is same as \( I_{p5} \) and the total variation in \( I_0 \) will be combined net effect of variations through series connected \( P_2 \) and \( P_5 \), replacing \( I_{p2} \) with \( I_{p5} \) on the right hand side of (A14) with \( I_0 \), adding (3.38), (3.39) and designating the total variation \( \Delta I_0 \) the total variation in \( I_0 \) is given by

\[ \Delta I_0 = \left( [ -2 \sqrt{I_0} \Delta vth + 2 \frac{\Delta \beta}{\beta} I_0 ] + [ 2 \sqrt{I_0} \Delta vsg_1 + I_0 \Delta vsg_2 ] \right) \] (3.40)

where \( \Delta vsg_3 \) and \( \Delta vsg_1 \) are replaced with \( \Delta vsg_{p2}, \Delta vsg_{p5} \) respectively.

3.9.3 Source to Drain Voltage Mismatch

Mathematical analysis of the ratio of the header currents over SS and FF process corners by using skewed width-to-length ratio for the header sources, shown in equation (3.18) is presented in this section. The source to drain voltage mismatch is obtained by using skewed transistors with digital control inputs in matched and mismatched current source branches.
Referring to transistor $P_2$ in Figure 3.10, and analyzing the current changes in transistor $P_2$ and $P_5$ due to source gate voltage of transistor $P_2$, the current through transistor $P_2$ can be expressed in linear region as follows

$$I_{P_2} = \beta_2 (v_{sg2} - v_{th2}) v_{sd2} - \beta_2 \frac{v_{sd2}^2}{2}$$ \hspace{1cm} (3.41)

where $I_{P_2}$ is the current through $P_2$, $\beta_2$ is the transconductance mobility parameter of $P_2$, $v_{th2}$ is the threshold voltage of $P_2$, $v_{sg2}$ is the source to gate voltage of $P_2$, and $v_{sd2}$ is the source to drain voltage of $P_2$.

Assuming that the transistors used in both the header $X$ and $Y$ have same threshold voltage and mobility and the transistors have same widths and lengths, the current through transistor $P_2$ in Figure 3.10 operating in linear region for header $X$ and $Y$ respectively is

$$I_{P_2x} = \beta (v_{sgx} - v_{th}) v_{sdx} - \beta \frac{v_{sdx}^2}{2}$$ \hspace{1cm} (3.42)

$$I_{P_2y} = \beta (v_{sgy} - v_{th}) v_{sdy} - \beta \frac{v_{sdy}^2}{2}$$ \hspace{1cm} (3.43)

where, $I_{P_2x}$ and $I_{P_2y}$ refer to current through header current sources $X$ and $Y$ respectively. For the same source gate voltage is applied to both current sources $X$ and $Y$ from the duty cycle to analog converter, then $v_{sgx} = v_{sgy}$, can be substituted with $v_{sg}$.

If the transistor $P_2$ in Figure 3.10, designated as $P_{2x}$ and $P_{2y}$ for headers $X$ and $Y$, respectively, have a mismatched width-to-length ratio, the corresponding source to drain voltages $v_{sdx}$ and $v_{sdy}$ will be mismatched. The relationship between voltages $v_{sdx}$ and $v_{sdy}$ can be expressed as $v_{sdx} = (1/K)v_{sdy}$, where $K$ depends on the width-to-length mismatch ratio of the transistors $P_{2x}$ and $P_{2y}$. The ratio of (3.42) and (3.43) can be expressed as

$$\frac{I_{P_{2x}}}{I_{P_{2y}}} = \frac{[(v_{sg} - v_{th})(1/K)v_{sdy} - \left(\frac{1}{K^2}\right)v_{sdy}^2/2]}{[(v_{sg} - v_{th})v_{sdy} - v_{sdy}^2/2]}$$ \hspace{1cm} (3.43)
After rearranging terms in (3.44) the ratio becomes
\[
\frac{IP_{2x}}{IP_{2y}} = \frac{[(v_{sg} - v_{th})\left(\frac{1}{R}\right) - \left(\frac{1}{R^2}\right)v_{sd,y}/2]}{[(v_{sg} - v_{th}) - v_{sd,y}/2]}
\] (3.44)

3.10 Duty Cycle Based PUF Conclusions

A duty cycle-based controlled and reconfigurable PUF primitive is proposed and validated. The proposed PUF provides a stable and reliable operation with a high entropy over a wide range of duty cycles under supply voltage and temperature variations. The proposed feedback control provides a capability to enhance the duty cycle entropy over process parameter variations. The feedback loop incorporates a small number of logic blocks, a duty cycle to voltage converter, and a self-bias generation circuit, enabling fast response and stable operation. The current starved inverter scheme provides a precise control of the circuit duty cycle by utilizing the digital inputs, enabling controllability and reconfigurability features. The PUF can also be adapted to operate at different frequencies and duty cycle values. Additionally, the digital inputs potentially provide the capability to calibrate and tune the PUF primitive post implementation and during testing.

The proposed circuit operates at a low frequency with a maximum frequency of 32 MHz with a power consumption of 3.75\(\mu\)W. The layout footprint is estimated to be in the order of 15\(\mu\)M\(^2\) which can be uniformly placed as a macro cell on a die for cryptography and security applications. The output has a low frequency of less than 32 MHz and therefore is measurable with low frequency, low cost, and low resolution instrumentation.

The proposed PUF can be enhanced to provide additional duty cycle values at the intermediate nodes of the ring oscillator that can increase the entropy further and enable the PUF to be considered as a strong PUF. Section 3.11 describes the details of an adaptable duty-cycle PUF based a redesigned version of the PWM circuit architecture.
3.11 PVT-Stable Adaptable Duty Cycle Based PUF

Controlled PUF primitives are versatile components of programmable security applications as discussed in [160, 161]. A process temperature and supply voltage stable PUF primitive that is adapted to use the duty cycle at each node of a of the seven-stage of a duty cycle controlled ring oscillator is proposed in this section. The proposed PUF is based on the principles of the duty cycle controlled PWM described in detail in Chapter 2. A temperature stable PUF primitive based on ring oscillator duty cycle comparisons has also been proposed [162]. The proposed PUF uses delay-mismatched inverter stages exploiting width-to-length mismatch among ring oscillator stages. This mismatch produces a different duty cycle at each inverter stage. This PUF therefore consists of a fifteen-stage ring oscillator to produce distinct duty cycles. The PUF proposed in [162] also lacks the capability of a controlled PUF.

Alternatively, the PUF primitive proposed in this section uses a current starved ring oscillator with seven stages to introduce delay-mismatched inverters that produce distinct duty cycles at the output of each stage [97]. A PVT stable, low power operation and reliable PUF primitive is realized using feedback techniques. Stable threshold values can be used to distinguish between duty cycles to differentiate between wrong and valid comparison conditions. In addition to the manufacturing process variations to provide random values that conventional PUFs rely on, the proposed PUF also houses digitally controlled current sources that can be configured to provide a random challenge to produce a random set of duty cycles over a wide range for response bit generation.

\[1\] Parts of this section and sub-sections is published in IEEE Proceedings of ISCAS 2018 [176]. Permission is included in Appendix A Section A5
3.11.1 PWM Preliminaries Recapped

A typical ring oscillator circuit with \((2m+1)\) stages, where \(m\) is a positive integer, is shown in Figure 3.2 and is reproduced here as Figure 3.19.

Figure 3.19 Ring oscillator circuit with \(2m+1\) inverter stages

The corresponding high and low time at the output of each node \(N1, N2, \ldots N(2m+1)\) can be expressed as described in Section 3.2 with (3.1 and 3.2) and reproduced here:

\[
\begin{align*}
    tph &= \sum_{i=1}^{(m+1)} tdf(i) + \sum_{i=1}^{m} tdr(i) \\
    tpl &= \sum_{i=1}^{(m+1)} tdr(i) + \sum_{i=1}^{m} tdf(i)
\end{align*}
\]

(3.46) (3.47)

where \(tdf(i)\) and \(tdr(i)\) are, respectively, the fall and rise propagation delay of each inverter stage.

As a case study for a seven stage ring oscillator \(i.e., m=3\), where the rise time between odd and even stages is mismatched by a factor \(K\)-factor = \((tdr(i)/tdr(i+1))\), the low and high time at the output and corresponding duty cycle have different values. Theoretical analysis of the duty cycle value using (3.46) and (3.47) and a value of \(K\)-factor ranging from 0.3 to 1, the corresponding duty cycle at each node, \(N1\) to \(N7\), has a different value and changes uniformly with the \(K\)-factor, as shown in Figure 3.20.
The separation between the duty cycles at each node $N1$ to $N7$ in Figure 3.20 can be increased by using added offset values to fall delay between alternate stages.

![Graph showing duty cycle vs. K-factor](image)

Figure 3.20 Duty cycle at the nodes $N1$-$N7$ under different delay ratio $K$-factor.

A digitally controlled pulse width modulator to control the ring oscillator rise and fall time at each stage and correspondingly the duty cycle at each stage output is described in detail in Chapter 2. An architectural block diagram and circuit schematic of the PWM using header and footer current sources is introduced in Chapter 2 and is shown in Figure 2.2 and 2.3 respectively is reproduced here in Figures 3.21 and 3.22 respectively.

![Block Diagram of Header and Footer Based PWM](image)

Figure 3.21 Block diagram of the header and footer based pulse width modulator

![Ring Oscillator Circuit](image)

Figure 3.22 Seven-stage current controlled ring oscillator circuit
A digital current source control feature for the PWM is utilized to demonstrate the proposed adaptable, controlled, and re-configurable PUF circuit primitive in this section. The duty cycle $D$ and the frequency $F_{\text{new}}$ of the PWM expressed in (2.30) and (2.22)

$$D = 1/(1+(\alpha/\beta)\gamma/\delta))$$

$$F_{\text{new}} = 2 \times (1 - D) \times F_0$$

where, referring to Figure 3.22, parameters $\alpha = I_A/I_A5$, $\beta = I_B/I_B5$, $\gamma = I_C/I_C5$, and $\delta = I_D/I_D5$. $I_A$, $I_B$, $I_C$, and $I_D$ are the currents passing through, respectively, $I_a$, $I_b$, $I_c$, and $I_d$. $I_A5$, $I_B5$, $I_C5$, and $I_D5$ are the currents passing, respectively, through $I_a$, $I_b$, $I_c$, and $I_d$ to provide a 50% duty cycle. $F_0$ is the frequency of PWM when $D$ is equal to 0.5, and $F_{\text{new}}$ is the new frequency of the PWM.

### 3.11.2 PWM Based Adaptable Duty Cycle PUF Primitive

The proposed PWM circuit for PUF application is shown in Figure 3.23. The footer circuits $Ic1$, $Id1$, $Ic2$, $Id2$, $Ic3$, $Id3$ and $Ic4$ are a set of NMOS transistors connected to each inverter stage to control the sink current of each stage. The footers are controlled with digital inputs to provide the correct current to produce the fall delay offset and accordingly to produce a unique duty cycle at each of the output nodes $N1$-$N7$. The header circuit provides duty cycle control with digital inputs and PVT compensation capability.

![Figure 3.23 Redesigned seven-stage current controlled ring oscillator](image-url)
The current controlled variable duty cycle PWM described analytically in (3.49) is exploited to develop a PUF primitive. Evaluation of the duty cycle at each node \( N1 \) to \( N7 \) of the current controlled PWM is performed using a range of current ratio values for currents \( I_A \) and \( I_B \) from the current sources \( I_a \) and \( I_b \). The corresponding current distribution at odd and even stages is determined for each node \( N1 \) to \( N7 \), to determine the ratio \( \alpha/\beta \) used in (3.49). The corresponding footer current and ratio \( \gamma/\delta \) for each node \( N1 \) to \( N7 \) is evaluated and applied in (3.49). The duty cycle for each node \( N1 \) to \( N7 \) versus header current ratio, \( K\)-factor = \( \alpha/\beta \) is shown in Figure 3.24. The current mismatch produces a wide duty cycle distribution for each node over a higher mismatch range of \( K\)-factor.

![Figure 3.24 Duty cycle at nodes N1-N7 under different current ratio K-factor.](image)

3.12 Adaptable Duty Cycle Based PUF Details

Each PWM based PUF primitive on a chip can be independently configured to produce seven different and independent groups of duty cycle values that can be adaptively changed through digital control inputs. An important requirement of a PUF primitive is to provide distinct values at the output for comparison that are above the error threshold. Additionally, the values should be reliable under environmental changes such as temperature and supply voltage variations. The manufacturing process stable PUF can be randomized with random digital control inputs. The PUF can be adapted to re-configure the PUF duty cycle outputs with digital control. The proposed
PUF is evaluated with transistor-level simulations and satisfies the requirements of a feasible PUF primitive.

3.12.1 Adaptable PUF Unique Outputs

A statistical analysis of the duty cycle is performed with Monte Carlo simulations using 32nm PTM [138] CMOS models. A duty cycle histogram chart of the Monte Carlo simulation of 200 samples of the two different configurations of the header current source ratio for the PUF circuit is shown in Figure 3.25. The duty cycle values are distinctly separated with a very low statistical spread which is indicated with low standard deviation value. The proposed PUF circuit provides a wide range of 20%-90% duty cycle outputs based on digital challenge inputs. Accordingly, the proposed PUF can generate a large set of challenge-response pairs for security applications.

![Duty cycle histogram](image)

Figure 3.25 Duty cycle histogram for \((\alpha/\beta) > 1\) (top) \((\alpha/\beta) < 1\) (bottom)

3.12.2 Adaptable PUF PVT Stability Simulation Results

The duty cycle comparison based proposed PUF primitive is stable over temperature, voltage, and process variations. The DC2V feedback circuit used in the PWM compensates the header currents over the IC manufacturing process conditions, temperature changes, and supply voltage variations to keep the duty cycle constant to within 1%-2% over the operating ranges. Circuit simulations performed with CMOS 32nm PTM models over SS and FF corners, temperature range of 0°C-100°C, and supply voltage of 1 V are shown in Figure 3.26. The duty
cycle differences over SS and FF process corners deviate within 1% value for the output nodes $N1$ to $N7$ and between 1%-2% over temperature range of 0°C-100°C. Simulation results of duty cycle over the supply voltage range of 0.9V-1.05V, 27°C, for SS and FF process corners, are shown in Figure 3.27. The duty cycle at each output node is stable to within 1% between the voltage range of 0.9V to 1.05V over SS and FF process corners. A typical value of 2% threshold difference for error limits over PVT conditions ensures the validity of unique values for duty cycle comparisons to generate distinct output response bits.

![Figure 3.26 Temperature versus duty cycle for output nodes $N1$-$N7$](image1)

![Figure 3.27 Supply voltage versus duty cycle for output nodes $N1$-$N7$](image2)

3.13 Adaptable Duty Cycle PUF Reliability Simulation Results

Monte Carlo circuit simulation of 100 instances of the proposed PUF primitive using 32nm PTM models is performed over the temperature range of 0°C-100°C at 1V to evaluate the temperature reliability. The variation of standard deviation of the duty cycle (left) and the mean value of the duty cycle (right) over the temperature range of simulation for output nodes $N1$-$N7$ are shown in Figure 3.28. The fractional value of the standard deviation and stable duty cycle mean
value demonstrates a stable and reliable PUF primitive over temperature. Monte Carlo circuit simulation of 100 instances of the proposed PUF primitive using 32nm PTM models is performed over the supply voltage range of 0.95V-1.05V at 27°C to evaluate the supply voltage reliability. The standard deviation and mean value of the duty cycle is shown in Figure 3.29 over the operating voltage range. The standard deviation of the duty cycle is a fractional value for output nodes N1-N7 with a stable mean value over the supply voltage range.

![Figure 3.28 Standard deviation (left) and mean (right) values of the duty cycle under temperature variations](image)

![Figure 3.29 Standard deviation (left) and mean (right) values of the duty cycle under supply voltage variations](image)

3.14 Adaptable Duty Cycle Based PUF Conclusions

A variable duty cycle PUF primitive is proposed for security applications. The proposed PUF primitive is demonstrated to be stable over the worst case and best case manufacturing process, supply voltage, and temperate variations. The proposed PUF primitive uses current starved inverters, thus reducing the power requirements. The feedback utilized to maintain a robust duty cycle under PVT variations uses a simple, stable circuit that provides a fast response with an
effective compensation over the operating ranges. The proposed PUF primitive is configured and controlled with digital inputs for security adaptation and therefore well suited for programmable applications, portable applications requiring low power and small area.
CHAPTER 4:

FINAL CONCLUSIONS

A novel implementation and application of pulse width modulator has been studied and demonstrated with analysis and simulations at system and circuit level. A novel duty-cycle based PUF and variations of the architecture has been studied and demonstrated with system analysis, circuit implementations and a wide range of simulation results.

The proposed designs have been qualitatively and quantitatively compared with state-of-the-art work and has been demonstrated to be well defined, superior and, comparable in attributes and merits. The work has been accepted for publications in leading technical journals and conferences for a successful scholarly demonstration.
CHAPTER 5: FUTURE WORK

The PWM circuit described in Chapter 2 can be used with a variety of circuits that require variable duty cycle and or fixed / variable frequency. Two of the applications of the circuit, the voltage regulator, converter and a stable physical unclonable function are described and demonstrated in this work through analysis and simulation. In addition other applications such as Class D power amplifier control can be explored and demonstrated with the use of the PWM.

One of the major weakness of the ring oscillator PUF (ROPUF) is the limited number of challenge response pairs (CRP) compared to an arbiter PUF. The controlled and adaptable PUF proposed in Chapter 3, Section 3.11 can be further enhanced to provide a wide distribution of duty cycle at each node of the ring oscillator PUF. This will ensure a high entropy of duty cycle distribution and potentially increase the number and quality of randomness of the challenge response pair, thus making the PUF a strong PUF. A complete study of this feature is recommended as a future plan of work. This will require support for an appropriate parallel circuit simulation environment.

The PUF control circuit can be configured to produce a non-linear output duty cycle behavior. This can help in developing a PUF that is resistant to machine learning attacks. Recent attempts to combine security and voltage regulation methods on IC have been described in Introduction Chapter 1, Section 1.3. The present duty cycle controlled PWM based PUF can be used in phases of duty cycle shuffle during its operation with a voltage regulator converter circuit to potentially provide security against power profile, side channel and leakage attacks on the
integrated circuit through the power network. A future fabrication of the circuit and measurement data from the fabricated circuits will confirm the full functionality in a real application. This will help to further confirm and demonstrate the novel ideas proposed in this work.
REFERENCES


82


APPENDIX A: COPYRIGHT PERMISSIONS

A.1 Copyright Permission Page

The permission below is for the use of material in Chapter 1, Section 1.2.

Title: An area efficient fully monolithic hybrid voltage regulator Conference Proceedings of 2010 IEEE
Proceedings: International Symposium on Circuits and Systems
Author: Selcuk Köse
Publisher: IEEE
Date: May 2010
Copyright © 2010, IEEE

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author’s approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/publishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.
A.2 Copyright Permission Page

The permission below is for the use of material in Chapter 1, Section 1.5 and Chapter 2.

Title: An enhanced pulse width modulator with adaptive duty cycle and frequency control
Author: Mahmood J. Azhar
Publisher: IEEE
Date: June 2014
Copyright © 2014, IEEE

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.
A.3 Copyright Permission Page

The permission below is for the use of material in Chapter 2.

Title: Digitally Controlled Pulse Width Modulator for On-Chip Power Management
Author: Inna Vaisband
Publication: Very Large Scale Integration Systems, IEEE Transactions on
Publisher: IEEE
Date: Dec. 2014
Copyright © 2014, IEEE

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis online.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.
A.4 Copyright Permission Page

The permission below is for the use of material in Chapter 3.

10/26/2018

Title: Duty-Cycle-Based Controlled Physical Unclonable Function
Author: Mahmood J. Azhar
Publication: Very Large Scale Integration Systems, IEEE Transactions on
Publisher: IEEE
Date: Sept. 2018
Copyright © 2018, IEEE

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication].
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.

Copyright © 2018 Copyright Clearance Center, Inc. All Rights Reserved. Privacy statement. Terms and Conditions. Comments? We would like to hear from you. E-mail us at customercare@copyright.com
https://s100.copyright.com/AppDispatchServlet#formTop

87
A.5 Copyright Permission Page

The permission below is for the use of material in Chapter 3, Section 3.10.

Title: Process, Voltage, and Temperature-stable Adaptive Duty Cycle based PUF
Conference 2018 IEEE International
Proceedings: Symposium on Circuits and Systems (ISCAS)

Author: Mahmood J. Azhar
Publisher: IEEE
Date: May 2018
Copyright © 2018, IEEE

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © [Year of original publication] IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.
ABOUT THE AUTHOR

Mahmood Javed Azhar (M’84) received the M.S.E.E degree in electrical engineering from University of Wisconsin Madison, WI, USA, in 1984. He was a Component Engineer with Intel Corporation, Custom Products Group, Chandler, AZ, USA from 1984 to 1986. From 1986 to 1987 he was a Member Technical Staff with CMOS Gate Array Design Automation Group, GTE (now Verizon Inc.) Microcircuits, Tempe, AZ, USA. From 1987 to 1994, he was a Senior Engineer with Motorola Inc., Semiconductors Group (now Freescale Semiconductors), custom products and analog mix-signal design division in Chandler and Tempe, AZ, USA. From 1994 to 2001 he was a Staff Engineer with Motorola Inc., Communications Group, Paging products Group, Boynton Beach, FL, USA. From 2001 to 2007 he was a Principal Staff Engineer with Motorola Inc. (now Motorola Solutions Inc.), Research Labs, RFIC Labs Division, Plantation, FL, USA. In 2008 and 2009 he was a Lead Engineer with Cadence Design Systems, Melbourne, FL, USA. During 2015 he worked as a consultant with Qualcomm, as CPU custom circuit design methodology engineer, in Raleigh, NC, USA. He has completed his Ph.D. degree work in Electrical Engineering at University of South Florida, Tampa, Florida, USA in the Fall semester of 2018. His research interests include the design of high performance integrated circuits. He is been active research and teaching assistant with the Department of Electrical Engineering, University of South Florida, Tampa, USA since 2013. He defended his Ph.D. dissertation on October 26, 2018.