Spintronic Circuits: The Building Blocks of Spin-Based Computation

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Abstract

In the most general situation, binary computation is implemented by means of microscopic logical gates known as transistors. According to Moore's Law, the size of transistors will half every two years, and as these transistors reach their fundamental size limit, the quantum effects of the electrons passing through the transistors will be observed. Due to the inherent randomness of these quantum fluctuations, the basic binary logic will become uncontrollable. This project describes the basic principle governing quantum spin-based computing devices, which may provide an alternative to the conventional solid-state computing devices and circumvent the technological limitations of the current implementation of binary logic.

PROBLEM STATEMENT & MOTIVATION

The problem under investigation in this project is: how can the limitations proposed by Moore's law be circumvented using a method that uses pure quantum states and is free from conventional limitations

MATHEMATICAL DESCRIPTION AND SOLUTION APPROACH

I. BINARY LOGIC, BOOLEAN ALGEBRA, AND CLASSICAL COMPUTING DEVICES.

Let A be a set algebra $A = \{\emptyset, A, B, \ldots, X\}$. Here, any set A is a subset of X, and if $A \in A$, then so is its complement, $A^c = X \setminus A \in A$. Similarly, if $A, B \in A$, then their union and intersections are also in A. In mathematics, this kind of set is known as *set algebra*. The elements of this set (of sets) can be identified by the rule

$$\emptyset \rightarrow 0, A \rightarrow a, B \rightarrow b, \ldots, X \rightarrow 1,$$

and to every element "*a*" a dual is associated *a'*, so that $a \rightarrow A$, $a' \rightarrow A^c$. The set operations with the (logical) "addition" and "multiplication"

$$a + b \rightarrow A \cup B, a \cdot b \rightarrow A \cap B.$$

In this way, the elements of A, together with the "operations" described above, form indeed an algebra, although it is quite different from the usual algebra of real numbers, with the usual addition and multiplication.

Equivalently, if *a, b* are understood as logical statements, then the addition corresponds to

logical disjunction (*OR*), and the multiplication corresponds to logical conjunction (*AND*), while the dual corresponds to logical negation (*NOT*):

$$a + b \rightarrow a \lor b, \, a \cdot b \rightarrow a \land b, \, a' \rightarrow \neg a.$$

With this identification, the set algebra is a Boolean algebra (or binary logic algebra), in which 0 = *FALSE* and 1 = *TRUE*.

As an example, consider the Boolean algebra B4, which consists of all the numbers written in base 2, from 0000_2 which is identified with the element 0, up to 1111_2, which is identified with the element 1. Then the dual of *a* is the number *a'* such as $a + a' = 1111_2$ in the usual sense, such as:

$$a = 1100_2 \Rightarrow a' = 0011_2.$$

However, it should be noted that the addition and multiplication operations on $\mathbb{B}_4$ are not the usual addition and multiplication of numbers (whether in base 2 or not), but instead it is given by the rules of union and intersection of sets. For example, since any number $a \in \mathbb{B}_4$ corresponds to a subset of 1111_2, then for the Boolean addition:

$$a + 1111_2 = 1111_2, \, \forall a \in \mathbb{B}_4.$$

II. TRANSISTOR-BASED LOGICAL GATES

It can be easily seen that any logical "statement" based on binary logic, as described in the previous section, can be understood as a succession of simple logical statements, whose "values" can be only 0 = *FALSE* or 1 = *TRUE*. This is just another way of saying that any Boolean algebra, such as $\mathbb{B}_4$, is made up of many copies of the simplest one, $\mathbb{B} = \{0,1\}$.

This mathematical structure is implemented using electronic *logical gates*, which are

based on the type of circuit element known as the transistor.

The purpose of these small devices is to act like a switch: *T RUE/FALSE*. Transistors consist of two adjoining *diodes*, or P-N junctions, which have two states much like a commercial switch: an "on" state, and an "off" state. However, these states are commonly known as a 1 = *T RUE* state when the electron or current flow is allowed through the junctions and a   0 = *FALSE* state, when the junction is closed and the current cannot flow through. The two parts of a junction consist of P-type and N-type semiconductors, where P and N stand for positive and negative doping, or doping with electron vacancies (holes) and electrons, respectively.
The purpose of having two adjoining junctions (either P-N-P, or N-P-N), is to allow for control of the states (on/off) of the junctions, since the junction will allow current to flow through only when the two semiconductors it is made of are set at a given electrostatic potential difference (for example, 0.3 Volts or 0.7 Volts, for certain types of semiconductor materials, like Ge or Si). The three semiconductors in a transistor (either P-N-P or N-P-N) are kept at different values of electrostatic potential, which makes it possible at once to provide the current which can flow through the device and the control to turn it on and off.

There are millions and billions of transistors in every electronic device. By combining such extremely large numbers of logical gates, it was possible to create very large logical memories, for example, such as to represent numbers like $2^{15} - 1$ in a computer hardware. To a large extent, the extraordinary progress made by the computer science and engineering in the second half of the last century was based on putting together more and more transistors on a smaller and smaller circuit board. However, this kind of progress has an ultimate fundamental limitation, commonly known as Moore's law, see Figure 1. While the law itself does not speak of any limitation (it is an empirical observation that the number of transistors per given area of

circuit board increases exponentially in time), one consequence of its extrapolation does: it is certain that the current technology will reach a point where the junction thickness (and inter-junction distances) will become so infinitesimally small that quantum tunneling effects will become observable, and so the state of a junction (on/off) will stop being controllable, due to the inherent randomness of quantum fluctuations.

To explain this fundamental quantum limitation, it is necessary to distinguish between the classical and quantum behavior of a "particle" traveling towards a potential (energy) barrier, see Figure 2. In classical mechanics (an approximation which is also appropriate for a PN junction, when its size is sufficiently large), creating a potential barrier (for example, by setting the electrostatic potential of one of the semiconductors to a certain, higher, value) will not allow the electrons from the other side of the junction to travel through - so indeed the junction may be considered "closed" or "off" (as shown in the top diagram of Figure 2).

However, upon decreasing the size (or "thickness") of PN junctions below a certain threshold value, the approximation given by classical mechanics breaks down, and quantum phenomena become observable. In particular, quantum tunneling through potential barriers stops being negligible, and electrons from one side of the junction will tunnel with a certain (non-zero) probability through the potential barrier meant to keep the junction in the "off" state, and so current will flow through a "closed" gate, subject to quantum randomness.

Therefore, the transistor-based implementation of binary logic might eventually reach this fundamental limitation, when it will not be possible to accurately control the state of logical circuits (they would fluctuate at random between *TRUE* and *FALSE*), making computation impossible. In the next subsection, a numerical estimate for the critical linear density of junctions beyond which this technology will stop being applicable is presented.

III. SIZE ESTIMATION FOR LINEAR ENSEMBLE OF SEMICONDUCTOR JUNCTIONS AT THE

CLASSICAL-QUANTUM TRANSITION POINT.

Assume there are N identical junctions, each kept at potential difference V (typical values

are around 0.5 Volts), approximated as rectangular potential barriers of linear size "d", and

aligned along a "linear" computer chip of length L. To estimate the critical value of d, denoted

d_0, at which the ensemble of junctions will fail to behave classically, in the sense that the

probability for transmission of electrons through the chip, when all junctions are "closed" (and

when, classically, no current should flow through), exceeds a certain threshold value, P_0 (for

example, we could take $P_0 = 10^{-6}$ as a significant failure of the chip to be "closed" when all the

junctions are in the "closed" state). The probability of quantum tunneling through a rectangular

barrier as described above can be approximated (by using the method known in physics as

Wentzell-Kramers-Brillouin, or WKB [5], a formula used for solving linear differential

equations with changing coefficients, which in this case is the amplitude) by the formula:

$$P(d) \cong \beta^d, \quad \beta = e^{\frac{-\sqrt{8em(V-E)}}{\hbar}},$$

where E, e, m represents the incident electron energy, charge, and mass, respectively, and V is

the electrostatic potential difference across the junction (or barrier "height"), and $\hbar$ is the reduced

Planck's constant. Therefore, the probability that the junction does not "transmit" is $1 - P(d)$.

Now, for identical junctions distributed uniformly over the total length L, the simple relation (2)

is obtained.

$$Nd = L \Longrightarrow N = \frac{L}{d} \tag{2}$$

Therefore, the probability that the chip "transmits" with all junctions "closed" is given by

$$P_T = 1 - [1 - P(d)]^N = 1 - [1 - P(d)]^{L/d}$$

this is to say it equals 1 minus the probability that all the junctions (which are independent) stay

closed at the same time. Imposing the "failure" condition:

$$P_T \geq P_0$$

leads to the inequality

$$1 - [1 - P(d)]^{\frac{L}{d}} \geq P_0 \implies 1 - P_0 \geq [1 - P(d)]^{\frac{L}{d}} \implies (1 - P_0)^{\frac{d}{L}} \geq 1 - P(d),$$

and finally to

$$P(d) + r^d \geq 1, \quad r = (1 - P_0)^{\frac{1}{L}}.$$

Therefore, the critical value d_o is the solution to the equation

$$\beta^{d_o} + r^{d_o} = 1 \tag{1}$$

which can be solved approximately (that is, find numerical values for β, r, plot the function on

the LHS of the equation, and then calculate the value of d at which the function reaches the value

1 (the minimum value of $P(d) + r^d \geq 1$), after plugging in the numerical values for all the

relevant parameters of the problem (e, m, $\hbar$, V, L, P_0). Finally, it is possible to obtain the critical

value $N_0 = \frac{L}{d_0}$ of junctions per unit length, at which the device stops behaving classically

(compared to Moore's law to estimate how soon the computer engineering industry will reach

that threshold). Being a transcendental equation, (1) cannot be solved exactly. However, since

both β and r are strictly positive and less than 1, the function $f(x) = \beta^x + r^x$ is monotonically

decreasing (since $f'(x) = \beta^x \ln(\beta) + r^x \ln(r) < 0$), so it is possible to find the unique solution

to (1) by implementing Newton's method for $f(x) - 1 = 0$. For $P_0 = .36 * 10^{-6}$, and $L_0 = 10^3$ nm, at $V - E = 0.3$ eV, we evaluate d_0. Plugging in the respective values, we get:

$$\beta = .9999999611$$

And,

$$r = .697676$$

With an initial assumption value for $x \cong 50$. Therefore, the transcendental function becomes

$$.9999999611^x + .697676^x - 1 = g(x)$$

Newton's Method follows using a tangent approximation:

$$x_{n+1} = x_n - \frac{g(x_n)}{g'(x_n)}$$

Where,

$$g^n(x) = \beta^x \ln^n(x) + r^x \ln^n(x)$$

Replacing the value $x = 50$, the 1st iteration yields:

$$g(50) = -1.93 * 10^{-6}$$

$$g'(50) = -4.43 * 10^{-8}$$

This gives forth $x_1 = 6.433$. Subsequent iterations are showed below. To simplify the iterative process, the rational expression is reduced to simplest terms, specifically:

$$x_{n+1} = x_n - \frac{\beta^x + r^x}{\beta^x \ln(\beta) + r^x \ln(r)} \Longrightarrow x_n - (-2.773) \Longrightarrow x_n + 2.773, \text{ for } x_1 \leq x_n \leq x_{11}$$

Iteration number	Value of $g(x_n)$	Approximation result
2nd	$g(x_2) = .09867$	$x_2 = 9.2109$
3rd	$g(x_3) = .03630$	$x_3 = 11.9886$
4th	$g(x_4) = .01335$	$x_4 = 14.7699$
5th	$g(x_5) = .00490613$	$x_5 = 17.6580$
6th	$g(x_6) = .00173$	$x_6 = 20.431$
7th	$g(x_7) = .000638$	$x_7 = 23.205$
8th	$g(x_8) = .0002262$	$x_8 = 25.872$
9th	$g(x_9) = .00008915$	$x_9 = 28.616$
10th	$g(x_{10}) = .00003246$	$x_{10} = 31.293$
11th	$g(x_{11}) = .00001159$	$x_{11} = 33.786$
12th	$g(x_{12}) = 3.90592 * 10^{-6}$	$x_{12} = 35.822$
13th	$g(x_{13}) = 1.11475 * 10^{-6}$	$x_{13} = 37.00572$
14th	$g(x_{14}) = 1.98862 * 10^{-7}$	$x_{14} = 37.322$

The approximation converges to the critical value for $d_0 = 37.322$ nm. Testing the solution graphically yields the same result:

Root plot:
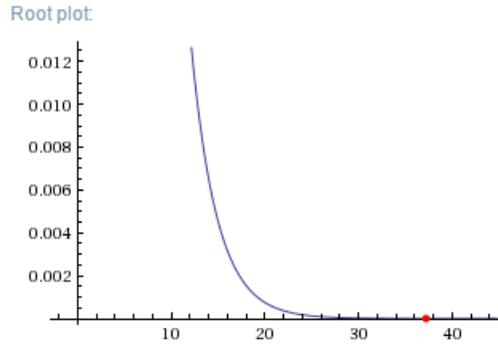
Alternate form:

$$0.697676^x + 1.^x = 1$$

Alternate form assuming x is real:

$$0.697676^x + 1.^x + (-1. + 0. i) = 0$$

Solution:

$$x = 37.3395$$

Therefore, the linear density, N_0, is 30 transistors for every 10^3 nm as calculated from (2). This linear density value is constant for any L_0, for the value of d_0 is a function of L_0. Therefore, it is concluded that the critical linear density for all electronic devices occurs at $30 \frac{transistors}{\mu m}$ (3) or any manipulation of (3).

IV SPINTRONICS-BASED COMPUTATION

To circumvent the fundamental limitation represented by quantum tunneling, it is necessary to use a different implementation of a binary logical gate, which at the same time should be using pure quantum states of the electron. This is such that the new implementation should not ever reach a break-down limit, as conventional (or charge-based) computing is currently facing. One candidate for this new type of implementation of binary logic is being referred to as spintronics, or spin-based electronics. To explain how the electron spin can be used to encode the two states of binary logic (1 = *TRUE* and 0 = *FALSE*), it is helpful to draw an analogy with optics, or rather

with the states of the particle of light, the photon (see Figure 3).

Light, in this example, is regarded as an electromagnetic wave (that is to say, one can neglect its true, quantum nature, and ignore the fact that it is really a collection of quantum particles - photons - and approximate it by a classical wave phenomenon). An electromagnetic wave consists of an electric component and a magnetic component, working together to propagate through space and time with each component feeding the other by periodic oscillations. The fact that a pair of time-varying electric and magnetic fields "feed" each other and propagate together in space and time is mathematically formulated through the equations known as Maxwell's equations.

Light is a *transversal* wave. This means that, relative to the direction of propagation, the two components (electric and magnetic) are perpendicular, and also perpendicular to each other (Figure 3).

When a transversal wave is polarized, the wave is split into two separate waves where one of them is blocked. Both waves have the same propagation direction, but the oscillation patterns are orthogonal to each other. For example, one wave could have the electric component oriented "horizontally" (see Figure 3), and the other would have it oriented "vertically". A linear polarizer will block one of these two, and let pass only the other, so the transmitted wave will now have only one direction of oscillation for the electric component, and only one (perpendicular) direction for the magnetic component. Naturally, linear polarization occurs sometimes when light reflects off smooth surfaces, for certain values of the incident angle (known as the Brewster angle [1]). The fact that the reflection is linearly polarized allows to block it off, by using polarizing glasses, which greatly dim the intensity of linearly-polarized light (also known as "anti-glare" glasses). Much like electromagnetic waves, a traveling electron

(that is to say, which is not confined or bound to an atom) also has two independent polarizations. Starting from the axioms of quantum mechanics [4], it is possible to show that a traveling electron also has two possible independent polarizations, referred to as the $K+$ and $K-$, or the Ordinary and Extraordinary waves. This is related to the fact that the total energy of the traveling electron consists of two parts, the usual kinetic energy and the energy associated with its "spin", or intrinsic angular momentum. 'Extraordinary' waves are waves (electron beams) that are distorted from general reflection laws due to spin coupling, while 'Ordinary' waves are waves that at incidence are in direction or anti-directional to the barrier axis and follow general optic laws. Due to the different properties of both reflected beams, there is a difference between the ordinary and extraordinary wave's reflection angles, known as the jump angle [4].

CONCLUSIONS AND MISCONCEPTIONS

By using this difference in the reflection angle between the two waves, it is possible to select one or the other by simply collecting the reflected wave at a specific angle (either the wave is given by Snell's law, or the wave includes the jump angle), and use them as the two logical states 0 = Extraordinary, = FALSE and 1 = Un-polarized = TRUE (or both polarizations present). Then the correct binary logic is indeed implemented by simple superposition, since obviously $0+0 =0, 0 + 1 = 1, 1 + 1 = 1$, which is the required Boolean algebra for binary logic. The obvious advantage of this approach is that it uses pure quantum states and is free from conventional limitations such as density of logical gates (Moore's law). As said before, the proposed solution no longer implements the conventional method of the transistor, but the transistor is still controllable. Because the transistor detects its state based on electron spin, does not mean one cannot control its state. If the controller wishes to put the transistor on an "*TRUE*" state, then the

controller can simply send current, intentionally. The method proposed solves the issue of the unintentional electrons passing through. In addition, the method used in page 8, could have also been solved using a Taylor polynomial by expanding out the polynomial:

$$1 + \sum_{1}^{n} \left[\frac{\beta^x ln^n(\beta) + r^x ln^n(r)}{n!} \right] x^n = f(x), \tag{4}$$

and solving for when (4) = 0.

NOMENCLATURE

SYMBOL	DEFINITION
β^x	Probability of electron tunneling
N_0	Linear density of transistors
L_0	Length of computer chip
d_0	Critical size of the transistor
x_n	Initial root of transcendental function
x_{n+1}	Subsequent root calculated by Newton's Method
$f(x)$	Transcendental equation to calculate the critical value
$g(x_n)$	$f(x) - 1$
r^x	Probability of all transistors not imposing the failure condition
$\beta^x + r^x = 1$	Minimum value of the inequality $\beta^x + r^x \geq 1$

FIGURES

Figure 1. Empirical data illustrating the growth of density of transistors on integrated circuits making up computers [2].

Figure 2. Schematic representation of classical and quantum scattering off potential barriers [4].
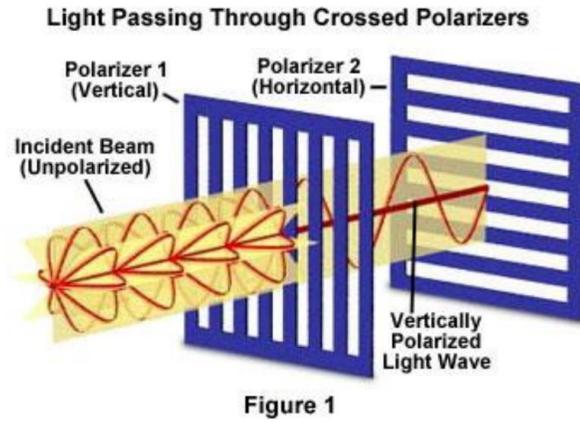
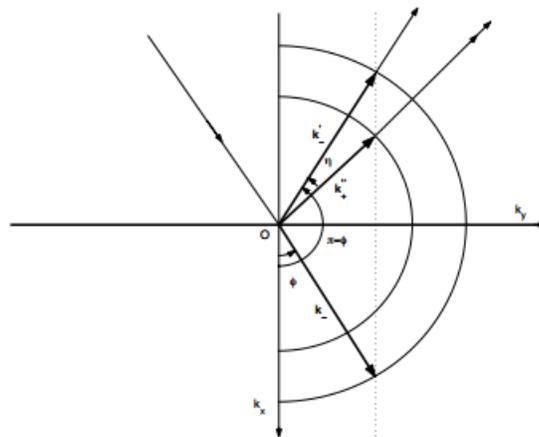Figure 3. Polarization of electromagnetic waves [3].

Figure 4. Potential barrier scattering for the ordinary component of the traveling electron wave [7].
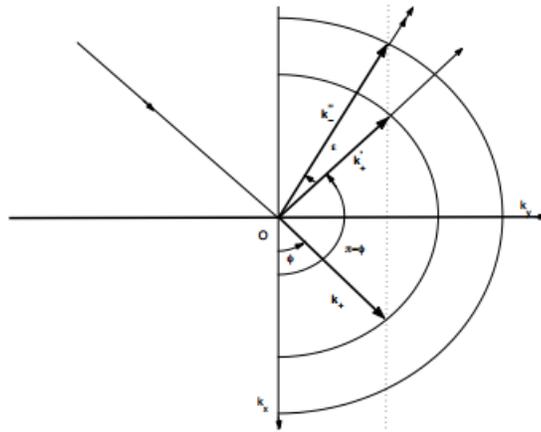
Figure 5. Potential barrier scattering for the extraordinary component of the traveling electron wave [7].

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