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# Processing and characterization of CIGS - based solar cells

Venkatesh Mohanakrishnaswamy  
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Processing And Characterization Of CIGS - Based Solar Cells

by

Venkatesh Mohanakrishnaswamy

A thesis submitted in partial fulfillment  
of the requirements for the degree of  
Master of Science in Electrical Engineering  
Department of Electrical Engineering  
College of Engineering  
University of South Florida

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## **DEDICATION**

This thesis is dedicated to my family

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# **PROCESSING AND CHARACTERIZATION OF CIGS - BASED SOLAR CELLS**

Venkatesh Mohanakrishnaswamy

## **ABSTRACT**

The goal of this research was to understand the role of the glass substrate and molybdenum (Mo) back contact on the performance of Copper Indium Gallium diselenide (CIGS) / Cadmium Sulphide (CdS) based photovoltaic devices, and to improve the performance of these devices.

The CIGS absorber layer was fabricated in a 2 stage process. In this process the metal precursors were deposited at 275°C followed by a high temperature selenization step. The advantage of the 2 stage process is that it is manufacturing friendly.

The first step in fabrication of solar cells is to clean the substrate which is necessary to obtain good device performance. A variety of environmentally friendly solvents were evaluated, to determine the optimal cleaning agent.

At elevated temperatures of processing sodium tends to diffuse out of Soda lime glass (SLG) and enter the semiconductor. The presence of this sodium during CIGS fabrication is necessary to obtain high efficiency CIGS based solar cells. A silicon nitride barrier layer was sputtered onto the SLG substrates, and this substrate was used to make complete devices. The CIGS absorber layer was deposited by the Type I recipe in two different vacuum systems. These devices were compared with standard devices the Si<sub>3</sub>N<sub>4</sub>

barrier layer, to understand the role of sodium on the devices fabricated from both of the systems.

Furthermore, the influence of molybdenum processing parameters, such as thickness and rate of sputtering, on device performance were studied.

The Voc of devices fabricated using the Type I process was limited to 460mV. In order to improve the Voc's a new absorber recipe (Type IV) was developed. Voc's of upto 490mV, Jsc's of upto  $37.4\text{mA/cm}^2$  and FF of 64%, were obtained. This improvement in performance was due to incorporation of gallium in the space charge region.

Techniques such as I-V measurements, spectral response, SEM and EDS measurements were used to characterize the devices.

## **CHAPTER 1**

### **INTRODUCTION**

The start of the Industrial revolution triggered the use of Non-Renewable sources of energy around the globe. Technological advances, like the development of the internal combustion engine and the birth of the petrochemical industry, spurred rapid growth in the demand for oil. Between 1950 and the early 1970's, world energy consumption was doubling every 15 years. As energy consumption escalated, many Industrial nations that included the United States, Japan, and countries from Europe, that had been energy self sufficient became dependent on energy imports, largely from the oil rich Middle East. The industrial world growing dependence on a few countries set the stage for the Arab oil embargo, when crude oil prices rose from \$3 per barrel in 1973 to \$40 a barrel in 1981. This sparked the need for renewable energy sources and energy efficiency.

Among the various renewable energy sources solar power stands out because the source of energy is unlimited and available everywhere. It is versatile in terms of both large scale and small scale power generation. The challenges of solar power are its cost and storage.

## **1.1 Photovoltaics**

Photovoltaics is an approach to convert sunlight directly into electricity. The advantages of PV are its high reliability, low operation cost and non-polluting nature. The PV effect was first discovered by a French physicist Becquerel in 1839. German scientist Heinrich Hertz experimented with selenium electrodes and this led to the development of the first primitive PV cell. These cells had only about 1~2% efficiency. In 1954 Bell labs came up with the first silicon solar cells with efficiency of 6%[1]. The space race between the United States and the Soviet Union led to the use of solar cells as a power source in space. PV systems were selected for space use because they were lightweight, which kept operational costs down and because they could produce power for long periods of time.

The main driving force behind the use of photovoltaics for terrestrial power supplies came in 1973 with the notorious oil shock. Since then all possible options for cost reduction have been explored, which was recognized as the major obstacle to the widespread use of photovoltaics.

## **1.2 Thin Film Photovoltaics**

Great efforts are being taken for the development of thin film solar cells. The greatest motivation of this being the cost reduction and energy savings during cell manufacture. All the thin film compound semiconductors being researched are direct band gap semiconductors. So the absorption of sunlight occurs within a few microns. One of the major hurdles that this technology suffers from is that most of the thin film semiconductors are polycrystalline. This leads to a loss in efficiency due to grain

boundary recombination. Some of the promising materials for thin film solar cells are amorphous silicon, cadmium telluride,  $\text{CuInSe}_2$  and its alloys. The maximum reported efficiency for a thin film solar cell is a CIGS based solar cell and the efficiency is 18.8% [2]. Figure 1.1 lists the highest independently confirmed efficiencies for solar cells and submodules.

Classification <sup>a</sup>	Effic <sup>b</sup> (%)	Area <sup>c</sup> (cm <sup>2</sup> )	V <sub>oc</sub> (V)	J <sub>sc</sub> (mA/cm <sup>2</sup> )	FF <sup>d</sup> (%)	Test Centre <sup>e</sup> (and Date)	Description
<b>Silicon Cells</b>							
Si (crystalline)	24.7 ± 0.5	4.00 (da)	0.706	42.2	82.8	Sandia (3/99)	UNSW PERL <sup>3</sup>
Si (multicrystalline)	19.8 ± 0.5	1.09 (ap)	0.654	38.1	79.5	Sandia (2/98)	UNSW/EuroSolar <sup>3</sup>
Si (supported film)	16.6 ± 0.5	0.98 (ap)	0.608	33.5	81.5	NREL (3/97)	AstroPower (Si-Film) <sup>4</sup>
<b>III-V Cells</b>							
GaAs (crystalline)	25.1 ± 0.8	3.91 (t)	1.022	28.2	87.1	NREL (3/90)	Kopin, AlGaAs window
GaAs (thin film)	23.3 ± 0.7	4.00 (ap)	1.011	27.6	83.8	NREL (4/90)	Kopin, 5 mm CLEFT <sup>5</sup>
GaAs (multicrystalline)	18.2 ± 0.5	4.011 (t)	0.994	23.0	79.7	NREL (11/95)	RTI, Ge substrate <sup>6</sup>
InP (crystalline)	21.9 ± 0.7	4.02 (t)	0.878	29.3	85.4	NREL (4/90)	Spire, epitaxial <sup>7</sup>
<b>Polycrystalline Thin Film</b>							
CIGS (cell)	18.4 ± 0.5	1.04(t)	0.669	35.7	77.0	NREL (2/01)	NREL, CIGS on glass <sup>8</sup>
CIGS (submodule)	16.6 ± 0.4	16.0 (ap)	2.643	8.35	75.1	FhG-ISE (3/00)	U. Uppsala, 4 serial cells <sup>9</sup>
CdTe (cell)	16.4 ± 0.5	1.131 (ap)	0.848	25.9	74.5	NREL (2/01)	NREL, on glass
CdTe (submodule)	10.6 ± 0.3	63.8(ap)	6.565	2.26	71.4	NREL (2/95)	ANTEC <sup>10</sup>
<b>Amorphous Si</b>							
a-Si (cell) <sup>f</sup>	12.7 ± 0.4	1.0 (da)	0.887	19.4	74.1	JQA (4/92)	Sanyo <sup>11</sup>
a-Si (submodule) <sup>f</sup>	12.0 ± 0.4	100 (ap)	12.5	1.3	73.5	JQA (12/92)	Sanyo <sup>12</sup>
<b>Photochemical</b>							
Nanocrystalline dye	6.5 ± 0.3	1.6(ap)	0.769	13.4	63.0	FhG-ISE (1/97)	INAP
Nanocrystalline dye (submodule)	4.7 ± 0.2	141.4 (ap)	0.795	11.3	59.2	FhG-ISE (2/98)	INAP
<b>Multijunction Cells</b>							
GaInP/GaAs	30.3	4.0 (t)	2.488	14.22	85.6	JQA (4/96)	Japan Energy (monolithic) <sup>13</sup>
GaInP/GaAs/Ge	28.7 ± 1.4	29.93(t)	2.571	12.95	86.2	NREL (9/99)	Spectrolab (monolithic)
GaAs/CIS (thin film)	25.8 ± 1.3	4.00 (t)	-	-	-	NREL (11/89)	Kopin/Boeing (4 terminal)
a-Si/CIGS (thin film) <sup>f</sup>	14.6 ± 0.7	2.40 (ap)	-	-	-	NREL (6/88)	ARCO (4 terminal) <sup>14</sup>

Figure 1.1 Confirmed Terrestrial Cell and Submodule Efficiencies [3]

### 1.3 $\text{CuInSe}_2$ and its Family

CIS a ternary Semiconductor, with a direct band gap of 1.0 eV is known to absorb light in the solar spectrum better than any other semiconductor. CIS has the highest reported absorption coefficient of  $3.6 \times 10^5 \text{cm}^{-1}$  [5]. The fact that these thin film cells gave efficiencies with no degradation being observed increased the research activity in this field.



The typical structure of CIS based solar cells is: Soda lime glass substrate (SLG)\ Molybdenum\ CIS layer\ CdS\ ZnO. The CdS layer acts as the n-type partner to the p-type CIS absorber layer. Molybdenum acts as the back contact and the ZnO layer acts as the front contact. The light is incident through the ZnO layer.

The CIS takes the chalcopyrite structure, which is a diamond like lattice with a face-centered tetragonal unit cell.

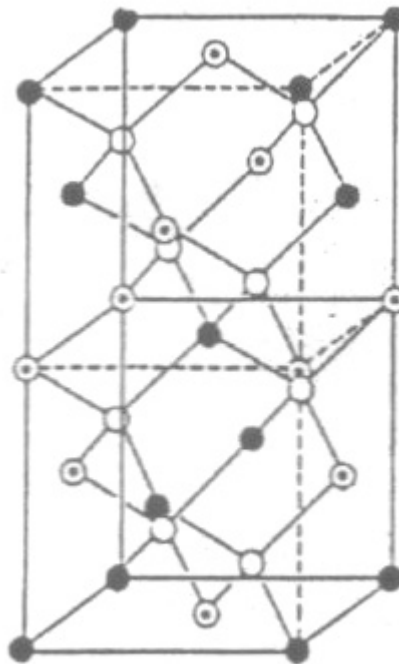


Figure 1.2 CIS Structure [4]

There are various native defects in CIS. Some of them are:

- 1 Copper Vacancies ( $V_{Cu}$ ): This is an acceptor defect
- 2 Copper on Indium antisite defect ( $Cu_{In}$ ): This is an acceptor defect

- 3 Indium on Copper antisite defect ( $\text{In}_{\text{Cu}}$ ): This is a donor defect
- 4 Selenium vacancies ( $\text{V}_{\text{Se}}$ ): This is a donor defect

CIS can be made highly conductive and p-type by depositing more copper than Indium. But this results in degradation of device performance. This is because of the formation of Copper Selenide, which being highly conductive tends to short circuit the junction. The formation of copper selenide can be avoided by having more Indium than Copper but the resulting material has a high compensation effect. This is due to the presence of both  $\text{V}_{\text{Cu}}$  and  $\text{In}_{\text{Cu}}$ . The former is acceptor defect and the latter is a donor defect. For good device performance the Cu/In ratio is kept close to unity. CIS, when properly formed, tends to be p-type because of the low formation energy of copper vacancies.

One of the drawbacks of the CIS cells is its low open circuit voltage. This is because of its low bandgap. This led to the incorporation of Gallium in the ternary CIS semiconductor resulting in the formation of the quaternary CIGS semiconductor. The incorporation of Gallium is done in such a way that it is used to substitute an equivalent amount of Indium. This substitution raises the bandgap of the material. The bandgap can be varied from 1.02eV (CIS bandgap) to 1.7eV (CGS bandgap). The bandgap variation for  $\text{CuIn}_{(1-x)}\text{Ga}_x\text{Se}_2$  is given by

$$E_g = 1.011 + 0.664x - 0.249x(1-x) \quad (\text{eq 1.1}) [6]$$

In addition to improving the  $\text{V}_{\text{oc}}$ 's, the incorporation of Gallium helps in improved adhesion to the Molybdenum back contact. It also results in changes in material properties like lattice constant, film morphology and defect mechanisms. The gallium profile in the absorber can be varied by using different processing techniques. This is

referred to as Gallium grading. Increasing the gallium content increases the bandgap by predominantly shifting the conduction band, shown in figure 1.2. Thus Gallium grading helps to build quasi-electrostatic fields, which enhances current collection.

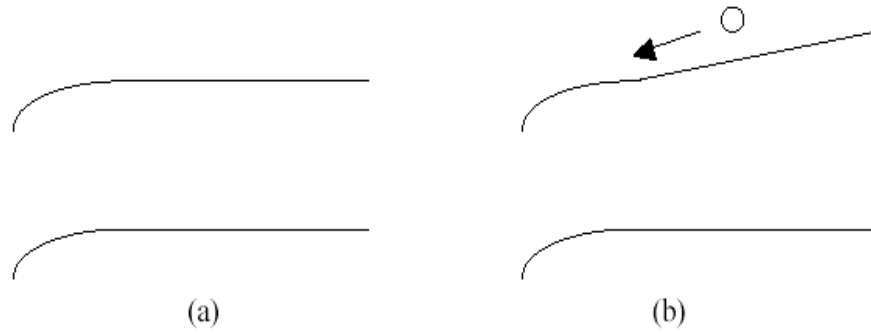


Figure 1.3 Band Bending a) Without Grading b) With Grading

T.Dullweber et al. [7] have studied various graded absorber layers like a linearly graded absorber, multi-graded absorber and a double graded absorber. The output parameters show a strong relation to the slope of grading in a linearly graded absorber. While in a multigraded absorber, the current is dominated by the minimum bandgap and the open circuit voltage is dominated by the bandgap in the space charge region. They also concluded that the 3 stage process shows more limitation to a design of graded bandgap structures as opposed to co-evaporation.

### 1.3.1 Role of Sodium

During the growth of CIGS film, at elevated temperatures of processing, Na tends to diffuse out of SLG through the back contact and into the semiconductor material [8]. The common methods used to analyze the role of Sodium in CIGS films is to use barrier

layers on the substrate to block the diffusion of Sodium from the substrate or use substrates other than SLG[9]. The presence of Na in polycrystalline CIGS based photovoltaic devices correlates with numerous changes in material and device quality. The observed changes include increase in conversion efficiencies[10], grain size, preferential orientation[11] and a reduced sensitivity of devices to the metal ratio[12].

Some of the possible mechanisms by which Na works are

1. Zhang/ Wei/ Zunger defect pair model ( $2 V_{Cu} - In_{Cu}$  pair dominance)[32] : Na can take up intended Cu positions in the lattice[13]. This results in a reduced defect pair formation. Thus affecting the hole density and leading to an increase in  $V_{oc}$  and fill factor.
2. Neumann defect pair model ( $Cu_{In} - In_{Cu}$  pair dominance) [14]: Na replaces Cu in the lattice. It follows that the number of defect pair is reduced, reducing the cation disorder and enhancing  $V_{oc}$  and fill factor.
3. Na acts as catalyst in the passivation of  $V_{Se}$  by oxygen [15].
4. U. Rau et al have observed the formation of a acceptor level at about 75mev above the valence band, which they attribute to the increase in the carrier concentration in the absorber material [16].

## CHAPTER 2

### PHYSICS OF SEMICONDUCTOR AND SOLAR CELLS

At low temperatures, electrons in a crystal occupy the lowest possible energy states. The occupation of energy states is in accordance with Pauli's exclusion principle. According to this principle each allowed energy level can be occupied by two electrons of opposite spin.

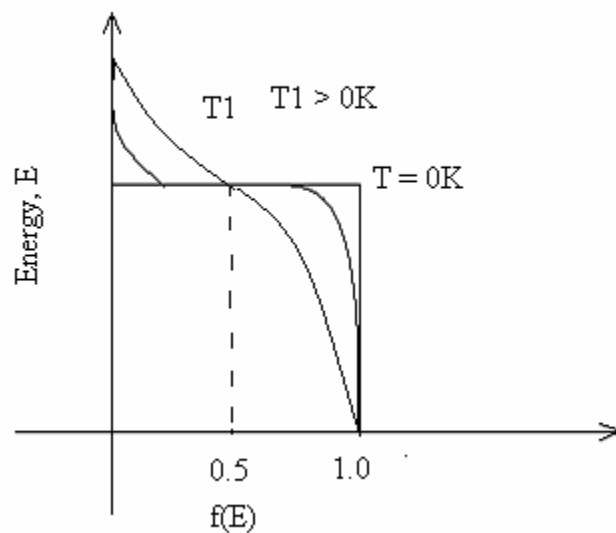


Figure 2.1 Variation of Fermi-Dirac Distribution Function With Temperature

Thus at low temperatures ( $T=0K$ ), all the energy levels upto a certain energy level are filled with two electrons. This energy level is known as Fermi level. But as the temperature increases, energy levels higher than the fermi energy ( $E_F$ ) will have a finite probability of having an electron, and energy levels less than  $E_F$  will have a finite probability of being empty. The Fermi distribution function  $f(E)$  is given by Eq. 2.1 and the variation of Fermi energy with temperature is shown in fig. 2.1.

$$f(E) = 1 / (1 + e^{(E - E_F) / KT}) \quad (\text{Eq. 2.1})$$

For a conduction band to contribute to current flow in a crystal it cannot be either completely full or completely empty.

A semiconductor is a material which has a narrow forbidden band gap between the conduction and valence bands. The energy band structure of a semiconductor is shown in figure 2.2. At higher temperature they have sufficient smearing out of the Fermi Dirac distribution function. This will ensure that some of the electrons from a completely filled valence band have moved to the conduction band, which has a lot of unoccupied energy states, thus enabling current flow.

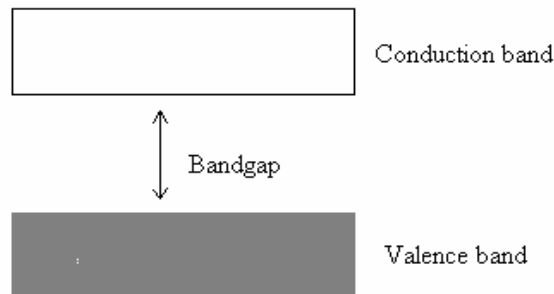


Figure 2.2 Representation of Semiconductor

## **2.1 Concept of Holes**

To understand the concept of holes let us consider the Silicon crystal structure. Silicon belongs to group IV of the periodic table and has 4 electrons in its outermost shell. Thus to complete its octet it makes covalent bonds with 4 neighboring silicon atoms. The semiconductor thus formed cannot conduct electricity. But at higher temperatures, if some electrons can gain enough energy to break free from the covalent bond, they can contribute to current flow. If the neighboring electrons can jump from their bond to the broken bond they can contribute to current flow as well. The electrons being released from the bond can be recognized as being in the conduction band. The broken bond can be termed as a hole and they can be recognized as being in the valence band.

## **2.2 Doping of Semiconductors**

Electronic properties of semiconductors can be altered by adding impurities to them. These impurities are referred to as dopants. These added impurities are either squeezed between the atoms of the host material, which are then referred to as the interstitial impurities or they can replace the atoms in the host crystal in which case they are called substitutional impurities.

To understand the effects of dopants let us again consider a Silicon lattice. When a group V atom replaces a Silicon atom, 4 of its electrons are used up to form covalent bonds while the fifth electron is bonded to the atom. Thus it is not free to move about in the lattice. The energy required to release the electron to the conduction band is very low,

typically in the range of a few meV below the conduction band. This type of semiconductor is referred to as n-type semiconductor.

In the analogous way when a group III atom replaces a silicon atom in the crystal lattice, it does not have sufficient electrons to form 4 covalent bonds. This creates a hole in the valence band. Thus an energy level is created, which is a few meV above the valence band. Depending on the level of doping the fermi level tends to go closer to valence band. This type of semiconductor is called a p-type semiconductor.

### 2.3 p-n Junction

When a p-type material and a n-type material are made to come together, a p-n junction is formed. The Fermi levels of both the materials will line up. The electrons from the n-type material move to the p-type material leaving behind ionized donors. On the other hand holes from the p-type material would move to the n-type material leaving behind ionized acceptors. The region of ionized acceptors and ionized donors, put together, is referred to as the space charge region and is shown in fig. 2.3. The charges on both sides give rise to an electric field. This field will oppose the natural diffusion tendency of the majority carriers. The diffusion potential or built-in potential is given by eq 2.2 and this difference in potential produces a bending of energy bands in the semiconductor, which is shown in fig. 2.3.

$$V_{bi} = \frac{KT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (\text{eq 2.2})$$

The width of the space charge region is given by

$$W = \frac{[2\epsilon (V_{bi} - V) (N_A + N_D)]^{1/2}}{[q N_A N_D]^{1/2}} \quad (\text{eq 2.3})$$



Where:

$N_D$  is Donor impurity concentration on the n-side

$N_A$  is Acceptor impurity concentration on the p-side

$V$  is Applied Voltage

$K$  is Boltzmann's constant

$n_i$  is intrinsic carrier concentration

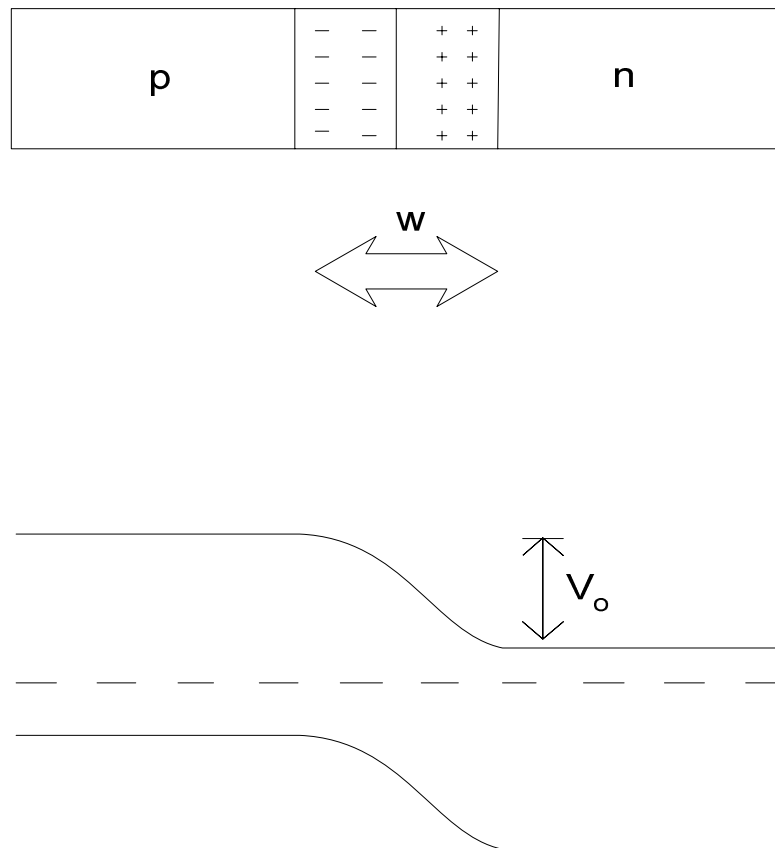


Figure 2.3 Metallurgical Junction and Band Bending in p-n Junction

## 2.4 Effect of Bias

In forward bias, (i.e) when a negative potential( $V_f$ ) is applied to the n-region with respect to the p-region, the band bending reduces as compared to its thermal equilibrium position. This means that the potential difference between the ends of the diode is reduced. The reduction of potential difference is equal to the applied voltage. Thus there is a reduction of the barrier height for the majority carriers. The reduced barrier height for roughly the same carrier concentration gradient, yields an increase in the diffusion current of majority carriers. The drift current, which oppose the diffusion current, is relatively insensitive to the change in barrier height and is the same as its thermal equilibrium value. In reverse bias, i.e when a positive voltage to the n-region with respect to the p-region, the band bending increases thus the diffusion current becomes negligible. The drift current as already mentioned is insensitive to the changes in band bending so they remain at there thermal equilibrium value. Thus in reverse bias a small negative current flows, this current is often referred to as the reverse saturation current  $I_0$ . The current in a p-n junction in the dark can be given by

$$I = I_0 \exp(qV/KT - 1) \quad (\text{eq 2.4})$$

## 2.5 Heterojunction

A heterojunction is a junction formed between two dissimilar semiconductors. When the two semiconductors have the same type of conductivity it is called an Isotype heterojunction. When the conductivity types differ it is called anisotype heterojunction. Heterojunction devices are extensively used in Injection lasers, light emitting diodes,

photodetectors and solar cells. The major problems of heterojunction devices are the lattice mismatch and differences in electron affinity, which gives rise to energy band discontinuities.

Let us consider two semiconductors of band gap  $E_{g1}$  and  $E_{g2}$  having electron affinities  $X_1$  and  $X_2$  respectively being partnered together to form a heterojunction. The Energy band diagram of the two semiconductors before and after forming the heterojunction is shown in Figures 2.4 and 2.5. It can be seen that there is a discontinuity in the valence band ( $\Delta E_v$ ) and conduction band ( $\Delta E_c$ ). Such discontinuities are due to the inherent differences in properties of the two semiconductors, such as the electron affinity. The impact of the discontinuity is that it hinders carrier flow when a solar cell is placed under illumination. Hence, proper selection of materials is an important criterion.

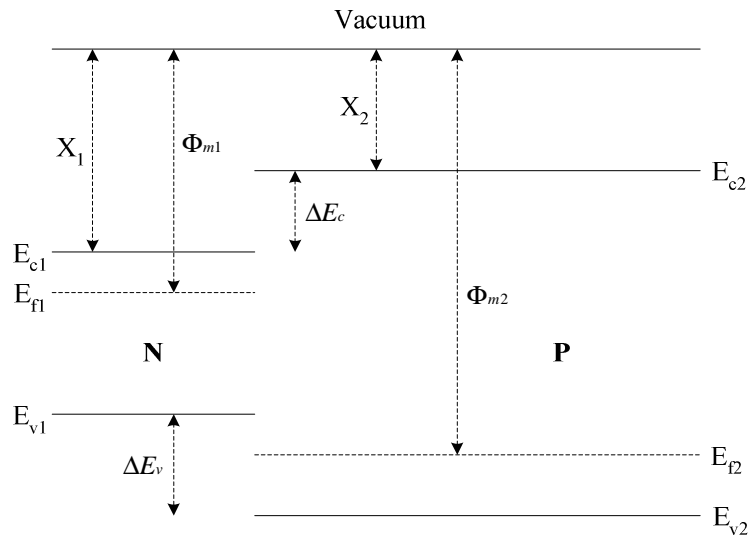


Figure 2.4 Two Semiconductors Before Heterojunction Formation [17]

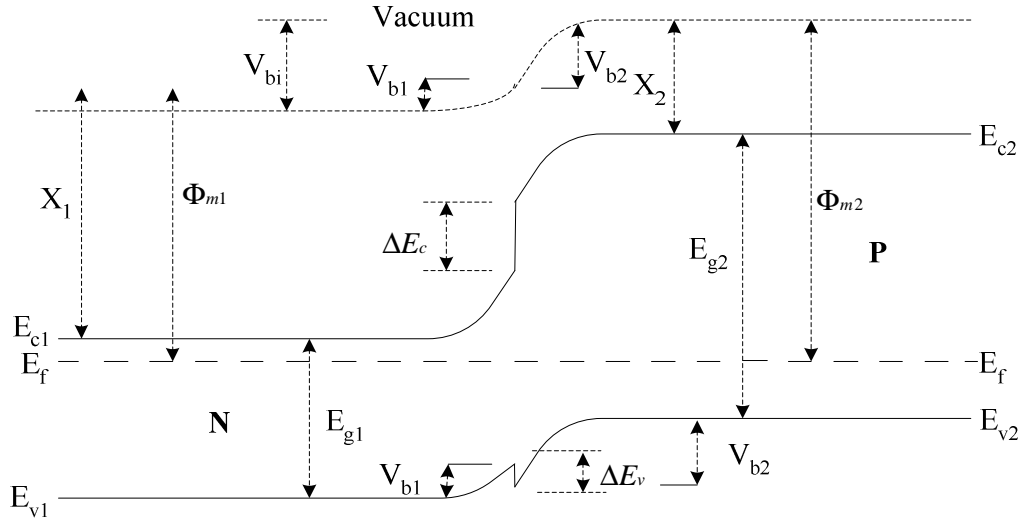


Figure 2.5 Band Diagram of p-n Heterojunction [17]

The discontinuities are given by

$$\Delta E_c = X_1 - X_2 \quad (\text{eq 2.5})$$

$$\Delta E_v = (E_{g2} - E_{g1} - \Delta E_c) \quad (\text{eq 2.6})$$

The total built in potential,  $V_{bi}$ , is equal to the sum of partial built in voltages ( $V_{b1}$ ,  $V_{b2}$ ), where  $V_{b1}$  and  $V_{b2}$  are electrostatic potentials of two semiconductors.

In this research a p-CIGS/n-CdS anisotype heterojunction has been studied The band diagram of this heterojunction with n-type ZnO front contact is shown in Figure 2.6

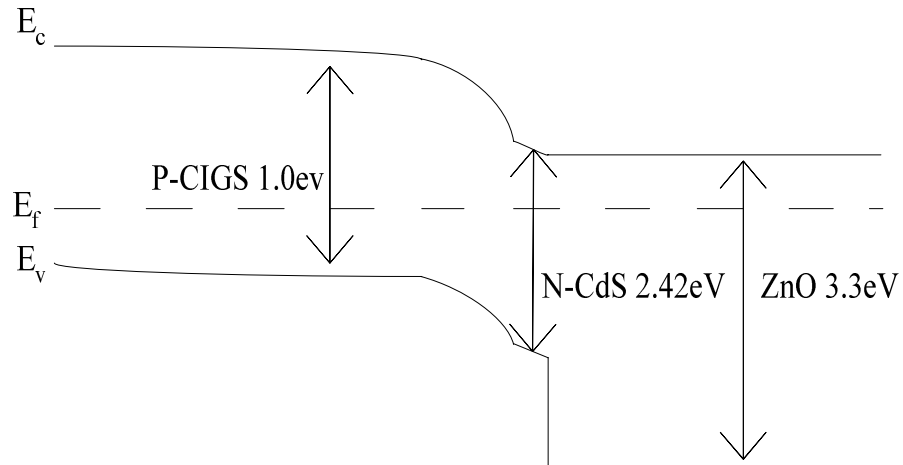


Figure 2.6 Band Diagram of p-CIGS / n-CdS Heterojunction Solar Cell

## 2.6 Solar Cells

The photovoltaic effect is the process of conversion of light energy into electricity. One of the ways of doing this is by using a solar cell. A solar cell is a device, which is made by partnering a p-type semiconductor and n-type semiconductor. The semiconductors are chosen such that one of the semiconductors absorb a significant portion of the light spectrum. Absorption of light depends on the bandgap of the material. If the bandgap is greater than the energy of the photon, light just passes through. On the contrary, if the bandgap is less than the energy of the photon, the photon is absorbed. The absorbed photon gives rise to Electron-Hole pairs(EHP) . These excess carriers are swept across the junction by the electric field and are collected at the contacts. This gives rise to photocurrent and can be made to deliver power to a load. Thus the important steps in solar energy conversion are

- 1 Absorption of radiation
- 2 Generation of carriers

- 3 Diffusion of minority carriers to the edge of the depletion width
- 4 Separation of minority carriers by the electric field.
- 5 Collection of carriers at the contact.

The absorption of light by a semiconductor can be described by the relation

$$I = I_0 [\exp(-\alpha(\lambda)t)] \quad (\text{eq 2.7})$$

$I_0$  - Intensity of light incident on the semiconductor

$\alpha$  – Absorption coefficient which is a function of wavelength

$t$  – Depth of material from surface of incidence.

## 2.7 Spectral Response

When monochromatic light of wavelength  $\lambda$  is incident on a semiconductor, EHP's are generated at a distance  $x$  from the semiconductor surface. The generation rate of these carriers is given by

$$G(\lambda, x) = \alpha(\lambda) F(\lambda) [1 - R(\lambda)] e^{-\alpha(\lambda) x} \quad [17] \quad (\text{eq 2.8})$$

$F(\lambda)$  – No. of incident photons /  $\text{cm}^2$  / s / unit bandwidth

$R(\lambda)$  – Fraction of these photons reflected from surface

Assuming a low injection condition, The spectral response can be given by

$$SR(\lambda) = (1 / q F(\lambda) [1 - R(\lambda)]) [J_p(\lambda) + J_n(\lambda) + J_{dr}(\lambda)] \quad (\text{eq 2.9})$$

$J_p(\lambda)$  – Photocurrent contribution from p-region

$J_n(\lambda)$  – Photocurrent contribution from n-region

$J_{dr}(\lambda)$  – Photocurrent contribution from depletion region

The photocurrent density can be obtained by

$$J_L = q \int F(\lambda) (1 - R(\lambda)) SR(\lambda) d\lambda \quad (\text{eq 2.10})$$

## 2.8 I – V Characteristics

When light is incident on a solar cell electron-hole pairs are generated. This gives rise to a current. In order to account for this current the dark current equation is modified as

$$I = I_0 \exp\left(\frac{qV}{kT} - 1\right) - I_L \quad (\text{eq 2.11})$$

The I-V characteristic of a solar cell in dark and light is shown in the following figure.

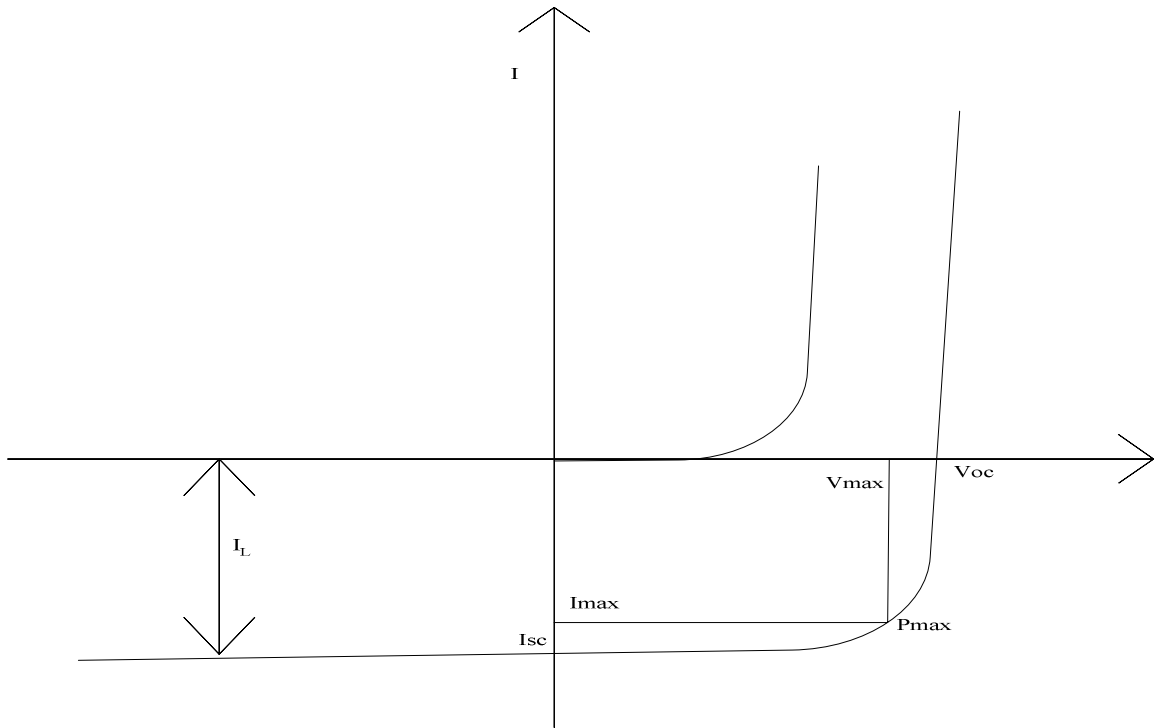


Figure 2.7 I – V Characteristic of a Solar Cell in Dark and Light

If  $L_p$  and  $L_n$  are the minority carrier diffusion lengths of holes and electrons respectively,  $W$  is the depletion width and  $G$  is the generation rate of EHP's, Then

$$I_L = q A G (L_n + L_p + W) \quad [18] \quad (\text{eq 2.12})$$

Thus it can be seen that the depletion region and the volume of material lying within a diffusion length on either side of the depletion region can be referred to as the active collection region of a p-n junction solar cell.

## 2.9 Equivalent Circuit of a Solar Cell

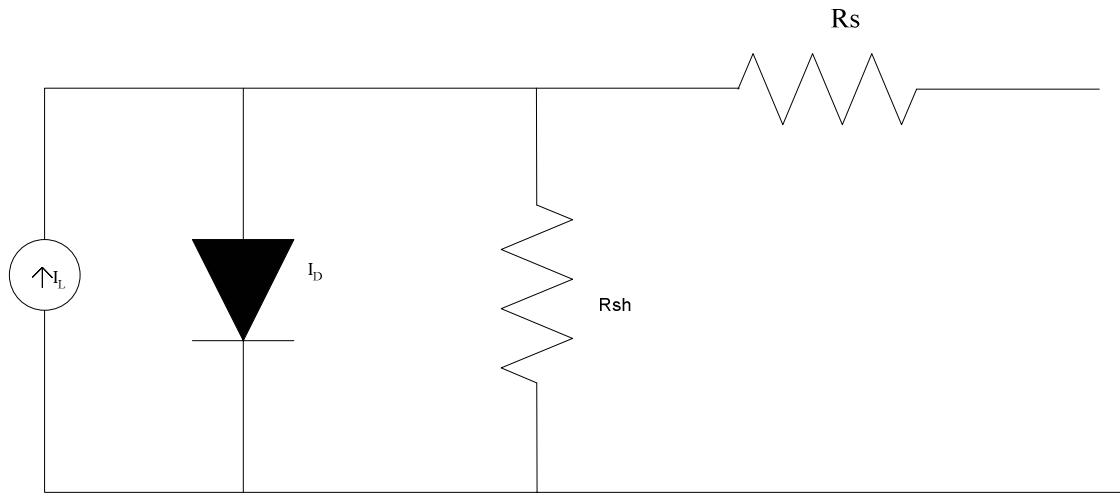


Figure 2.8 Equivalent Circuit of a Solar Cell

Figure 2.8 shows the equivalent circuit of a solar cell. The photocurrent  $I_L$  is represented by a current generator. A diode is in parallel with the current generator. There are two resistances, one is the series resistance and other is the shunt resistance. Series resistance  $R_s$ , takes into account the bulk resistance from the absorber and the resistances from the contact materials. Ideally the value of this parameter should be zero.  $R_{sh}$  is the shunt resistance which accounts for any parallel paths across the junction. Ideally this value should be infinity.



## 2.10 Output Parameters of a Solar Cell

The current flowing in a solar cell under illumination is given by

$$I = I_0 \exp((qV/nkT) - 1) - I_L \quad (\text{eq 2.13})$$

where  $n$  is the diode ideality factor.

The first term gives the voltage driven current. The second term gives the light generated current. The short circuit current is the current generated by the light and is given by the term  $I_{SC}$ .

$$I_{SC} = I_L \quad (\text{eq 2.14})$$

The open circuit voltage,  $V_{OC}$ , is obtained by setting  $I = 0$  in eq 2.13

$$V_{OC} = kT / q \ln[ (I_L / I_0) + 1 ] \quad (\text{eq 2.15})$$

It can be seen that  $V_{OC}$  depends on the properties of the semiconductor by the virtue of its dependence on  $I_0$ .

The output power at any point in the 4<sup>th</sup> quadrant is given by the area of a rectangle. At one point the output power is maximum. This leads to the definition of the other output parameter, the fill factor (FF).

$$FF = (V_{MP} I_{MP}) / (V_{OC} I_{SC}) \quad (\text{eq 2.16})$$

The conversion efficiency is given by

$$\eta = FF V_{OC} I_{SC} / P_{IN} \quad (\text{eq 2.17})$$

## 2.11 Loss of Efficiency

One of the major loss mechanisms in a solar cell is the recombination in the bulk semiconductor. From the point of generation some of the carriers get recombined before reaching the terminal. The lower the recombination rate in both the bulk and surface,

higher is the  $V_{OC}$  and  $J_{SC}$  . Recombination in the depletion region through trapping levels can limit the  $V_{OC}$  and  $J_{SC}$  as well.

## CHAPTER-3

### DEVICE STRUCTURE AND FABRICATION OF OUR SOLAR CELLS

#### 3.1 Device Structure

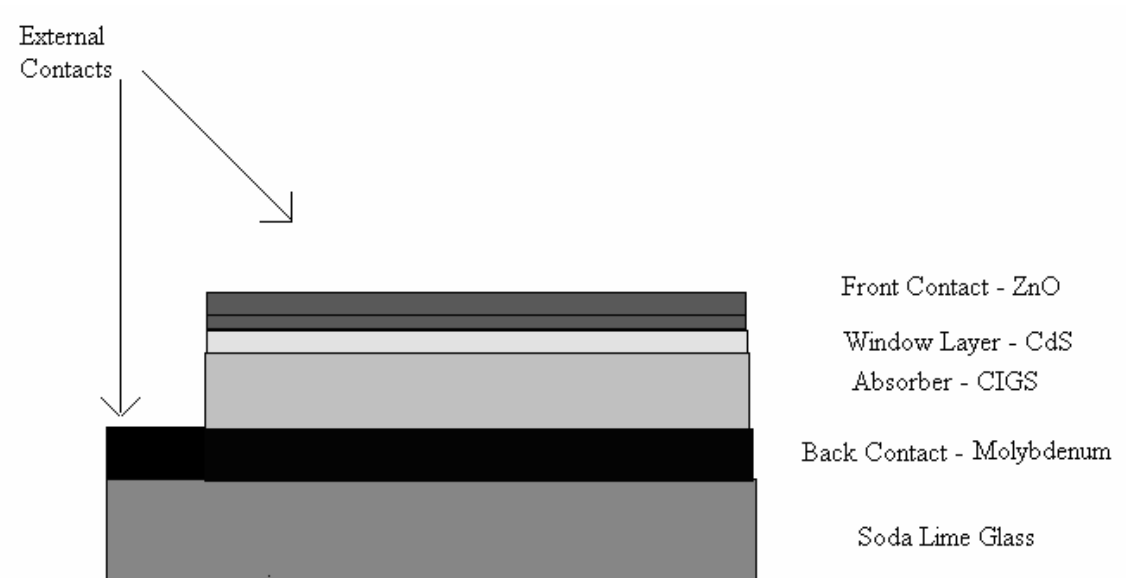


Figure 3.1 Device Structure

The above figure shows the structure of the solar cells fabricated in our laboratory. On a 2mm thick Soda lime glass substrate a thin layer of Molybdenum back contact is deposited. Then the CIGS absorber layer is deposited. Following this, the n-type CdS buffer layer is deposited. Finally the ZnO front contact is deposited.

### 3.1.1 Molybdenum Back Contact

Some of the requirements of a good back contact material for CIGS solar cells are

1. To form an ohmic contact
2. Low recombination rate for minority carriers
3. Certain inertness, to the corrosive atmosphere which the material is being exposed to, during CIGS deposition

Molybdenum was the popular choice as back contact material because it fulfilled all the requirements. Jaegermann et al.[19] have reported that a schottky barrier is formed for an intimate p-CIS / Mo contact. This is not in agreement with the fact that an ohmic back contact is necessary for obtaining high efficiency CIGS solar cells. T. Wada et al[20] have investigated the CIGS / Mo interface and have concluded that the CIGS / Mo heterocontact including the MoSe<sub>2</sub> layer is not a schottky type contact but a favorable ohmic contact.

K.Orgassa [21] et al. investigated W, Mo, Ta, Nb, Cr, V, Ti and Mn as possible back contact material for CIGS solar cells. All the films were deposited by electron beam evaporation on soda lime glass. Subsequently CIGS layer was deposited by co-evaporation, CdS by CBD and ZnO by RF sputtering. They have concluded that Ti, V, Cr and Mn tend to react with Selenium during absorber growth thus affecting the absorber growth. Devices with Ta and Nb back contact showed good performance only with graded bandgap absorber. Devices with a tungsten back contact showed comparable performance as devices with a Mo back contact, with and without bandgap grading. The authors have also established a relation to calculate the current density loss due to the back contact.

$$J_{\text{loss}} = q \int f_{1.5}(\lambda) A_{\text{BC}} d\lambda \quad (\text{Eq. 3.1})$$

$A_{\text{BC}}$  -: Optical absorbance of the back contact in the solar cell. This can be calculated from energy flux balance into and out of this layer.

$f_{1.5}(\lambda)$  -: Spectral photon flux density of AM1.5 spectral intensity distribution.

$J_{\text{loss}}$  is dependent on the thickness of the absorber layer. For a thick absorber  $J_{\text{loss}}$  is zero.

But as the thickness starts to reduce  $J_{\text{loss}}$  begins to increase depending on the reflective property of the metal.

Hamda A Al-Thian et al.[22] have studied the effect of various sputtering pressures during deposition and its influence on Na out diffusion during the CIGS deposition process and its subsequent effect on CIGS device performance. Molybdenum thin films were deposited at various pressures from 0.6mT to 16mT and complete devices were fabricated on these substrates. The CIGS absorber layer for these devices was fabricated by the 3-stage process. They found that the level of Na in the absorber layer had a direct correlation to the sputtering pressure. Samples with the molybdenum sputtered under 0.6mT, showed lower sodium counts as opposed to samples with molybdenum sputtered under 8mT of argon pressure. This has been attributed to the variation in structure of moly with the variation in pressure. Moly sputtered at 0.8mT had a dense, small grain structure with close grain boundaries. Films sputtered at 5mT had porous and fibrous grains with valleys. Films sputtered at 8mT had open columnar structure, consisting of free standing columns, with an increasing amount of column boundary voids. They concluded that the correct sputtering pressure for the best device performance was 5mT.

Scofield et al.[23] investigated the electrical and mechanical properties of molybdenum and concluded that the resistivity of molybdenum thin films increased beyond sputtering pressures of 2mT. Films deposited at higher pressures passed the adhesion test. The stress was compressive at 0.2mT and 20mT but went through a cycle of tensile stress with the maximum tensile stress at 2mT.

Since we have already dealt with CIS in chapter 1 we will move on to Cadmium Sulphide.

### **3.1.2 Cadmium Sulphide**

CdS is widely used as the n-type semiconductor material to form a p-n junction with p-type CIGS absorber material. CdS is a direct bandgap material with a bandgap of 2.4ev. It has a wurzite structure. It has an absorption edge of 510nm. Thus some of the light in the blue region is absorbed in the CdS layer. These absorbed photons can generate carriers, most of which is lost due to recombination.

There are many ways to deposit CdS namely chemical bath deposition (CBD), sputtering and closed space sublimation (CSS). Of these CBD is the most widely used technique because of its uniformity, ease of deposition and the elimination of the use of vacuum equipment. The lattice constant of CdS is close to that of CIGS, thus the interface between the two will have lower defect density. The disadvantages of CdS are

1. Its bandgap limits the short wavelength part of solar spectrum from reaching the absorber, leading to a loss of current.
2. The generation and disposal of large quantities of hazardous waste.
3. The CBD method has a low material yield (cadmium acetate - 27% ; thiourea – 0.34%)[28]

From an industry standpoint both the low yield and high amount of toxic waste cause high production costs as well as environmental problems.

To circumvent these problems K.Ramanathan et al.[24] have investigated a surface treatment technique. CIGS thin films were treated in an aqueous solution containing Cd or Zn ions followed by the completion of the solar cell with the ZnO layer. They have observed an increase of  $2\text{mA}/\text{cm}^2$  in  $J_{sc}$ , when compared to CdS containing cells, due to absence of losses in the blue region. But the cells with partial electrolyte treatment show lower open circuit voltages and fill factor. This they have attributed to the nature of the interface created by dissimilar materials and to defect states introduced during the processing steps.

A.E. Delahoy et. al.[25] have investigated ZIS,  $\text{In}_2\text{Se}_3$ , and ZnSe as possible candidates to replace the CdS buffer layer. Devices with all these materials as a buffer layer have lower efficiency as compared to CdS. Out of these materials the most promising material is ZIS. The performance of devices with ZIS had 9.9% efficiency while the CdS containing devices had an efficiency of 10.4%. T.Nakada et al.[31] have reported an efficiency of 17.7% with a ZnS buffer layer deposited by CBD.

The difficulty in replacing CBD CdS arises from the fact that the process confers many benefits:

1. Cleaning of the CIGS surface
2. Conformal coverage
3. Protection against sputtering
4. Defect passivation (Surface and grain boundaries)

5. Provision of a conduction band edge 0.2-0.3 eV higher than CIGS to avoid recombination under forward bias.

### **3.1.3 ZnO Front Contact**

Two of the primary requirements of a good front contact are:

1. High conductivity
2. Transparency to incident photons.

ZnO is one of the widely used front contact material for CIGS based solar cells. It has a bandgap of 3.3eV. It has good optical and electrical properties. ZnO films show a transmission of about 90% between 400-1000nm. The transmission begins to drop at higher wavelengths, due to free carrier absorption, which increases with increase in doping. Thus a compromise has to be made in terms of low resistivity and free carrier absorption.

## **3.2 Device Fabrication**

### **3.2.1 Substrate Cleaning**

Cleaning of contaminants in the substrate is a very crucial step and has to be done with utmost care as this has a direct impact on device performance. Soda lime glass substrates of dimensions 4" x 2" x 2mm were cut using a diamond scribe. These substrates are soaked in a bath containing de-ionized water and micro-90 cleaning agent. The typical concentration of the cleaning agent in the bath is approximately 2%. The substrates remain soaked in the bath for 3 hrs. The substrates are scrubbed thoroughly. The substrates are then placed in an ultrasonic bath, containing a solvent like 2-propanol,



for 20 min. This step is done to eliminate organic impurities and some contaminants left by the cleaning agent itself. Then the substrates are placed in a hot water bath, maintained at 70°C, for 30 min. After this the substrates are placed, in DI water. The substrates are blown dry using dry nitrogen before subsequent processing.

### **3.2.2 Molybdenum Deposition**

The chamber used for molybdenum deposition has a load lock and a main chamber. In the load lock the substrate is heated to 150°C using a time temperature profile. Approximately 1.5mT of Ar is allowed to flow for 25min. This is done in order to get rid of any moisture in the substrate. Subsequently, the substrate is transferred to the main chamber. The main chamber is pumped down approximately to 5 microtorr before deposition. DC magnetron sputtering is used to deposit 1micron of molybdenum. A bi-layer of molybdenum is sputtered. The first layer is sputtered at 5mT and the second layer is sputtered at 1.5mT. The thickness of the first layer is 3000Å and the thickness of the second layer is 7500 Å. The first layer gives good adhesion but has a higher resistivity because of its less dense structure. The second layer has more dense structure and has a lower resistivity. Resistivity numbers of 5E-5 ohm-cm are routinely obtained in our process.

### **3.2.3 CIGS Absorber Deposition**

Our laboratory has developed a two stage manufacturing friendly process. In this process, the metal precursors are deposited sequentially followed by a selenization step. The manufacturing friendliness comes from the fact that this method does not use the

complex co-evaporation process and the metal precursors can be deposited by sputtering or by evaporation and toxic material like hydrogen selenide is not used. The co-evaporation process does not give a uniform coverage over a large area and it also needs very high degree of control.

### **3.2.3.1 CIGS Deposition**

2" X 2" molybdenum coated SLG substrate is loaded into CIGS deposition system. The chamber is pumped down to 1 microtorr. The substrate is heated to 275°C before starting deposition. The fabrication of the CIGS absorber layer is done by the two stage process. The first stage is the precursor formation where the metal precursors are deposited sequentially at 275°C. Following this is the second stage called the selenization. In the second stage the metal precursors are annealed at high selenium flux for 28min. The selenization is done in a specific time-temperature profile.

In the course of this research the CIGS absorber layer was fabricated by two methods. First, is the Type – 1 process and the second one is the Type - 4 (split In – split Ga) process.

### **3.2.3.2 Type – 1 CIGS vs. Type – 4 CIGS**

Type – 1 CIGS:

Precursor formation

1. The substrate temperature is held at 275°C.
2. 1,250 Å of Cu is deposited at 0.8 Å /s.
3. 800 Å of Gallium is deposited at 1.2 Å /s.
4. In, Se are co-evaporated until 3,100 Å of Indium is deposited at 2.3 Å /s.

## Selenization

1. Constant selenium flux of  $25 \text{ \AA} / \text{s}$  is maintained throughout selenization.
2. Temperature is ramped from  $275$  to  $450^\circ \text{C}$  in approximately 4min.
3. Temperature is held at  $450^\circ \text{C}$  for 7 minutes.
4. Ramp from  $450$  to  $550^\circ \text{C}$  in approximately 4minutes
5. Temperature is held at  $550^\circ \text{C}$  for 7 minutes.
6. At the end of 16<sup>th</sup> minute a thin layer of Cu called the top Cu is deposited
7. Cool down from  $550$  to  $425^\circ \text{C}$

Substrate is allowed to cool down to room temperature in vacuum.

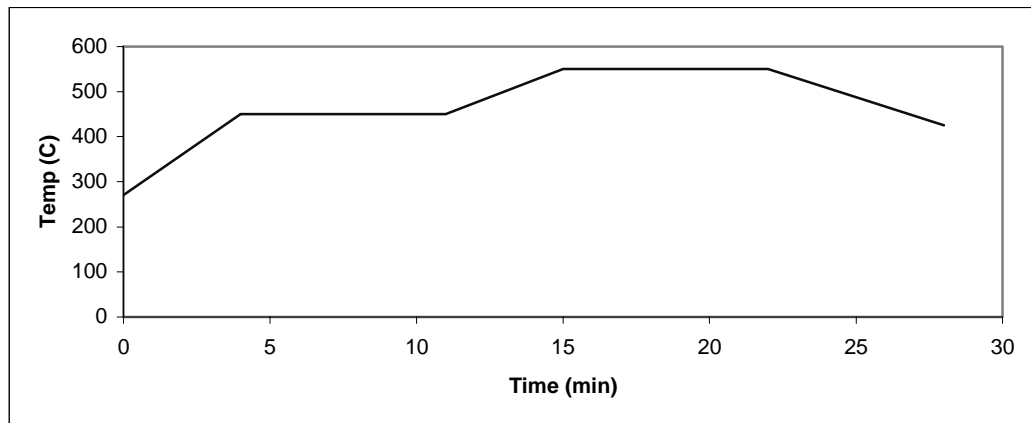


Figure 3.2 Selenization Profile

Type – 4 CIGS:

Precursor formation

1. The substrate temperature is held at  $275^\circ \text{C}$ .
2.  $1,250 \text{ \AA}$  of Cu is deposited at  $0.8 \text{ \AA} / \text{s}$ .
3. Approx.  $3/4^{\text{th}}$  of Gallium is deposited at  $1.2 \text{ \AA} / \text{s}$ .

4. In, Se are co-evaporated until 1550 Å of Indium is deposited at 2.3 Å /s.
5. Approx. 3/16<sup>th</sup> of Gallium is deposited at 1.2 Å /s.
6. In, Se are co-evaporated until 1550 Å of Indium is deposited at 2.3 Å /s.

#### Selenization

1. Constant selenium flux of 25 Å /s is maintained throughout selenization.
2. Temperature is ramped from 275 to 450°C in approximately 4min.
3. Temperature is held at 450°C for 7 min.
4. At the end of the 3<sup>rd</sup> min the remaining 1/16<sup>th</sup> of Gallium is deposited.
5. Ramp from 450 to 550°C in approximately 4min
6. Temperature is held at 550°C for 7min
7. At the end of 16<sup>th</sup> minute a thin layer of Cu called the top Cu is deposited
8. Cool down from 550 to 425°C

Substrate is allowed to cool down to room temperature in vacuum.

#### 3.2.4 Chemical Bath Deposition of CdS

A thin layer of CdS, about 300-500 Å, is deposited on the absorber by CBD. The CBD solution consists of 150ml of de-ionized water to which 27.5cc of 0.15M ammonium hydroxide is added followed by 22cc of 0.015M cadmium acetate. Cadmium acetate is the cadmium source. The sample is introduced into this solution and at 30°C 22cc of thiourea is added. This is the source for sulphur. The temperature of the solution is raised upto 80°C. The solution is constantly stirred using a magnetic stirrer.

### 3.2.5 ZnO Deposition

After CdS deposition the substrate is transferred into a RF sputtering system for the deposition of ZnO. The mask used for the deposition is designed so as to get 25 individual circular dots on the substrate. This helps to make devices with varying compositional ratios. The size of each dot is approx.  $0.1\text{cm}^2$ . The substrate is heated to  $125^\circ\text{C}$  using a temperature profile. Then the first layer of undoped ZnO is sputtered in an Argon and oxygen ambient where the Ar pressure is kept at 1mT and oxygen pressure is kept at 0.3mT. The typical thickness of undoped layer is  $400\text{ \AA}$ . Following this a doped layer of  $4500\text{ \AA}$  is deposited. Sputtering is done in an Argon ambient of 1.3mT. The target has alumina pieces kept on it to provide alumina doping. Resistivity of high  $10^{-4}$  ohm-cm is routinely obtained in our process.

The other device structure investigated over the course of this research is the device with a silicon nitride barrier layer, shown in figure 3.3

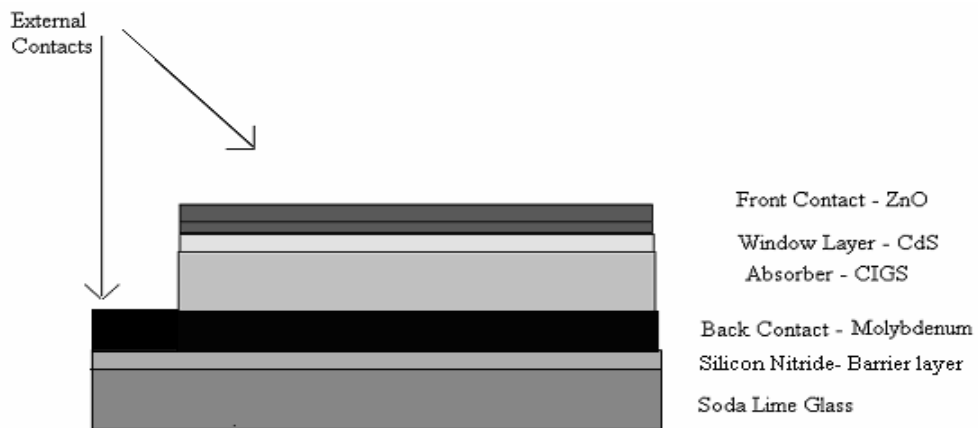


Figure 3.3 Device Structure With Silicon Nitride Barrier Layer

### 3.3 Silicon Nitride

Soda lime glass substrates were loaded into a RF sputtering system. The substrate was heated to 200C. The silicon nitride was sputtered at 2mT of Argon. Some of the important properties of silicon nitride are

Table 3.1 Properties of Silicon Nitride[26]

Density	3-3.3 g/cm <sup>3</sup>
Electrical Conductivity	Insulator
Breakdown Field	Typically a few 10 <sup>6</sup> V/cm
Thermal Conductivity	0.15 W/cm K
Thermal Diffusivity	0.07 cm <sup>2</sup> /sec
Coefficient of thermal expansion	3ppm/K
Dielectric constant	6-8

The processing details of all the other layers are the same. The absorber layers for these devices were deposited in two different systems. Though the basic process is the same in both these systems, the systems differ in terms of their geometry.

### 3.4 System-1

System-1 for convenience will be referred to as the old system. This chamber has a substrate holder designed for 2' x 2' molybdenum and has a lamp heating arrangement. There are 4 boats each for Cu, In, Ga and Se sources. There are separators between one boat and the others. This minimizes cross contamination. The boats are placed in such a

way that there is an intentional gradient of each material along the substrate. This helps in analyzing the influence of compositional gradients in all our experiments.

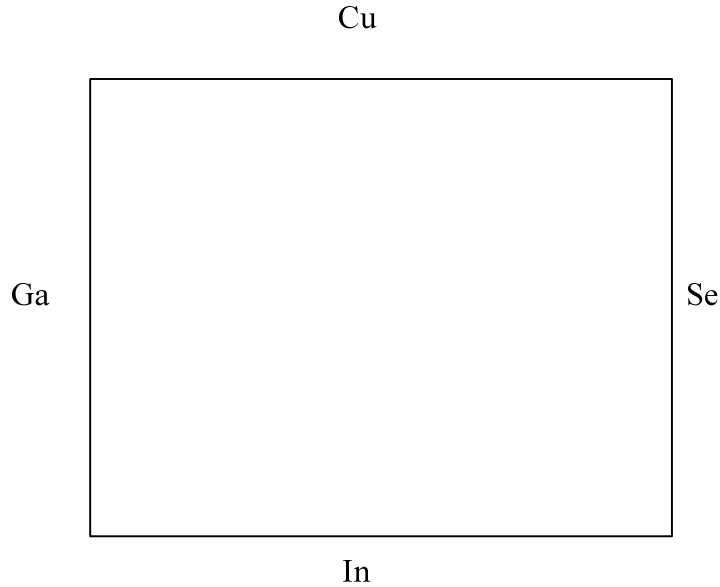


Figure 3.4 Orientation of Sources With Respect to the Substrate in the Old System

### 3.4 System – 2

System-2 for convenience will be referred to as the new system. This system has a loadlock and two chambers namely chamber-1 and chamber-2, all in line. The sample is loaded in to the loadlock and transferred into chamber-1 via gate valve1. This chamber has Cu and Ga evaporation guns. This ensures the elimination of the selenium back ground during the deposition of these metals. After this the substrate is transferred to chamber-2 via gate valve-2. This chamber has 3 evaporation guns for Cu, In and Se. Both these chambers have boron nitride heaters for heating the substrate. The temperature control is done using a thermocouple and a controller. The gradient of materials in this

system is slightly more complex as opposed to the old chamber. This is because Cu and In have the same direction of the gradient.

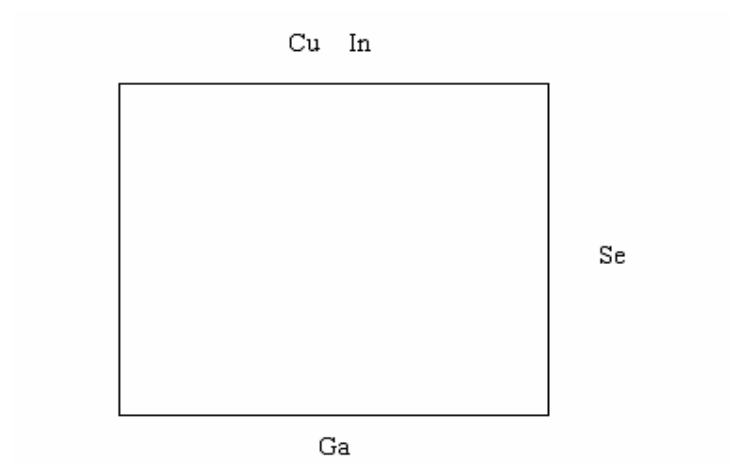


Figure 3.5 Orientation of Sources With Respect to the Substrate in the New System



## CHAPTER 4

### RESULTS AND DISCUSSION

The objective of this work was to understand the influence of back contact processing conditions on the performance of CIGS based solar cells fabricated by the processes described in previous chapter. The devices thus fabricated were analyzed using I-V and spectral response measurements. The open circuit voltage, fill factor and short circuit current density are the primary parameters used to study the influence of processing conditions on the device performance. These were used as guidance in the design of experiments. The device numbering in a substrate is shown below.

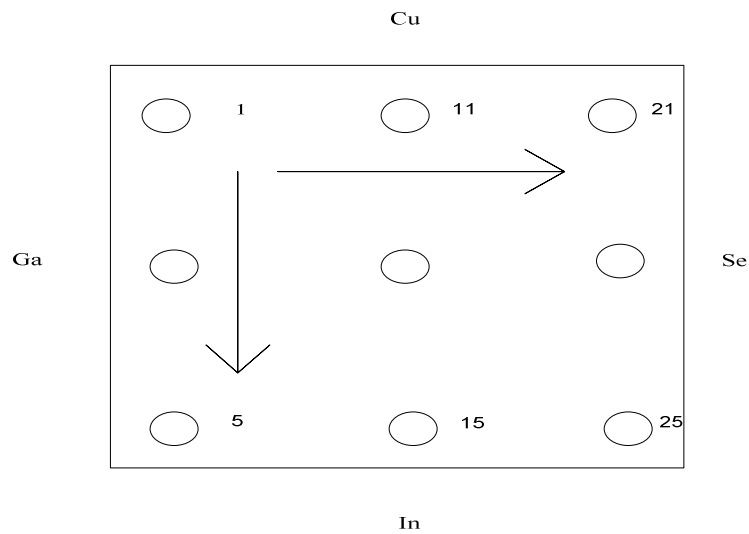


Figure 4.1 Device Numbering and Orientation of Sources with Respect to the Substrate

#### 4.1 Impact Of Substrate Cleaning on Device Performance

A clean substrate is one of the primary requisites to obtain high efficiency solar cells. The cleaning procedure followed in our laboratory has already been discussed in chapter 3. One of the important steps in this is the solvent clean, which is used to remove organic impurities and stains left from scientific soap. The standard solvent that was used for this purpose was trichloro-trifluoro-ethane. Since there was an environmental safety issue associated with this solvent, we had to replace it with a more environmental friendly solvent like methanol or Trichloroethane or 2-propanol.

400	400	400	390	390
380	390	400	390	370
390	380	390	390	360
390	390	340	360	370
340	320	370	370	340

Figure 4.2 Voc (mV) Distribution in Sample Cleaned with TrichloroEthane and TrichlorofluoroEthane

400	410	400	380	340
390	400	400	400	390
320	330	320	360	380
300	280	+	380	380
+	270	240	280	210

Figure 4.3 Voc (mV) Distribution in Sample Cleaned with Methanol and TrichloroEthane

400	390	380	340	390
+	390	400	440	430
280	+	400	+	380
290	410	130	400	370
190	330	400	430	400

Figure 4.4 Voc (mV) Distribution in Sample Cleaned with Methanol and TetrachloroEthylene

The figures 4.2, 4.3, 4.4 show the spread of Voc's on substrates cleaned using different cleaning agents. When molybdenum was deposited on these substrates, white spots were evident on the surface of the molybdenum. These spots came from the glass substrate to the molybdenum surface. These spots were present in the glass substrate even after cleaning indicating that the cleaning agents were not powerful enough to remove the stains from the glass substrates. When devices were fabricated on these substrates, the device performance within a substrate was non-uniform, which was evident from the Voc spread from the above figures. This can be referred to as spotty device performance. This could be because the growth of CIGS was affected in these spotty areas of molybdenum. The Jsc's in all the above cleaning methods were limited to 25mA/cm<sup>2</sup>. Then 2-propanol was tried as a cleaning agent and molybdenum films without any spots were obtained. The devices fabricated on these substrates had Voc's around 450mV, Jsc's around 35mA/cm<sup>2</sup> and FF around 60%. Thus we started using 2-propanol as our standard solvent for cleaning.

## 4.2 Metal Ratio and Top Cu Optimization

It can be seen from figure 4.5 that Voc's were limited to 400mV, the Jsc's were limited to 25mA/cm<sup>2</sup> respectively.

140 (25%)	260 (40%)	240 (37%)	60 (26%)	290 (45%)
300 (48%)	280 (46%)	210 (31%)	260 (48%)	320 (46%)
390 (48%)	330 (44%)	280 (41%)	290 (44%)	320 (38%)
370 (48%)	310 (38%)	300 (38%)	320 (44%)	370 (45%)
400 (50%)	400 (47%)	320 (38%)	400 (51%)	430 (58%)

Figure 4.5 Voc (mV) Distributions in Run V012

Voc spread in Run # V012, shown above, clearly shows that the best devices in this run were obtained in the Indium end i.e. the In-rich regime in the compositional gradient. This indicates that we were having a higher level of Cu in our film. Thus as the devices progressed from the In-side to Cu-side they became Cu-rich. The metal ratio at the Cu end was 1.04 and was 0.97 at the In end. When the metal ratio became greater than 1 due to the presence of excess Cu, it resulted in the formation of Cu<sub>x</sub>Se<sub>y</sub>. Cu<sub>x</sub>Se<sub>y</sub> being highly conductive tends to short circuit the junction. To get the metal ratio close to 1.0 at the Cu end it was decided to increase the Indium thickness by 200Å. Thus in Run # V015, the Indium thickness was increased by 200Å and all other conditions were the same as in Run V012.

100 (30%)	170 (31%)	360 (48%)	350 (42%)	370 (48%)
320 (40%)	360 (51%)	370 (58%)	370 (60%)	390 (53%)
330 (39%)	350 (44%)	370 (54%)	350 (53%)	330 (45%)
370 (55%)	370 (47%)	370 (48%)	370 (55%)	370 (54%)
340 (43%)	370 (56%)	370 (58%)	370 (59%)	370 (59%)

Figure 4.6 Voc (mV) and Fill Factor Distribution in Run V015

It can be seen that the fill factors have improved. These fill factor numbers are close to our standard values. This showed that our bulk metal ratio was good. So, we left the bulk metal ratio unchanged and decided to lower the top Cu thickness. In Run # V016 we lowered the top Cu thickness from 60Å to 30Å.

390	370	350	350	320
370	360	360	350	340
420	380	370	380	390
410	390	400	400	390
420	420	420	360	400

Figure 4.7 Voc (mV) Distribution in Run V016

The Voc spread from Run # V016 still indicated that we had to lower the top Cu thickness. Thus we reduced the top Cu to 20Å.

420 (60%)	460 (61%)	450 (56%)	440 (56%)	430 (55%)
430 (57%)	420 (52%)	440 (56%)	430 (60%)	430 (60%)
440 (58%)	450 (56%)	440 (54%)	410 (51%)	430 (54%)
420 (56%)	430 (54%)	420 (53%)	420 (56%)	410 (57%)
270 (33%)	410 (51%)	250 (32%)	420 (53%)	420 (54%)

Figure 4.8 Voc (mV) and FF Distribution in Run V020

The Voc spread from Run V020 in figure 4.8 shows good device performance. The 2 bad devices could be due to molybdenum being spotty.

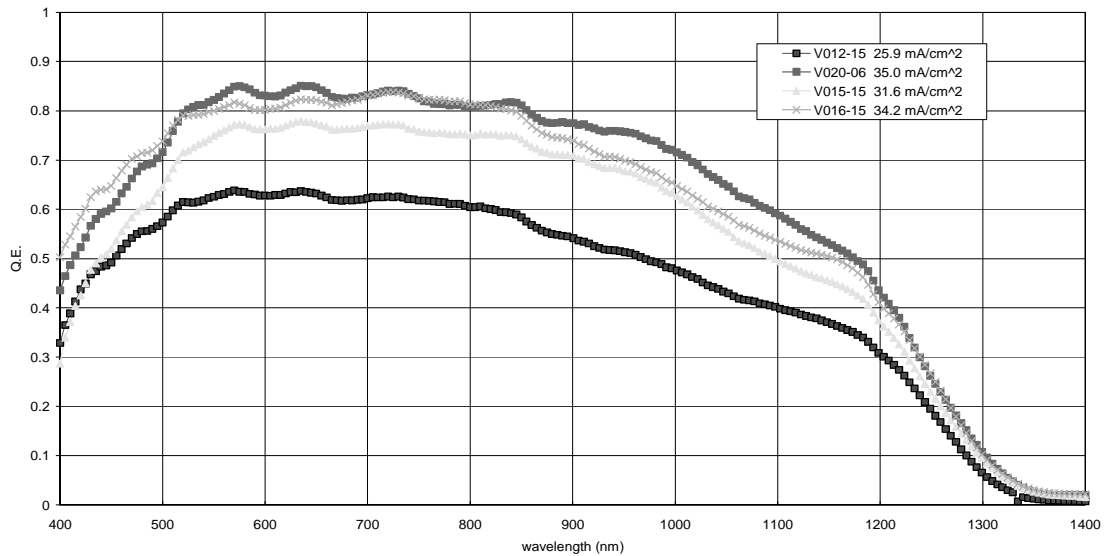
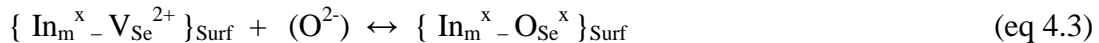
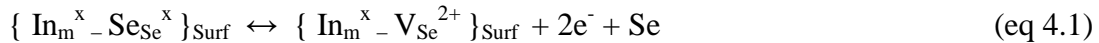


Figure 4.9 Spectral Response Comparison of Devices From Runs V012, 15, 16, 20 with Top Cu of 60Å, 20Å, 60Å, 30Å Respectively

The spectral response in figure 4.9 showed that the bulk metal ratio is the primary controlling factor of currents. It can also be seen that with variation in top Cu the spectral response shows improvement till the 900nm wavelength range, which corresponds to the first few thousand Angstroms in the absorber layer. Indicating that the effect of top Cu is on the surface of the absorber layer[30].

### 4.3 Substrate Effects – Role of Sodium

At elevated temperatures of processing sodium tends to diffuse out of soda lime glass and migrates through the film and is known to exist in interfaces and grain boundaries[27]. It is also known to form  $\text{Na}_{\text{Cu}}$  antisite defect[13]. Na and Cu are Group-1 elements therefore substitution of one by the other gives rise to neutral defects. Na is also thought to be a catalyst in the oxidation of selenium vacancies. Selenium vacancies ( $\text{V}_{\text{Se}}$ ) can form at surface indium sites this is shown in eq 4.1. These are donor defects. Oxygen at the surface in presence of sodium gains 2 electrons from the lattice producing  $\text{O}^{2-}$  which fills the selenium vacancy on the indium surface thus passivating the donor defects. This is shown in eq 4.2 and 4.3. In these equations M denotes a metal site (which can be In or Cu) and x denotes a neutral charge



To reduce the effect of sodium in our devices we deposited a silicon nitride barrier layer on the SLG and fabricated devices in both the old and new system. The device fabrication is described in chapter-3.

#### 4.3.1 Old System

Samples were fabricated in this system with nitride thickness varying from 20-150 Å.

Si <sub>3</sub> N <sub>4</sub> Thickness ( Å )	Voc(mV)	Isc (mA)	FF (%)
20	400	5.4	53%
50	260	3.0	27%
150	90	2.5	30%

Figure 4.10 Variation of Device Performance as a Function of Nitride Thickness in Old System

#### 4.3.2 New System

Samples were fabricated with silicon nitride thickness varying from 200Å<sup>o</sup> – 1600Å<sup>o</sup>.

Si <sub>3</sub> N <sub>4</sub> Thickness ( Å )	Voc(mV)	Isc (mA)
200	350	6.0
800	300	2.5
1600	290	0.3

Figure 4.11 Variation of Device Performance as a Function of Nitride Thickness in New System



### 4.3.3 Old System vs New System

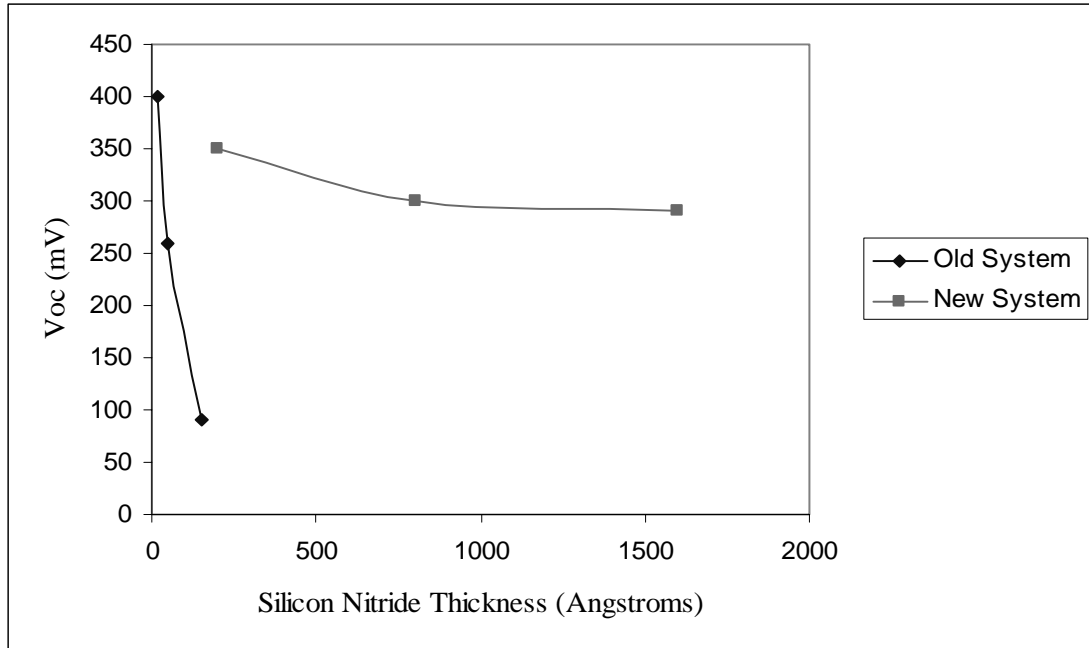


Figure 4.12 Variation of Voltage as a Function of Silicon Nitride Thickness in Old and New System

It is evident from figure 4.12 that the drop in device performance, as a function of silicon nitride thickness, was more rapid in the old system as opposed to the new system. This can be speculated upon as follows. The primary difference between the two systems is that in the new system we have the ability to deposit Cu in a selenium-free environment; Whereas in the old system there is a continuous selenium background during copper deposition. The back-ground selenium was due to a large amount of accumulated selenium in the system and the contamination of the copper source with selenium during depositions. This resulted in the formation of copper selenide. It was felt that that the device performance in the old system was limited by the formation of copper

selenide. In the new system Cu and Ga were deposited in chamber 1, which does not contain selenium. The substrate is then moved to chamber 2 for the  $\text{In}_2\text{Se}_3$  and selenization steps. It is thought that the  $\text{Cu}_x\text{Se}_y$  formed in the old system is not only a problem by itself but also resulted in the formation of high levels of copper vacancies. This resulted in Cu-poor CIGS films. Oxidation is more prevalent in this environment, and our process has been tuned accordingly to get the best  $V_{oc}$ 's and device performance. The presence of silicon nitride reduced the amount of sodium reaching the CIGS layer as a function of silicon nitride thickness. This lack of sodium resulted in lower oxidation and a high level of  $\text{In}_{\text{Cu}}$  anti-site defects, thus resulted in lower  $V_{oc}$ . In the new system oxidation is less prevalent and the process has been tuned accordingly to obtain the best device performance. Thus as the sodium level is reduced the accompanying reduction in oxidation is less important and thus there is less of an effect on  $V_{oc}$ . The 200Å data point from the new system was interesting. For this device Cu was deposited in chamber 2 of the new system. Chamber 2 has a selenium environment. Though we expect to form some  $\text{Cu}_x\text{Se}_y$  during Cu deposition, this would be less than that of the old system. Thus the impact on the  $V_{oc}$  should be in between the old and new system. This can be seen in the graph above.

#### 4.3.4 Stability of Devices with 20Å Nitride Barrier Layer

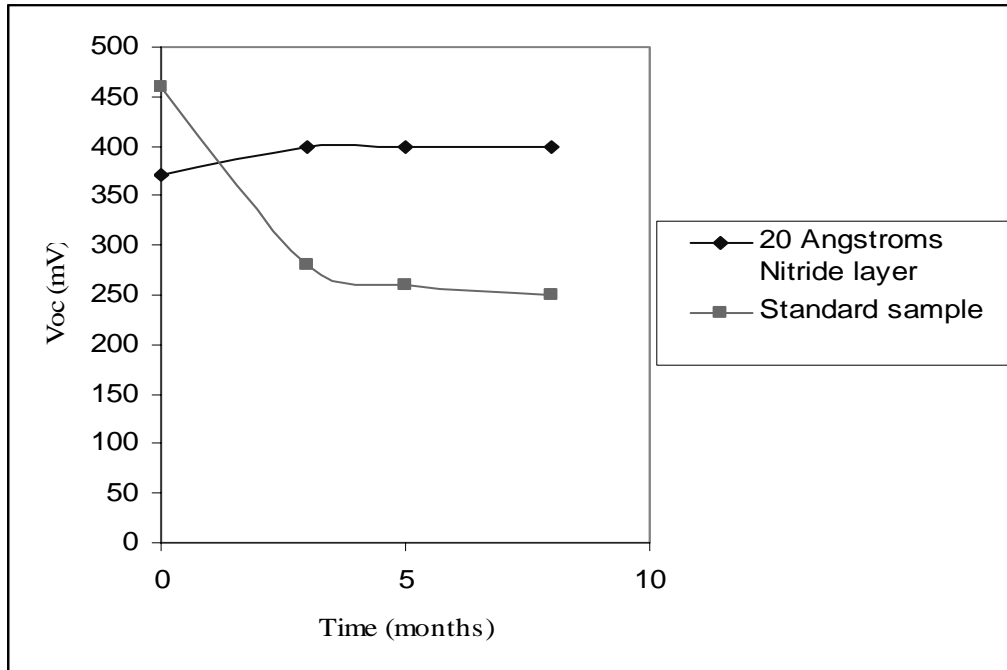


Figure 4.13 Voc Variations of Standard Sample and 20 Å Nitride Sample Vs Time

Although, the performance of devices with a 20Å silicon nitride barrier layer was lower than the standard device (without the barrier layer), the performance improved as time passed (8 months) as seen in figure 4.13. This result reinforces the discussion above. In the absence of a barrier layer the process was tuned to get good initial performance. However as the device was kept in the lab in the presence of air and moisture, they oxidized and degraded. Devices with 20Å silicon nitride barrier layer started with lower initial performance because of under oxidation since the oxidation could continue when the device was kept in the lab, though at a slower pace because of reduced Na environment, the performance seemed to improve and the device was more stable.

### 4.3.5 Run #V029, V046

350	370	350	370	370
240	360	350	310	430
290	320	220	350	240
160	270	220	230	240
150	180	200	210	250

Figure 4.14 Voc (mV) Variation in Run# V046 (50A Silicon Nitride Layer)

330	400	390	340	360
300	380	360	390	380
220	370	310	370	380
380	310	370	340	350
370	350	350	370	340

Figure 4.15 Voc (mV) Variation in Run# V029 (20A Silicon Nitride Layer)

It can be observed from figures 4.14 and 4.15 that as the devices went from Cu end to In end, there seems to be a drop in device performance. It is more pronounced in the 50 Å (V046) silicon nitride blocking layer. This can be speculated as follows: As we move from the Cu end to In end there is a gradient in Cu thickness and In thickness (i.e.) at the Cu end we have more Cu and less In and at the In end we have more In and less of Cu. This corresponds to a higher level of  $V_{cu}$  in the indium end as opposed to Cu end. In

our standard process the level of Cu is tuned to the environment of sodium coming from substrate. In the presence of a barrier layer the Group-1 (Cu + Na) level is lowered. In the indium end, as already mentioned, there is a higher level of  $V_{cu}$ . In the presence of Na they get into these sites and form  $Na_{cu}InSe_2$ . In the absence of Na, Indium tends to get into these sites and forms  $In_{cu}$  antisite defects. These are donor defects. Thus as we progress from Cu end to In end we have higher level of  $In_{cu}$  antisite defect. This leads to a drop of  $V_{oc}$  from Cu to In end.

#### 4.3.6 Increase in Cu Level

The Cu level was increased in order to analyze the possible compensation for lack of sodium. The edge to edge difference in Cu thickness was  $100\text{\AA}$ . Thus we decided to increase the Cu thickness on the substrate by  $100\text{\AA}$ .

380	390	380	280	380
380	390	370	350	360
400	390	330	380	380
380	370	370	370	370
370	370	360	360	340

Figure 4.16  $V_{oc}$  (mV) Spread After Increasing Cu Level

The  $V_{oc}$  spread in figure 4.16 showed no specific trends, suggesting that sufficient Cu was supplied to compensate for the sodium thereby suppressing the formation of  $In_{cu}$  antisite defects. The best device had a  $V_{oc}$  of 400mV and  $J_{sc}$  of  $34.5\text{mA}/\text{cm}^2$ . Fig 4.17 shows the spectral response of device V042-11, which had the maximum  $J_{sc}$  of

35.2mA/cm<sup>2</sup> . The Jsc value is close to the Jsc from our standard devices but the Voc is very low in comparison to the values from our standard devices. This shows that even though Cu can substitute for Na , we need sodium for good device performance.

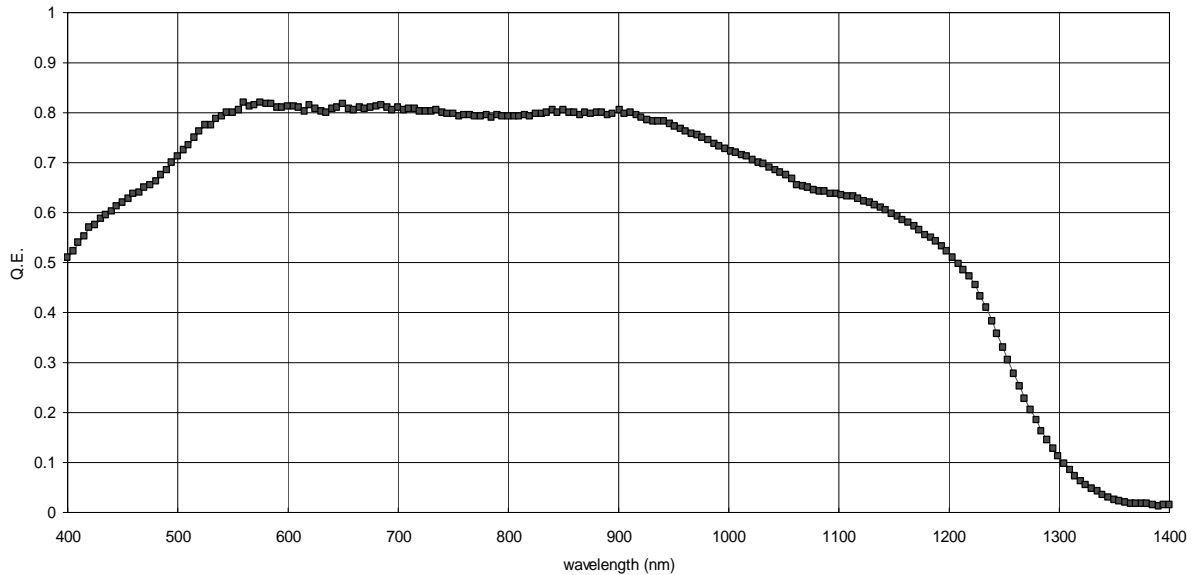


Figure 4.17 Spectral Response of Device V042-11

From the SEM images in Figure's 4.18 and 4.19 it can be seen that the absorber layer grown on substrates with a barrier layer has a rougher surface as opposed to our standard CIGS film. This could result in a non uniform coverage of CdS thus resulting in a bad junction and lower Voc's.

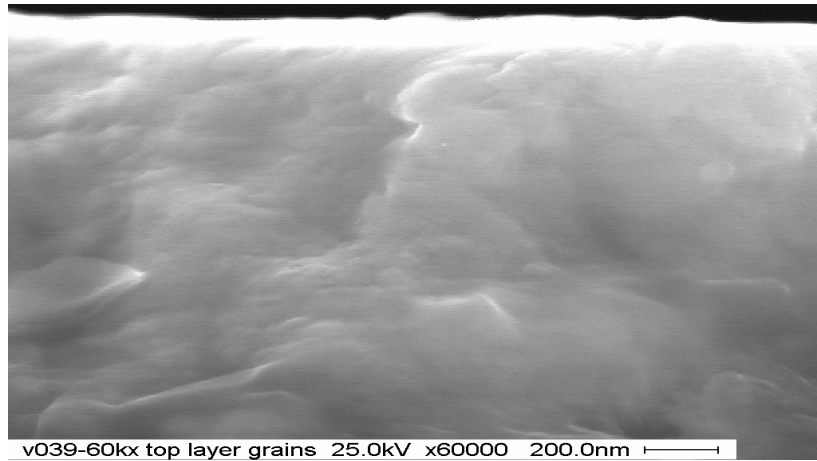


Figure 4.18 SEM Image of Standard CIGS

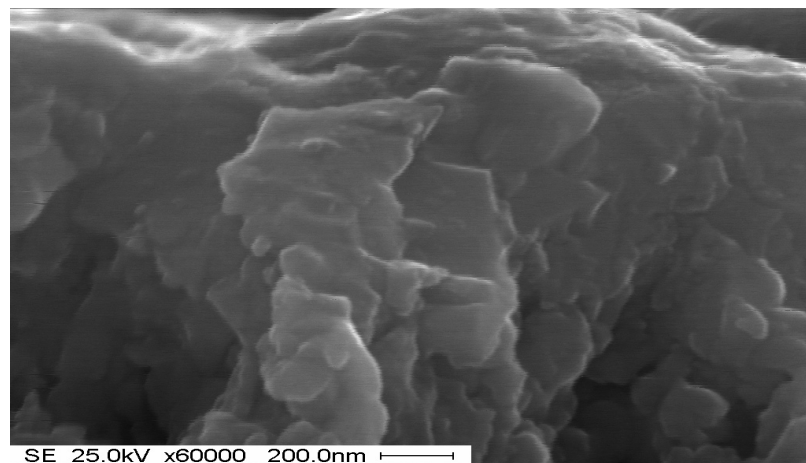


Figure 4.19 SEM Image of CIGS with a 50A Barrier Layer

From the above we concluded that blocking off any amount of sodium using a barrier layer hurts our device performance. So we decided to optimize the molybdenum back contact, through which sodium migrates to the absorber at elevated temperatures of processing and in turn fine tune our device performance.

#### 4.4 Resistivity vs Rate

It has been reported that in a bi-layer sputtered molybdenum film the first layer which is sputtered at high pressure is less dense and hence has a higher resistivity. The

second layer which is sputtered at lower pressure is denser and hence has a lower resistivity[22]. It can be observed from figure 4.20 that the resistivity of molybdenum films which are used in our studies is dependent on the rate of deposition.

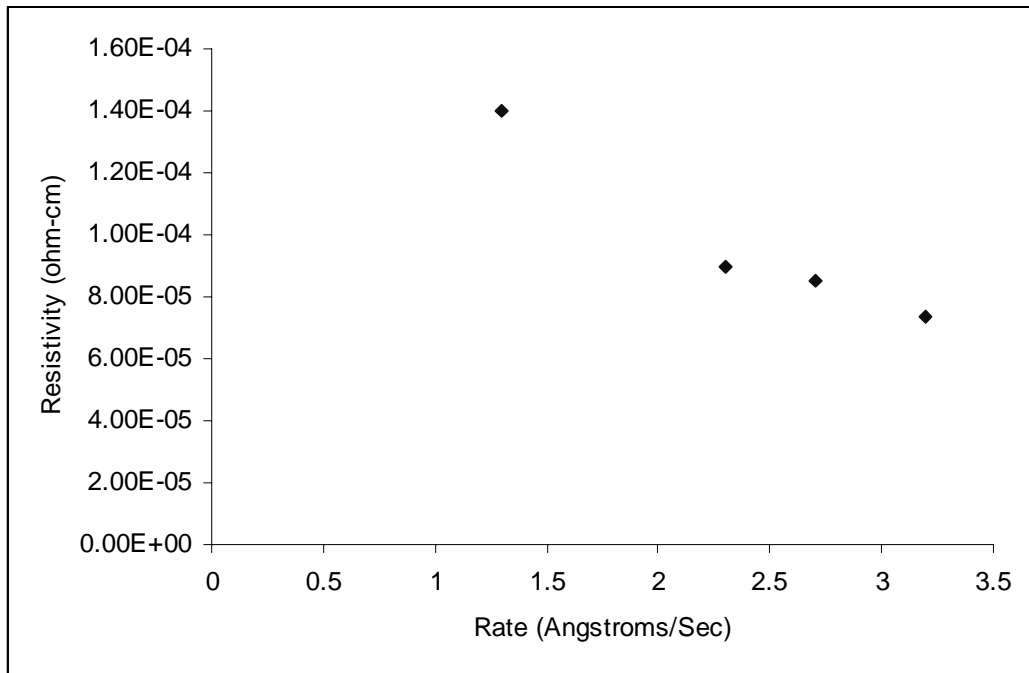


Figure 4.20 Variation of Resistivity with Rate of Sputtering of Molybdenum

To obtain higher rate of deposition the sputtering power has to be increased. Increasing power leads to an increase in density, and a decrease in resistivity.

#### 4.5 Device Performance vs Rate

In figure 4.21 the filled data points for Voc and Jsc are from devices with molybdenum sputtered from a new target and the non-filled Voc and Jsc data points are from devices with molybdenum sputtered from an old target. It can be seen from figure



4.21 that to obtain a  $J_{sc}$  value of approx  $35\text{mA}/\text{cm}^2$  the sputtering rate of molybdenum has to be kept above  $2.7\text{\AA}/\text{s}$ . This is true for the data points from both the old and new targets. From the discussion in section 4.4, it can be inferred that the density of molybdenum was directly related to the sputtering rate. From a sodium perspective, lower density would translate into higher sodium migrating into the CIGS absorber layer. As the sputtering rate increases the density increases. Thus the channel for sodium migration is more constrained. This would translate into lesser sodium migrating to the film. When excess sodium is present in films they tend to form deep states [29] and can start trapping carriers. This is a possible reason for lower  $J_{sc}$  values at lower sputtering rate.

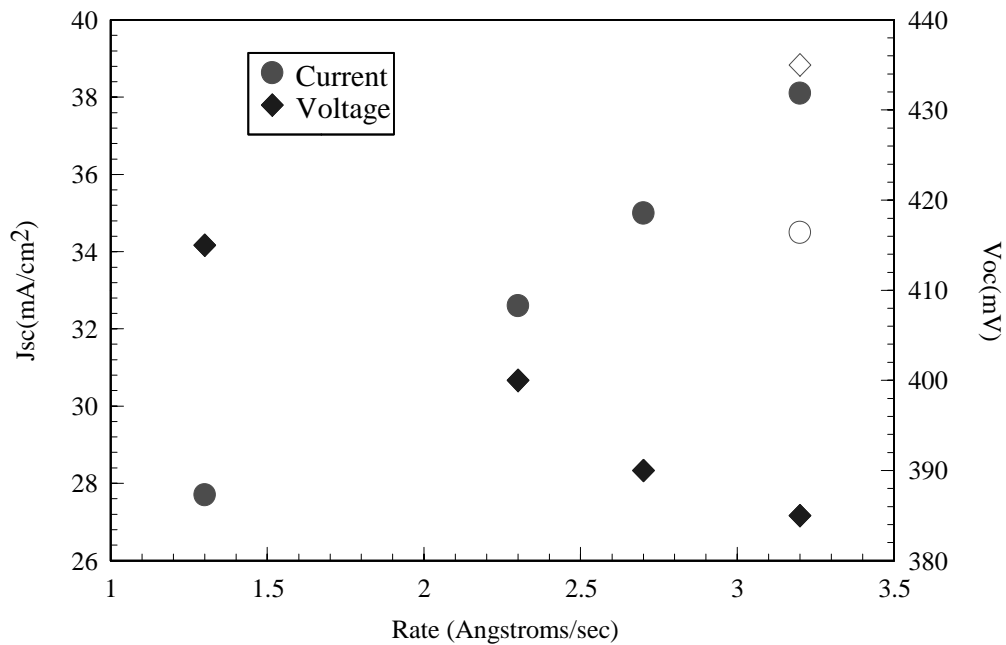


Figure 4.21 Variation of Device Performance as a Function of Rate of Sputtering of Molybdenum

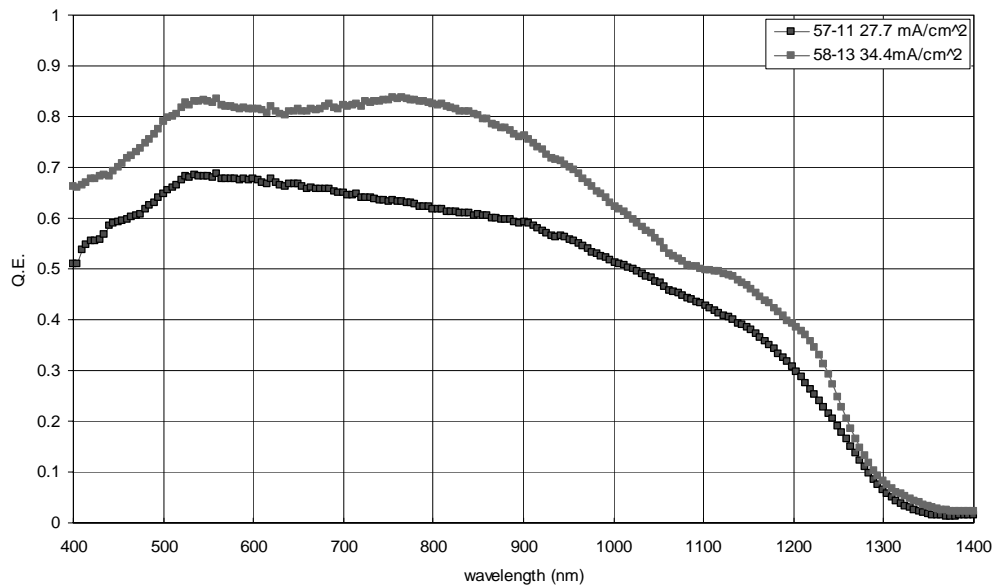


Figure 4.22 Comparison of Spectral Response of Samples From Runs V057, 58

Figure 4.22 shows the SR of the two devices with molybdenum sputtered at  $1.3\text{\AA}/\text{s}$  (Run V057) and  $3.2\text{\AA}/\text{s}$  (run V058). It can be seen from the SR that the response of device V057 was uniformly shifted down and has a bigger slope hinting that there might be a collection problem in this case. Thus the sputtering rate has to be kept above  $2.7\text{\AA}/\text{s}$  to get good  $J_{sc}$ .

The impact of molybdenum sputtering rate on  $V_{oc}$  was not very clear. This is because even though the average  $V_{oc}$  of devices seems to drop with increasing sputtering rate but the average  $V_{oc}$  of device with molybdenum sputtered at  $3.2\text{\AA}/\text{s}$  from the old target has the best performance. This suggests that the drop in  $V_{oc}$  with the new target was due to high discharge voltage, which is dealt in the next section.

#### 4.6 Effect of Discharge Voltage on Voc

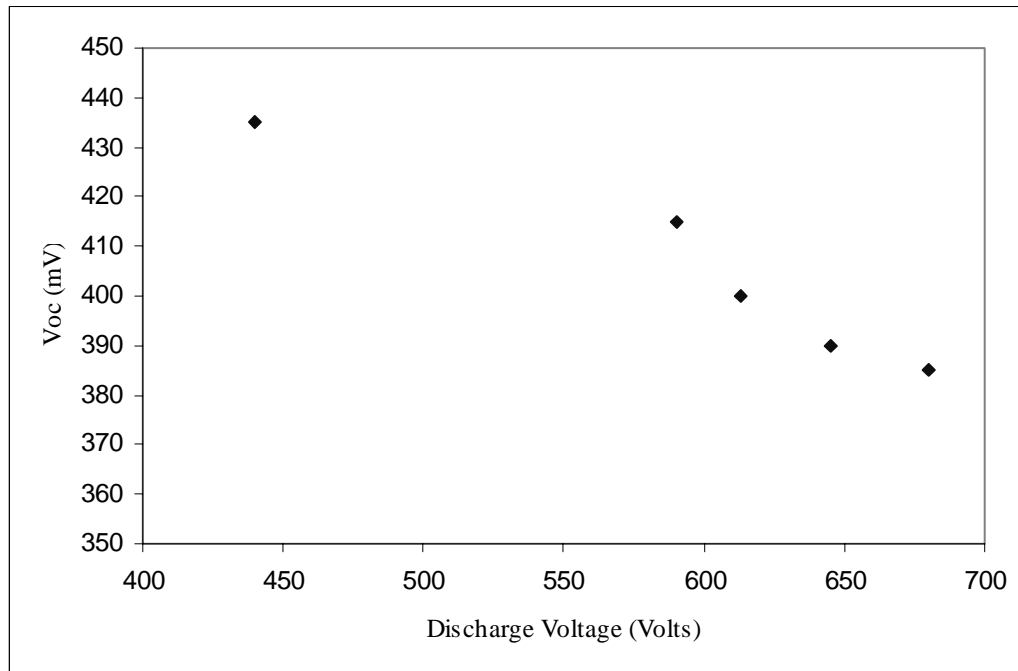


Figure 4.23 Variation of Open Circuit Voltage with Discharge Voltage of Molybdenum Sputtering

It can be seen from figure 4.23 that as the discharge voltage of molybdenum sputtering is increased the Voc of devices keeps decreasing. The devices fabricated on molybdenum sputtered at 680V had a tendency to pop out from the molybdenum surface suggesting that the devices were in high level of stress. The drop in device performance could be because of the high level of stress developed with increase in discharge voltage. To obtain good device performance the discharge voltage has to be kept below 600V.

#### 4.7 Effect of Molybdenum Thickness on Device Performance

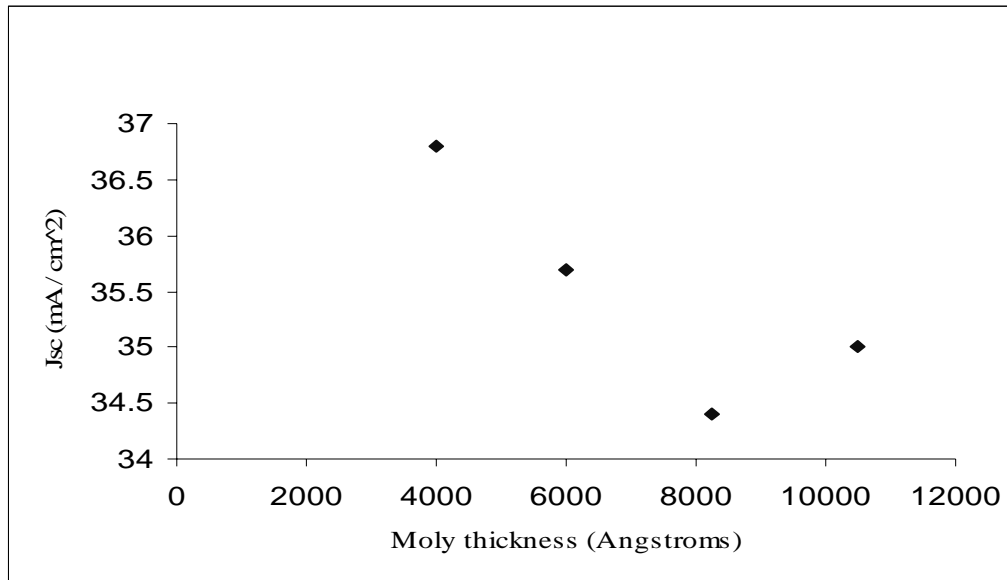


Figure 4.24 Variation of Maximum Jsc with Variation on Molybdenum Thickness

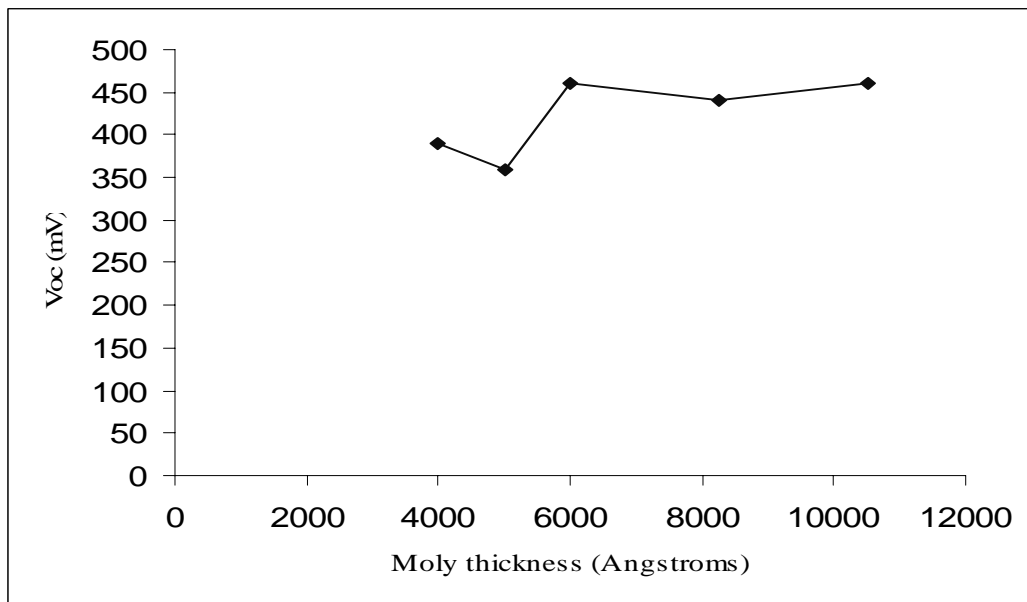


Figure 4.25 Variation of Maximum Open Circuit Voltage with Variation in Molybdenum Thickness

The Molybdenum thickness was decreased with an intention to let more sodium migrate to the CIGS film. The molybdenum thickness was reduced from 10,500Å to 5000Å by reducing the thickness of the second layer. The first layer thickness was kept at 3000Å. It can be observed from figure 4.25 that the maximum Voc value was constant with varying thickness till 6000Å.

420	450	440	430	390
450	460	450	450	430
450	430	420	440	420
450	440	390	400	420
410	440	420	430	270

Figure 4.26 Voc (mV) Spread on Substrate with Molybdenum Thickness 6000Å

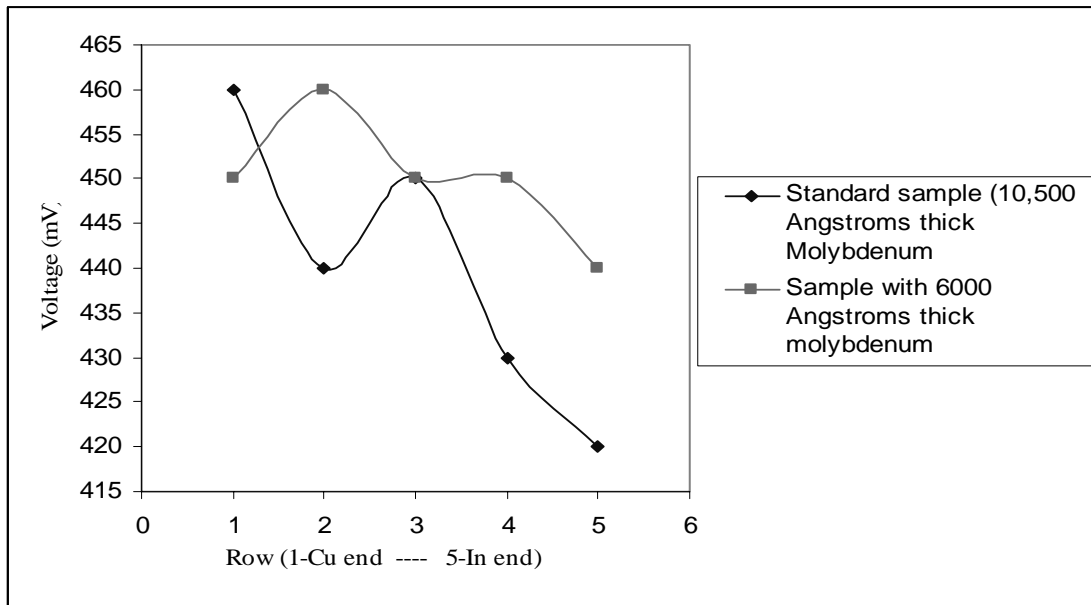


Figure 4.27 Metal Ratio Sensitivity (Variation of Maximum Voc within the Substrate Between a Standard Sample and a Sample With 6000Å<sup>0</sup> Thick Molybdenum Layer)

Although the maximum value of  $V_{oc}$  is approximately the same at all thickness from 6000Å to 10,500Å, it can be seen from figure 4.26 that  $V_{oc}$  spread across the substrate is more uniform in the case of a 6000Å thick molybdenum layer, i.e. the devices were less sensitive to variation of metal ratio. This is shown clearly in figure 4.27 by comparing the variation of  $V_{oc}$  while progressing from the Cu end to the In end in a standard sample within the sample with that in the 6000Å thick molybdenum layer. The reduced sensitivity to variation in metal ratio is probably because of more sodium migrating into the film, thus increasing the Group-1 / Group- 3 ratio uniformly across the substrate without getting Cu-rich. When the thickness was reduced to 5000Å, it can be observed that there was a drop in  $V_{oc}$ , so it was decided to keep the second layer thickness at 3000Å. The molybdenum thickness was reduced to 4000Å by reducing the first layer thickness to 1000Å and maintaining the second layer at 3000Å. Though the performance of the devices was better than the devices with 5000Å molybdenum, still they were lower than that of 6000Å molybdenum. Generally, after the deposition of the absorber layer the film looks bluish in color hinting that the surface of the film is smooth. CIGS films deposited on 4000Å and 5000Å thick molybdenum appeared grayish in color meaning that the films were rougher. When CdS was deposited on these substrates it could have resulted in a non-uniform coverage of CdS, leading to a bad junction. This can also be ascertained by the I-V curve in Figure 4.28 which shows the sample with a 4000Å thick molybdenum layer showing shunting. This could have resulted in loss of  $V_{oc}$  or it could be because of some defects in the absorber. It can be observed from figure 4.24 that the maximum  $J_{sc}$  is obtained from the device with 4000Å thick molybdenum layer. This is probably because the rougher surface helped get rid of some of the reflection losses. The

best overall device performance was obtained at 6000Å of molybdenum thickness. The best device had a Voc of 460mV, Jsc of 35.7mA/cm<sup>2</sup> and a Fill Factor of 62%, Figure 4.29 shows the I-V curve of this device.

In order to measure the sodium content in the absorber layer we did EDS measurements on our samples. The data obtained from this measurement was inconclusive because we realized that the sodium detected from this measurement was predominantly from the SLG substrate. The sodium content in the film can be measured accurately by doing SIMS measurements but we couldn't do this measurement because of the unavailability of the equipment.

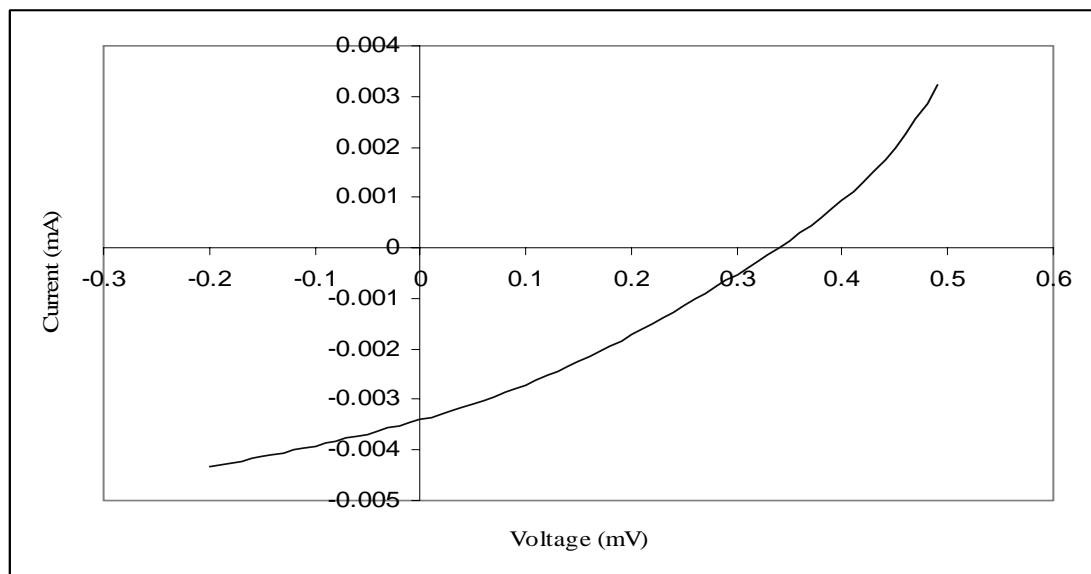


Figure 4.28 I-V of Device with 4000Å<sup>o</sup> Thick Molybdenum Layer

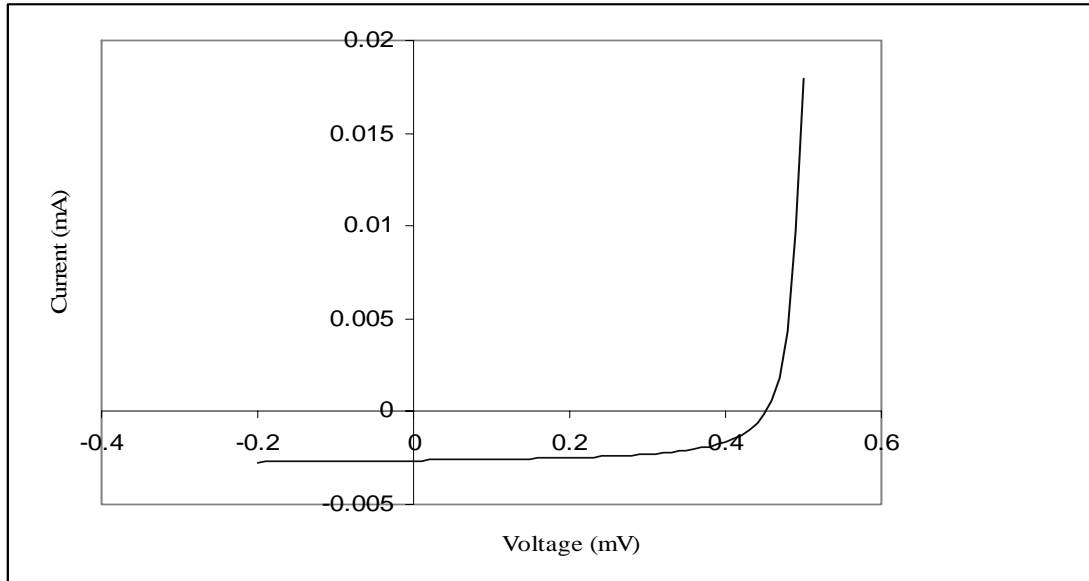


Figure 4.29 I-V of Device With 6000Å<sup>o</sup> Thick Molybdenum Layer

#### 4.8 Type IV (Split Ga – Split In) Process

The best results obtained in our laboratory for our 2-stage process is a device with an efficiency of 13.0%[30]. During this time the gallium was deposited by sputtering, which was eventually replaced with an evaporation set up. The process kinetics with gallium sputtering helped the incorporation of a little bit of gallium in the space charge region which helped to open up the bandgap to around 1.0eV. This in turn helped to get Voc's as high as 495mV. When we switched to gallium evaporation, the process kinetics did not help in the incorporation of gallium in the space charge region, hence the Voc's were limited to 460mV. The base process was changed so as to try and incorporate gallium in the space charge region. This process was called the Type IV (split In – split Ga) process.



In this process the gallium was split into 3 parts. The idea behind this was that the first part (Back Gallium) would help in adhesion to the back contact, the second part (middle Gallium) which was deposited by splitting the  $\text{In}_2\text{Se}_3$  would help in obtaining a normal gallium profile from the back contact to the front contact and the third part (top Gallium) would help in opening the bandgap. The complete processing details for this process are given in chapter 3.

#### 4.8.1 Run # V067, V070 ( x \150 Å \50 Å )

In Run # V067, gallium was split into 600Å of back gallium, 150Å of middle gallium and 50Å of top gallium. The Voc spread of devices from the run is shown in Figure 4.30.

460	460	410	430	400
480	460	460	450	390
450	470	470	450	450
470	480	480	480	470
460	470	470	470	440

Figure 4.30 Voc (mV) Spread From Run # V067

It can be seen that the device performance is very uniform throughout the substrate with the best devices having Voc's of 480mV. The Jsc obtained in this run was 32.3mA/cm<sup>2</sup>. Figure 4.31 shows the comparison of the spectral responses between a device fabricated using the Type I process and the device from this run.

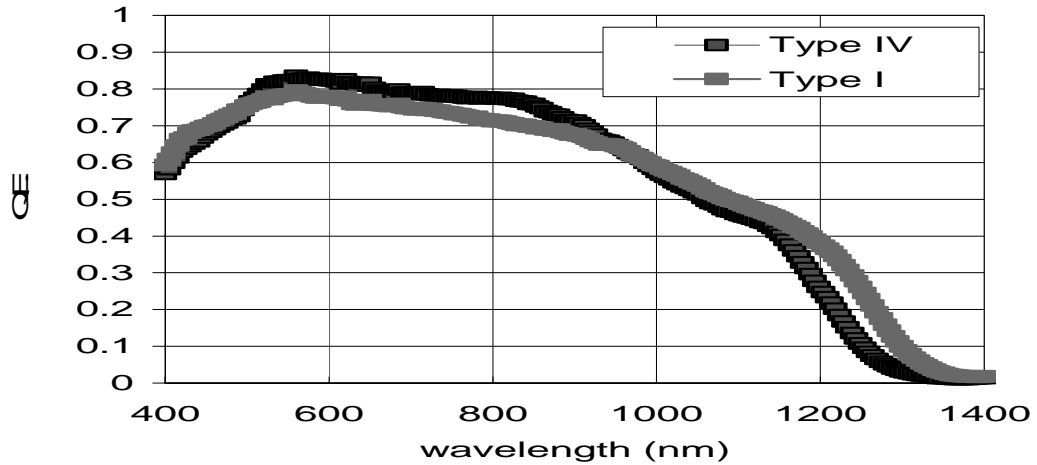


Figure 4.31 Spectral Response Comparing Type I vs Type IV

It can be concluded from figure 4.31 that the Type IV process incorporates gallium into the space charge region which has resulted in an approximate 40meV increase in the bandgap when compared with the Type I process. This bandgap shift helped in obtaining Voc values greater than 460mV.

To analyze the effect of back gallium the thickness of back gallium was lowered to 500Å<sup>o</sup>, leaving all other parameters same as that of Run V067.

480	430	460	290	400
480	470	490	490	460
490	490	490	470	480
490	490	480	490	490
430	450	430	430	410

Figure 4.32 Voc (mV) Spread From Run # V070

It can be observed in figure 4.32 that the best devices had Voc's of 490mV, which was the highest value of Voc obtained over the course of this research. However, the Jsc was limited to 30.6mA/cm<sup>2</sup>. By varying the back gallium thickness there was no significant improvement in device performance, so it was decided to analyze the effect of the middle gallium on device performance.

#### 4.8.2 Effect of Middle Gallium

The effect of middle Gallium was analyzed by varying the thickness of middle gallium and by keeping the back and top gallium thicknesses constant.

Table 4.1 Effect of Variation of Middle Gallium (Back Gallium 600 Å \ \ Top Gallium 50Å)

Run #	Middle Ga Thickness(A <sup>o</sup> )	Voc (mV)	Jsc (mA/cm <sup>2</sup> )	FF
V067	150	480	32.3	64%
V069	250	430	32.2	61%
V074	100	460	30.8	54%

Table 4.2 Effect of Variation of Middle Gallium (Back Gallium-500Å \ \ Top Gallium-50Å)

Run #	Middle Ga Thickness(A <sup>o</sup> )	Voc (mV)	Jsc (mA/cm <sup>2</sup> )	FF
V070	150	490	32.3	62%
V068	250	410	37.4	59%

The middle gallium has a significant impact on both the  $J_{sc}$  and  $V_{oc}$ . It can be seen from Tables 4.1 and 4.2 that the best  $V_{oc}$  values are obtained with a middle gallium of  $150\text{\AA}$ . When we raise the gallium level to  $250\text{\AA}$ , in the case of devices with  $600\text{\AA}$  of back gallium there is an overall drop in device performance, however the devices with  $500\text{\AA}$  of back gallium had a  $J_{sc}$  of  $37.4\text{mA}/\text{cm}^2$ . This is the highest value of  $J_{sc}$  obtained for this process. The  $V_{oc}$  of devices with  $250\text{\AA}$  of middle gallium was lower than that of devices with  $150\text{\AA}$  of middle gallium, irrespective of the thickness of the back gallium

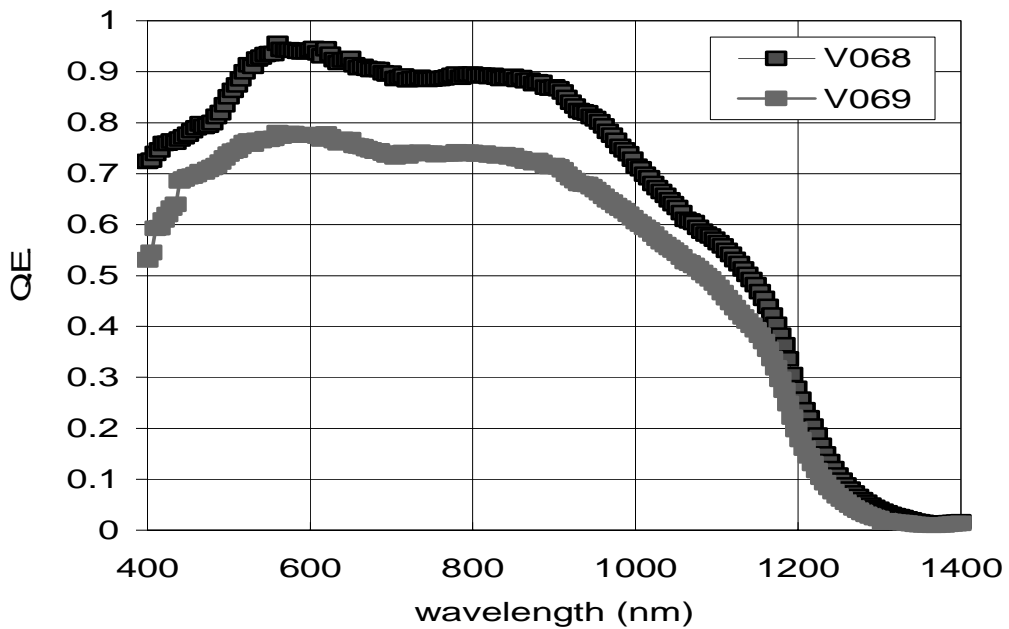


Figure 4.33 Comparison of SR Between V068 and V069

Figure 4.33 shows the comparison of devices with varying back gallium thickness ( $500\text{\AA}$  - V068,  $600\text{\AA}$  -V069). The middle and top gallium thickness were  $250\text{\AA}$  and

50Å respectively in both the devices. It can be seen that the devices with 500Å of back gallium has a slightly lower band gap as opposed to devices with 600Å of back gallium. This suggests that the back gallium level would determine the amount of gallium that would remain in the front of the device, i.e. the less the gallium at the back of the device the more the migration from the front of the device. The slightly higher bandgap in the case of device with 600Å of back gallium could be the reason for the higher Voc in this device when compared with the device with 500Å of back gallium. The higher Jsc in devices with 500Å of back gallium could be because of a favorable band gap profiling caused by the migration of some of the gallium to the back.

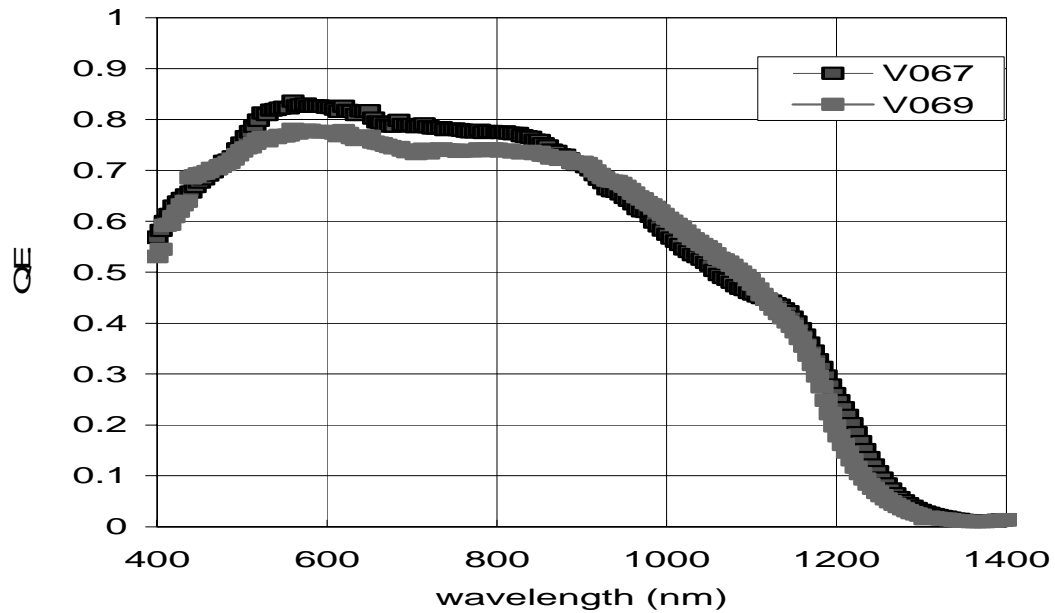


Figure 4.34 Comparison of SR Between V067 And V069

Figure 4.34 shows the comparison of devices with varying middle gallium thickness (150Å - V067, 250Å -V069). The back and top gallium thickness were 600Å

and 50Å respectively in both the devices. It can be observed that even though the total gallium level in the front of the device was increased, it didn't translate into a significant bandgap shift. This suggested that some of the gallium that was deposited stayed as free gallium thus resulting in point defects, which affected the device performance

The devices with 150 Å of middle gallium had the best Voc's, while the devices with 250 Å of middle gallium had the best Jsc's. There may be two possible explanations for this behavior:

1 Gallium vacancies may have been created in the absorber with 150Å<sup>o</sup> of middle gallium. However, 250 Å of middle gallium may result in excess gallium in the absorber. This shift from gallium vacancies to excess gallium can be used to explain this difference in the device performance.

2 With 150Å<sup>o</sup> of middle gallium there may be point defects in the bulk of the material, which results in lower Jsc. However, with 250 Å of middle gallium the point defects may be predominantly on the surface thereby, affecting the Voc's.

### 4.8.3 Effect of Top Gallium

Table 4.3 Effect of Variation of Top Gallium (Back Gallium-500 Å \ Middle Gallium-250Å \ )

Run #	Top Gallium Thickness(A <sup>o</sup> )	Voc (mV)	Jsc (mA/cm <sup>2</sup> )	FF
V068	50	410	37.4	59%
V072	25	440	27.8	53%

It can be seen from Table 4.3 that the devices were sensitive to the variation of top gallium. The devices with lower top gallium probably had lower point defects on the surface which resulted in higher Voc's but the lower Jsc's may be due to an unfavorable bandgap profiling which might have led to collection problems.

The best device from this process had a Voc of 480mV, Jsc of 32.3mA/cm<sup>2</sup>. Some of the devices had Voc's as high as 490mV, Jsc's as high as 37.4mA/cm<sup>2</sup> and FF's as high as 64%.

## CHAPTER 5

### CONCLUSIONS AND RECOMMENDATIONS

The accomplishments of this research were

- 1 Analyzed the influence of silicon nitride barrier layer on Type-I CIGS solar cells.  
The absorber layers for this research work were fabricated from both the old and new CIGS deposition system.
- 2 Analyzed the influence of molybdenum processing conditions on Type-I CIGS solar cells.
- 3 Developed a Type- IV CIGS deposition process.

Silicon Nitride was sputtered on to SLG and devices were fabricated on these substrates. The absorber layer was deposited, by the Type-I process, on both the old and new system. The results showed that the devices fabricated in the old system were more sensitive to the presence of the barrier layer. The Voc's dropped from 400mv to 90mv as the silicon nitride thickness increased from 20Å to 150Å. The devices fabricated in the new system with silicon nitride thickness varying from 200Å to 1600Å had a corresponding Voc variation of 350mV to 290mV. This difference in behavior was because the Cu deposited in the new system had no selenium background. Whereas, in the old system we had a continuous unintentional selenium background, which resulted in



the formation of copper selenide. Thus the CIGS films deposited in the old system were copper poor when compared to the films from the new system. The impact of Na is more on Cu-poor films. The Voc distribution in samples with 20Å and 50Å silicon nitride layers showed a drop in device performance as a function of Cu/In ratio suggesting the possibility of formation of  $\text{In}_{\text{Cu}}$  antisite defect. We tried to compensate for Na by increasing the copper level in the film. The overall device performance improved and there were no specific trends within the substrate. The best device had a Voc of 400mV and a Jsc of  $35\text{mA}/\text{cm}^2$ . It can be seen that the Voc is low when compared to our standard device. It can be concluded from this that blocking off the diffusion of any amount of sodium hurts our device performance and copper cannot compensate for the absence of sodium. This showed that Na apart from occupying the copper sites ( $\text{Na}_{\text{Cu}}$ ) also has other beneficial effects.

In order to increase the sodium content in the film the molybdenum layer can be made less dense. As the molybdenum sputtering rate varied from  $1.2\text{Å}/\text{s}$  to  $3.2\text{Å}/\text{s}$ , the resistivity of the film decreased. This meant that the films were getting denser with increased sputtering rate. To obtain good device performance the sputtering rate had to be kept above  $2.7\text{Å}/\text{s}$ . The reduction in device performance at lower rate may be due to excess sodium in the film. The thickness of the molybdenum layer was decreased from  $10,000\text{Å}$  to  $4,000\text{Å}$  with the intention of letting more sodium into the CIGS film. It was found that a  $6000\text{Å}$  thick molybdenum layer gave the best device performance of 460mv and  $35.7\text{mA}/\text{cm}^2$ . The devices were also insensitive to the variation in metal ratio (uniform device performance throughout the substrate).

The structure of CIGS is strongly dependent on the structural properties of the molybdenum layer. Properties like morphology, grain size and stress state can affect the CIGS nucleation and growth process. Some of the results that we have observed may be due to the changes in the structure of the CIGS itself. The structural change may be because of two possible reasons. First, change in the sodium content in the CIGS film could have affected the structure. Second, the properties of the molybdenum film may be altered due to the variation in the deposition rate and due to the deposition of molybdenum on the silicon nitride barrier layer, thus affecting the CIGS structure.

In order to incorporate sodium in a controlled manner, a sodium source has to be deposited on molybdenum before the deposition of the CIGS layer and the SLG substrate could be coated with an alkali barrier layer like silicon nitride. The sodium source can be deposited either by evaporation of NaCl or by doing a NaCl solution treatment. The evaporation of NaCl may not be feasible in our laboratory because of the concern of cross contamination in the existing equipments.

One of the key process parameter in molybdenum deposition was found to be the discharge voltage during sputtering. The Voc's were found to decrease with increase in sputtering discharge voltage. To obtain good device performance the discharge voltage had to be kept below 600V. At around 700V the devices had poor adhesion to the back contact. This could be because of a high level of stress developed in the molybdenum film due to high discharge voltage.

The type IV recipe developed to incorporate gallium in the space charge region helped to improve the Voc's beyond 460mV. In this process, the total gallium thickness was split into 3 parts. The first part was called the back gallium, which was deposited

after the copper deposition. The second part was referred to as the middle gallium, which was deposited by splitting the indium selenide. The third part which was deposited in the 4<sup>th</sup> minute of selenization was called the top gallium. The gallium at the back of the device seemed to determine the amount of gallium that stayed in the front of the device i.e. lesser the gallium at the back of the device more is the migration from the front of the device. This showed that the kinetics of the process tends to create an automatic gallium profiling in the device. This inherent behavior could be exploited to improve the device performance.

It was observed that the increase in gallium level (beyond 200Å) in the front of the device (middle + top Ga) did not translate into a significant bandgap shift. This suggested some of the gallium that was deposited stayed as free gallium thus resulting in point defects, which affected the device performance. In order to circumvent this problem experiments like increasing the substrate temperature during precursor formation, adjusting the selenization timing and profile, and argon annealing, can be carried out.

The devices fabricated using the type IV process had Voc's as high as 490mV, Jsc's as high as 37.4mA/cm<sup>2</sup> and fill factors as high as 64%.

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