2004

High voltage conversion for MEMS applications using micromachined capacitors

Puneet Khanna

University of South Florida

Follow this and additional works at: http://scholarcommons.usf.edu/etd

Part of the American Studies Commons

Scholar Commons Citation

Khanna, Puneet, "High voltage conversion for MEMS applications using micromachined capacitors" (2004). Graduate Theses and Dissertations.
http://scholarcommons.usf.edu/etd/1111

This Thesis is brought to you for free and open access by the Graduate School at Scholar Commons. It has been accepted for inclusion in Graduate Theses and Dissertations by an authorized administrator of Scholar Commons. For more information, please contact scholarcommons@usf.edu.
High Voltage Conversion For Mems Applications
Using Micromachined Capacitors

by

Puneet Khanna

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering
Department of Electrical Engineering
College of Engineering
University of South Florida

Major Professor: Shekhar Bhansali, Ph.D.
John Bumgarner, Ph.D.
Shinzo Onishi, Ph.D.
Sang Chae Kim, Ph.D.
Kenneth Buckle, Ph.D.

Date of Approval:
November 10, 2004

Keywords: dc-dc converter, switched capacitors, mems, porous silicon

© Copyright 2004, Puneet Khanna
ACKNOWLEDGEMENTS

I am deeply grateful to Dr. Shekhar Bhansali for his invaluable guidance towards the completion of this work. I would also like to thank Dr. John Bumgarner and Dr. Shinzo Onishi for the valuable suggestions they provided all through this research. A very special thanks to the entire Largo team for all the efforts they have taken and patience they have shown for training the students.

From the Tampa team, Robert Tufts and Richard Everly need to be thanked for perfect operation of our cleanroom.

Finally, I am indebted to my family and friends for all the love and support that made this possible.
# TABLE OF CONTENTS

LIST OF TABLES ................................................................................................................................. iv

LIST OF FIGURES .............................................................................................................................. v

ABSTRACT ........................................................................................................................................... ix

CHAPTER 1: INTRODUCTION ....................................................................................................... 1

1.1 Definition of “High Voltage” in MEMS ................................................................................ 1

1.2 Powering MEMS ................................................................................................................ 2

1.3 Voltage Conversion Technique ....................................................................................... 5

CHAPTER 2: SWITCHED CAPACITOR DC-DC CONVERTER ................................................... 9

2.1 Basic Concept .................................................................................................................... 9

2.2 Charge Pumping .............................................................................................................. 11

2.3 Effect of Parasitic Elements in Switched Capacitor Circuits ........................................ 13

2.4 Topology Considerations ............................................................................................... 16

2.5 Standardized Charge Pump Designs ........................................................................... 21

2.5.1 Cockcroft and Walton Circuit ................................................................................ 21

2.5.2 Dickson Charge Pump ......................................................................................... 23

CHAPTER 3: PROTOTYPE CIRCUIT DEVELOPMENT .............................................................. 27

3.1 Independent Charge Circuit .......................................................................................... 29

3.1.1 Timer Connections ............................................................................................... 32

3.1.2 Cascaded Counter Circuit .................................................................................... 33
LIST OF TABLES

Table 1 – Output Comparison between First Converter and the Improved Version ........ 42
Table 2 - Output Comparison between Independent and Parallel Charge Circuit......... 46
Table 3 - Digilab XCRP Board CPLD Pinout ............................................................. 51
Table 4 - Output Voltage Ratio Settings................................................................. 52
Table 5 - Digilent XCRP Board Expansion Connector Pinout............................... 53
Table 6 - Comparison of Various Capacitor Types ............................................... 62
Table 7 - Comparison of Porous Silicon and DRIE Processes ............................... 87
Table 8 - Area Needed for 20 nF Capacitors ( mm$^2$) Using 100 µm Deep Pores....... 98
Table 9 - Area Needed for 20 nF Capacitors ( mm$^2$) Using 200 µm Deep Pores....... 98
Table 10 - Capacitance and Series Resistance Measurement of Plain Capacitor ....... 106
LIST OF FIGURES

Figure 1 – Basic Switched Capacitor Voltage Doubler .......................................................... 9
Figure 2 – Charge Redistribution between Capacitors .......................................................... 12
Figure 3 - Voltage Replication Charge Pump ...................................................................... 12
Figure 4 - Output of Voltage Replication Charge Pump ...................................................... 13
Figure 5 - Equivalent Circuit of Continuous Switching Charge Pump .............................. 15
Figure 6 - A SC Converter with Five Capacitors and Thirteen Switches ......................... 17
Figure 7 - Capacitor Configurations of the Five Capacitor Converter ............................... 17
Figure 8 - A SC Converter with Four Capacitors and Ten Switches ................................. 18
Figure 9 - Capacitor Configurations of the Four Capacitor Converter ............................. 18
Figure 10 - Modified Converter with Four Capacitors and Ten Switches ....................... 19
Figure 11 - Capacitor Configurations of Modified Converter .......................................... 19
Figure 12 - Cockcroft-Walton Voltage Multiplier .............................................................. 21
Figure 13 - Capacitor Configurations of Cockcroft-Walton Circuit ................................. 22
Figure 14 - Dickson Charge Pump ..................................................................................... 24
Figure 15 - Dickson Charge Pump Using Mosfets ............................................................ 25
Figure 16 - First Two Phases of Independent Charge Circuit ............................................ 29
Figure 17 - Block Diagram of Independent Charge Circuit ................................................. 31
Figure 18 - Connection Diagram of 555 Timer Used in Independent Charge Circuit ...... 32
Figure 19 - Pin Diagram of CD40161 Four Bit Programmable Counter....................... 33
Figure 20 – Cascade Configuration of Four Bit Counter........................................... 33
Figure 21 - Clear Logic for MOD 20 Count................................................................. 34
Figure 22 - Demultiplexer Connections..................................................................... 35
Figure 23 - Photograph of the Independent Charge Breadboard Circuit..................... 36
Figure 24 - Series Capacitor Bank of Prototype Circuit............................................. 37
Figure 25 - Highly Rippled Output from the First Independent Charge Circuit......... 37
Figure 26 - Output of 555 Timer................................................................................. 38
Figure 27 – Capacitor Charge Pulse Through Relay................................................... 39
Figure 28 - Output Using 1nF Capacitors.................................................................. 39
Figure 29 - Unfiltered Output of Improved Independent Charge Circuit.................. 41
Figure 30 - Filtered Output of the Improved Charge Circuit...................................... 41
Figure 31 - Parallel Charge Circuit............................................................................ 43
Figure 32 - Photograph of Parallel Charge Prototype Circuit................................... 44
Figure 33 - Unfiltered Output of Parallel Charge Circuit.......................................... 45
Figure 34 - Filtered Output of Parallel Charge Circuit............................................... 45
Figure 35 - Synchronization Pulses Required for High Voltage Converter............... 47
Figure 36 - Block Diagram of a CPLD...................................................................... 48
Figure 37 - DXCRP Development Board................................................................. 49
Figure 38 - Tunable High Voltage Converter............................................................. 50
Figure 39- Pin Diagram of CMOS Based Quadruple Switch SN74HC4066............. 55
Figure 40 - CMOS Switch Based High Voltage Converter...................................... 55
Figure 41 - Synchronization Output Pulses from the CPLD..................................... 56
Figure 42 - Converter Output with Load Connected Across 20 Capacitors ..................... 57
Figure 43 - Converter Output with Load Connected Across 15 Capacitors ..................... 57
Figure 44 - Converter Output with Load Connected Across 10 Capacitors ..................... 58
Figure 45 - Converter Output with Load Connected Across 5 Capacitors ....................... 58
Figure 46 - Increased Effective Surface Area of Electrode via Micromachining .............. 64
Figure 47 - The I-V Characteristic of a Silicon Electrode in Hydrofluoric Acid ............. 67
Figure 48 - Porous Silicon Setup ................................................................. 68
Figure 49 - Porous Silicon Fabrication Process ..................................................... 72
Figure 50 - Photograph of Porous Silicon Setup at USF ......................................... 74
Figure 51 - Initial Attempts at Porous Silicon Fabrication ....................................... 75
Figure 52 - Successful Porous Silicon Etching ....................................................... 77
Figure 53 - Pores Obtained Using 500 Micron Thick Wafers .................................... 79
Figure 54 - Typical Parallel-Plate Reactive Ion Etching System ............................... 80
Figure 55 - Pores Obtained in Initial Attempts at DRIE Processing .......................... 83
Figure 56 - 140 micron Deep Pores using DRIE .................................................... 84
Figure 57 - Conformal Coating of Polysilicon at Top of Pore .................................. 85
Figure 58 - Uniformly Thick Coating of Polysilicon over Entire Pore Wall .................. 85
Figure 59 - Polysilicon Coating near Bottom of Pore ............................................. 86
Figure 60 - Series Capacitor Bank Process Flow ..................................................... 89
Figure 61 - Unit Cell of Capacitor ........................................................................ 94
Figure 62 - Specific Capacitances ( nF / mm$^2$) for 100 µm Deep Pores ................. 96
Figure 63 - Specific Capacitances ( nF / mm$^2$) for 200 µm Deep Pores ................... 97
Figure 64 - Layer 1 of Mask - Trenches for Increase in Effective Area ...................... 100
Figure 65 - Layer 2 of Mask - Isolation Trenches .......................................................... 100
Figure 66 - Layer 3 of Mask - Polysilicon Etch Regions ............................................. 101
Figure 67 - Layer 4 of Mask - Metal Deposition Areas................................................. 101
Figure 68 - Single Block of Nine Capacitors................................................................. 102
Figure 69 - ONO Film (40nm – 100nm – 30 nm) on a Plain Wafer............................... 103
Figure 70 - Plain Capacitor Showing Bond Pads on Polysilicon and Silicon .............. 104
Figure 71 - Dielectric and Polysilicon Layers of Plain Capacitor ................................. 104
Figure 72 – Cross-Section of Etched Bond Pad Opening............................................. 105
Figure 73 - Capacitance Dependence on Frequency for the Fabricated Capacitors ..... 106
Figure 74 - Equivalent Circuit of the MOS Capacitor in Accumulation ...................... 107
ABSTRACT

This thesis explores high voltage converter circuits for MEMS applications using micromachined devices. A novel MEMS based tunable DC-DC converter has been developed. Conventional high voltage converters based on charge pumps are unable to convert voltages to higher than few tens of volts due to power handling limitations of the CMOS components. In order to overcome this limitation a high voltage circuit has been proposed, which when integrated with micromachined switches will generate output voltages in the range of 100 Volts. The converter is based on a two phase switched capacitor circuit, and allows regulation of voltage conversion ratio. Three prototype circuits have been built for proof of concept. A test program has been written for synchronized CPLD based control of the switched capacitors.

Individual capacitor fabrication technology is explored using two methods - Porous Silicon and DRIE processing. A micromachined capacitor bank has also been fabricated in silicon using a novel process sequence which provides for critical real estate savings and integration benefits. It enables on-chip integration of numerous
microcapacitors, without losing customized configurability of the capacitor bank. The technique utilizes polyimide to facilitate lithography on a highly contoured surface. Plain capacitors have been fabricated on silicon with oxide-nitride-oxide stack being used as the dielectric to provide a building block for further fabrication of a variety of capacitors.
CHAPTER 1
INTRODUCTION

1.1 Definition of “High Voltage” in MEMS

“High voltage” is a relatively ambiguous term when used in a general context. In layman terms, high voltage can be described as capable of producing sparks and delivering shocks to humans. However in the scientific domain, the distinction between high voltage and low voltage depends on the relevant application. Many scientific applications require voltages in the order of thousands of volts, while others need just a few millivolts. The term “high voltage” thus needs to be defined for the relevant realm of discussion – MEMS.

MEMS devices usually exploit common physical phenomena at atypically lower voltages. For example, on an everyday scale voltages higher than a few hundred or perhaps thousand volts are required to create an electric field with a gradient large enough to produce obvious electrostatic forces. However, the forces depend on the distance from the electrodes, and at the microscopic scale of MEMS, even a few tens of volts acts like a high voltage.

MEMS devices generally require voltages in the range of 1 to 100 volts. Most applications (such as thermal actuation) need voltages in the lower end of the spectrum, and an input of 1 to 12 V would suffice. This range of operation is not uncommon in the
IC industry and standard power supplies are available for the purpose. However occasionally, certain applications such as electrostatic actuation or microfluidic devices might need DC bias voltages ranging from 40 to 100V. This requirement is much higher than the supply voltage of deep sub-micron CMOS technology that is typically used in integrated circuits. Hence, specific voltage conversion schemes need to be implemented for such devices. This approximate range of voltage (40 – 100 V) henceforth will be referred to as “high voltage” in this thesis.

1.2 Powering MEMS

Powering MEMS devices pose unique complications due to the distinctive requirements from the power sources. A generic voltage source cannot be used for many MEMS applications because:

- MEMS devices are extremely small in size. A bulky power source would render most applications futile. Though some devices may be a part of a large mechanism, most MEMS devices need to be portable. Thus the power supply needs to lend itself to the packaging to enable deployment of the device.

- In many applications, micromachining has an inherent advantage of being an inexpensive alternative to conventional mainstream technology. Thus, for these applications, the power supply needs to be economical to retain the cost advantage.
Apart from these obvious limitations there are other considerations too. It has been stated earlier that the supply range for MEMS devices is 1 to 100V. Electrostatic MEMS devices can have even greater voltage requirements in the future. With the entire IC industry nudging towards lower operating voltages, the MEMS need may seem contradictory to technology progression. A closer inspection reveals that this contradiction is in fact an endeavor towards the same goal of higher efficiency. Many MEMS devices contain moving parts that often need to resonate at certain frequencies. The tuning voltage required is a function of the device design, there being a trade off between the voltage and other parameters like mechanical resonance frequency, electrical losses and linearity of device [1]. Thus, even though low voltage operation may be achievable via design changes, efficiency issues make it undesirable. These factors have led to the preferred voltage of operation for many devices to be greater than 10 V.

The high voltage requirement from the power source leads to additional complications. A supply that meets all the requirements of the micromachined device, might still be incompatible with the complete system. It needs to be kept in mind that most MEMS structures do not operate in isolation. They have a control or logic circuit that is integrated along with them so as to form system-on-chip devices. This implies that the power source is needed for both; the MEMS device and the accompanying control circuit. This places an additional constraint of dual compatibility on the power source.

There can be various approaches to solve the above issues. The easiest might seem to be the use of separate power sources for the MEMS device and the control circuit. Though a fast solution, it may be an expensive one. Also, having two different power supplies on the same system may affect the economic feasibility, and
simultaneously place additional space and weight burden. Another route may be to use dedicated high voltage technology and high voltage devices for the control circuit [1]. This again may not be cost effective and may limit the flexibility of the control logic.

These cumulative demands might seem unreasonable especially if one were to compare the standard voltage requirements of CMOS circuits (3.3 to 5 V) and the higher end voltage requirement of MEMS (up to 100 V). With newer implementations leaning towards microbatteries as the preferred source, powering MEMS structures would seem even more impossible. Here ironically, it is the very nature of these devices that comes to the rescue. MEMS applications requiring high voltages, such as electrostatic actuation, need a large charge buildup, hence large voltages, but very less current. Thus the actual power requirement in these devices is very low, with current needed being less than 1 mA. Since the batteries available can produce sufficient power for the purpose, one need only incorporate a voltage conversion circuit so as to provide high voltage to the micromachined element, while the rest of the system can draw power directly from the voltage source.

High Voltage Conversion thus becomes an enabling technology for the transition of many micromachined devices from concept to reality. High Voltage Conversion schemes and their implementation thus need to be customized specifically for MEMS applications.
1.3 Voltage Conversion Technique

Traditionally, the simplest way of converting voltage is by using coil based transformers. Unfortunately this route is not very attractive when applied to Microsystems. There are various reasons for this –

- Transformers and inductors are magnetic elements and this makes them unsuitable for monolithic integration. Although chip ferrites for surface mounting have made much progress, they are still unsatisfactory. [2]

- Transformers are extremely bulky components. Increasing the frequency of operation can reduce their size to some degree; nevertheless they still remain relatively voluminous and cannot be easily realized using MEMS technology.

- Conversion is extremely lossy when using magnetic elements. Losses tend to exaggerate at higher frequencies with magnetic core losses, eddy current losses and hysteresis effects becoming more severe. Practically, this means there is a limit to which one can reduce the size of the transformer by increasing frequency.

- Operation down at zero load is not possible with transformers. They need dummy loads and complex control techniques. At the micro scale any conversion that is not self-regulated makes the technique largely infeasible.
Another technology that is available is the use of switched capacitors. Multiple capacitors are used to progressively store energy from a voltage source via a synchronized charge transfer mechanism. This energy is dissipated via the output circuit at a higher voltage. The use of “Switched Capacitor DC-DC Converters” is an interesting alternative to the traditional approach, with none of the aforementioned downsides. This technique has certain advantages as compared to other techniques –

- No magnetic inductors or transformers are present. Thus, they are more suitable for integration with IC technology.

- Capacitors in general are less bulky than inductors and thus these transformers are small in size, light in weight and have a high power density.

- They have a very high efficiency when compared to all classical power supplies in the small power range of a few watts. By reducing switching frequency the total power losses can be reduced to zero.

- When completely unloaded, the converter output voltage assumes a value uniquely determined by the converter topology [3]. Thus operation at zero load is possible with no need for dummy loads.

- The voltage conversion ratio is not rigid and can be changed according to need, via simple switching variations, without any permanent change on the topology.
• There are no AC harmonics present in the output waveform due to direct DC to DC conversion.

• Very good regulation is possible; it being able to maintain the output voltage at a desired constant value despite large variations in load and input voltage [4].

• Electromagnetic interference problems are minimal due to a continuous input current coupled with the absence of magnetic devices (L•di/dt is negligible) [4].

Despite the above advantages, switched capacitor circuits also suffer from certain drawbacks.

• The maximum output voltage that can be reached is limited by the switches. The switching elements that are normally used in these circuits are CMOS based or at best application specific FET’s. These have physical current carrying limitations beyond which the circuit logic fails. The maximum output achieved thus far using ASIC’s is around 30 V.

• As the voltage conversion ratio increases, the number of capacitors required increases. Although capacitors do take lesser area than inductors, a large number of them may reduce the area benefits normally expected.
• There is no one single topology available that can be universally applied. Numerous topologies are possible and their theoretical analysis is difficult, especially as the number of elements increase. It is quite tedious to establish the state-space equations, let alone find the solutions. Also some of the important parameters of the converters, such as the relationship between Pulse Width Modulation (PWM) and Frequency Modulation (FM), the relationship between switching frequency and the capacitance, the restriction of the duty ratio, etc., may be concealed [5].

Notwithstanding the above limitations, switched capacitor DC-DC converters have enough advantages to warrant their use in MEMS applications. This thesis explores various techniques with which this technology can be adapted specifically for MEMS. New designs have been examined for their practical viability. Enhancements have been made over traditional methods, which eliminate two of the drawbacks mentioned above. Firstly, MEMS based switches have been proposed to replace the CMOS based switches thus removing the constraint on the output voltage level. Secondly, micromachined capacitor bank has been developed which increases the real estate savings. It is MEMS itself that has made these enhancements possible –a perfect example of a technology furthering itself.
CHAPTER 2
SWITCHED CAPACITOR DC-DC CONVERTER

2.1 Basic Concept

In this section the working principle behind switched capacitor voltage conversion circuits will be examined. The most common switched capacitor voltage converter is the voltage doubler circuit shown in Figure 1 below. Though this is the simplest form of the circuit, it illustrates certain concepts which are common to all such converters.

![Figure 1 – Basic Switched Capacitor Voltage Doubler](image)

This voltage doubler consists of two capacitors, the charge pump capacitor C1 and the output capacitor C2, and two switches. The two switches are synchronized and switch together at every trigger from the control circuit (not shown here). During the first half of the switching cycle, capacitor C1 is charged to the input voltage $V_{IN}$. During the
second half of the cycle, this capacitor is placed in series with the input voltage. Thus during the discharge cycle the output capacitor is charged to twice the input voltage, thereby accomplishing the voltage doubling function. The average input current is approximately twice the average output current. The duty cycle – defined as the ratio of charge cycle time to the entire switching cycle time – is kept at 50 %, because that generally yields the optimal charge transfer efficiency. The duty cycle however is specific to this circuit, and different configurations would have different optimization conditions.

It generally takes a few cycles for the initial transient conditions to settle down. After the steady state is achieved, the charge pump capacitor only has to supply a small amount of charge to the output capacitor during each switching cycle. The switching frequency and the load current determine the amount of charge transferred. One can easily notice that while the pump capacitor is being charged by the input voltage, the output capacitor C2 supplies the load current. The output capacitor thus gets discharged continuously while getting charged intermittently. As the capacitor discharges, the load current causes a slight drop in the output voltage. This is seen as a component of the output voltage ripple.

Since all forms of the switched capacitor circuit work on the principle of synchronized charge-discharge, some form of voltage ripple would always be present in the unfiltered form of output. The ripple can be reduced by either using larger capacitors or by operating at higher frequencies. Since smaller volume requirement demands smaller capacitors, there is an effort to reach higher and higher operating frequencies. However, switching speeds have practical limitations due to switching losses and switch reliability.
Hence, the efficiency of switched capacitor converters is largely component dependent. Furthermore, these converters do not maintain high efficiency for a wide range of voltage amplification ratios. This is because the current ratio is scaled according to the basic voltage conversion, and thus any output voltage magnitude less than that for which the circuit is designed, will resulting additional power dissipation within the converter, and efficiency will be degraded proportionally.

2.2 Charge Pumping

A very important phenomenon in switched capacitor circuits is the concept of charge pumping. As stated earlier these circuits amplify voltage by accumulating charge across capacitors. Thus charge needs to be progressively “stacked” across the output capacitors. This technique is commonly referred to as “charge pumping”, and is discussed below.

Figure 2 below shows two capacitors, C1 and C2 charged to voltages V1 and V2 respectively. When the switch is closed, the charge gets redistributed via an impulse of current. The total charge stored on the combined capacitor bank is –

\[ Q_T = C1 \cdot V1 + C2 \cdot V2. \]

This charge is distributed between the two capacitors, the total sum remaining constant according to the principle of conservation of charge.
The net voltage $V_T$ across the parallel combination is given by –

$$V_T = \frac{Q_T}{C_1 + C_2} = \frac{C_1 \cdot V_1 + C_2 \cdot V_2}{C_1 + C_2} = \left( \frac{C_1}{C_1 + C_2} \right) V_1 + \left( \frac{C_2}{C_1 + C_2} \right) V_2$$

The same principle of charge redistribution is used in charge pumping. Consider the basic charge pumping circuit shown in Figure 3. This is not a voltage amplification circuit, rather a simple voltage replication one.
The voltage replication circuit consists of two capacitors similar to the voltage doubler shown earlier. The first is the pump capacitor C1 and the other is the output capacitor C2. At initial steady state, the pump capacitor is charged to $V_{\text{IN}}$. When connected to C2, the charge gets redistributed as per the principle explained above. Assuming $C1 = C2$, both the capacitors now are charged to voltage $V_{\text{IN}}/2$. On the next triggering of the switch, C1 is charged back to $V_{\text{IN}}$. And on redistribution the voltage possessed by either of the capacitors will now be $(V_{\text{IN}} + V_{\text{IN}}/2) / 2$, i.e. $V_{\text{IN}}/2 + V_{\text{IN}}/4$. Similarly, after the third charge transfer cycle, the output voltage is pumped to $V_{\text{IN}}/2 + V_{\text{IN}}/4 + V_{\text{IN}}/8$. As this process continues, the output voltage asymptotically approaches $V_{\text{IN}}$. The waveform below illustrates the behavior of the output voltage.

Figure 4 - Output of Voltage Replication Charge Pump

2.3 Effect of Parasitic Elements in Switched Capacitor Circuits

In order to fully understand various issues concerning voltage conversion using capacitors, the theoretical as well as practical functioning of capacitors need to be examined. Any capacitor used in the real world has an equivalent series resistance (ESR)
and equivalent series inductance (ESL) associated with it. Though these parasitic elements do not affect the ability of a capacitor to store charge, they do effect the efficiency of the voltage converter. This is because the dynamic properties of the capacitors become highly significant at such high frequencies.

If an ideal capacitor were to be charged with an ideal voltage source, the charge build-up in the capacitor would take place instantly, corresponding to a unit impulse of current. However, in the practical circuit the combined resistances of the switches and ESR’s of the capacitors lead to an effective resistance, and similarly an effective inductance, to be present in the current flow path. These parasitic elements limit the peak current, and thus increase the charge transfer time. The amount of power dissipated across these parasitic elements is a complex function of their physical magnitude as well as the dynamic settings of the circuit. Consider the voltage replication charge pump described in the earlier section. Assume that steady state conditions have been reached. The charge transferred in each cycle is \( \Delta Q = C1(V_{IN} - V_{OUT}) \). Assume that the switching frequency is \( 'f' \). Thus the average current flowing through the circuit would be,

\[
I = f \cdot \Delta Q = f \cdot C1(V_{IN} - V_{OUT}), \text{ or}
\]

\[
I = \frac{V_{IN} - V_{OUT}}{1/(f \cdot C1)}, \text{ or}
\]

\[
I = \frac{V_{IN} - V_{OUT}}{R}
\]
The quantity $1/(f \cdot C_1)$, can be considered as an equivalent resistance “$R$”, connected between the source and the load.

The resistance “$R$” is a virtual resistance that arises due to the dynamic nature of the circuit. The resistance, though virtual, has a real power dissipation associated to it. This power is forced to be dissipated across the switch resistances and other parasitic quantities. Hence regardless of how low the parasitic element magnitudes are reduced, there will always be a finite power loss associated with the frequency of switching. The virtual resistance “$R$” can be reduced by increasing the frequency of operation, thereby minimizing power loss. However, increasing the frequency also increases the switching losses. Thus, there is a balance to be achieved between “virtual losses” and the “real losses”. Hence the highest efficiency that can be obtained from any switched capacitor circuit is frequency dependent, the optimal frequency being a complex function of component properties and the topology of the circuit.

Figure 5 - Equivalent Circuit of Continuous Switching Charge Pump
2.4 Topology Considerations

There have been various kinds of charge pumps that have been proposed since the discovery of this concept. The implementation of each circuit is highly process dependent and each one has its own advantages and disadvantages. As a general guideline, though not a rule, the more complex a circuit is, the more efficient it is probably going to be, and the lesser components it would use. The ideal voltage conversion ratio is a factor the converter topology and is not dependent on the static properties of the capacitors and switches. The same number of switches and capacitors might be configured differently to provide a different voltage conversion ratio. Another important criterion is the number of phases used in the circuit. One triggering pulse is supposed to toggle a set of switches simultaneously. The number of such pulses used in a circuit, all of them synchronized with each other, determines the phase of the circuit. The basic voltage doubler described earlier was a single phase circuit. Most commonly used circuits are double phase, though higher phase ones are occasionally used.

Makowski and Maksimovic [3] illustrated the configuration dependence of the voltage conversion ratio via the two-phase converters described below. The converter shown in Figure 6 has five capacitors and thirteen switches. The switches are triggered using two non overlapping clock pulses shown above the circuit. The switches corresponding to a particular clock pulse are indicated as numbered phases 1 and 2. When switches 1 are on, all capacitors except the output capacitor (the capacitor across the load R), are placed in parallel to the voltage source “$V_g$”. When switches 2 are on, all the capacitors are placed in series with the voltage source, and dump charge onto the load. Figure 7 shows the two
configurations in which the capacitors are interconnected during phase 1 and phase 2. By inspection, the ideal output voltage is $V_o = 5 \ V_g$ (when the converter is unloaded).

![SC Converter with Five Capacitors and Thirteen Switches](image)

*Adapted from Makowski and Maksimovic [3]*

![Capacitor Configurations of the Five Capacitor Converter](image)

*Adapted from Makowski and Maksimovic [3]*

The figure below shows another switched capacitor converter. This one is also a two phase circuit but has four capacitors and ten switches.
Capacitor configurations corresponding to phases 1 and 2 of this converter are shown in the figure below. This converter too gives an ideal voltage conversion ratio of 5. This circuit has the obvious advantage that it uses lesser components than the previous converter. Also it has a lower output resistance than the previous converter. However it has a disadvantage that all capacitors do not hold the same capacitor voltages, unlike in the previous case.
Thus it is seen that lesser number of components can provide the same voltage conversion if configured in a superior manner, though there is a practical limit to it. Furthermore, there is always a compromise between efficiency and regulation. It is normally difficult to ensure good output voltage regulation along with a high conversion ratio especially in the presence of wide load variations and input voltage variations.

Another interesting observation is that different topologies may be possible with the same number of components giving the same output voltage ratio. The figure below shows another switched capacitor converter with four capacitors and ten switches, having a voltage conversion of 5.

Figure 10 - Modified Converter with Four Capacitors and Ten Switches

Adapted from Makowski and Maksimovic [3]

Figure 11 - Capacitor Configurations of Modified Converter

Adapted from Makowski and Maksimovic [3]
Switched capacitor circuits can be used to perform step down conversions as well. The maximum voltage conversion ratio that is possible using a certain number of capacitors is defined by Fibonacci numbers. For a given number of capacitors \( k \), the maximum step-up or step-down ratio is given by the \( k^{th} \) Fibonacci number, while the bound on the number of switches required in any switched capacitor circuit is \( 3k – 2 \) [3].

Fibonacci numbers are defined as per the recursive definition –

\[
F_0 = 1, \\
F_1 = 1, \\
F_k = F_{k-2} + F_{k-1}, \text{ for } k > 1.
\]

This provides the sequence,

1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, …

This means that for (1, 2, 3, 4, …, \( n \)) capacitors, the maximum voltage conversion ratio that can be achieved using two phase switched capacitor circuits is (1, 2, 3, 5, 8, …, \( n^{th} \) Fibonacci number). Makowski and Maksimovic also state another important implication of this principle, in that; it specifies the complete set of realizable conversion ratios for a given number of capacitors. All possible conversion ratios are a ratio of the Fibonacci numbers up to the \( k^{th} \) number. For example, for \( k = 2 \), the set consists of \( 1/2, 1 \) and \( 2 \). For \( k = 4 \), there are 19 possible ratios: \( 1/5, 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 1, 5/4, 4/3, 3/2, 5/3, 2, 5/2, 3, 4 \) and \( 5 \). Negative sign of all these ratios is also possible implying negative voltage output.

It should be kept in mind that the topology of the circuit is the only factor that determines the ‘ideal’ voltage conversion ratio. The ‘real’ conversion ratio also has
dependencies on the values of capacitances, ESR and switch resistances, switching
frequency, clock duty ratios etc. to name a few.

2.5 Standardized Charge Pump Designs

As stated earlier there have been a variety of standardized charge pump designs that have
been proposed by various researchers. Certain standardized topologies are highly popular
because of their simplistic yet highly efficient designs. A few of these topologies are
discussed below –

2.5.1 Cockcroft and Walton Circuit

Cockcroft and Walton were English and Irish physicists who are credited with building
the first switched capacitor voltage multiplier in 1929. Their voltage multiplier was used
to generate voltages around 800 KV, for the purpose of accelerating protons to energies
higher than that of natural alpha particles (They were awarded the Nobel prize for physics
in 1951). Though initially used for such ultra high voltages, the multiplication concept is
relevant for any voltage magnitude.

Figure 12 - Cockcroft-Walton Voltage Multiplier

Adapted from Pylarinos [6]
The figure above shows the basic Cockcroft-Walton voltage multiplier circuit [6]. The two phases of this circuit are represented by Φ and Θ. The circuit consists of two sets of series banks of capacitors. The first set consists of three capacitors \( C_A, C_B, \) and \( C_C \) having equal capacitance. The capacitor \( C_A \) is connected to the supply voltage \( V_{DD} \). The second set of series capacitors, \( C_1 \) and \( C_2 \), interface with the first set via three switches. For easy computations, let us take \( C_1 = C_2 = C_A \). The configurations during the two phases are shown below.

![Diagram of Cockcroft-Walton Circuit]

**Figure 13 - Capacitor Configurations of Cockcroft-Walton Circuit**

During the first switch phase Φ, the capacitor \( C_1 \) is connected parallel to \( C_A \), and is thus charged to \( V_{DD} \). In the next phase Θ, \( C_1 \) is connected parallel to \( C_B \), which is yet uncharged. Hence the charge on \( C_1 \) gets redistributed between the two and each is charged to voltage \( V_{DD}/2 \). In the next cycle Φ, \( C_2 \) and \( C_B \) are connected in parallel, and now each would hold charge with potential \( V_{DD}/4 \). In this cycle \( C_1 \) is again charged to...
V_{DD}. Again in the next cycle, charge on C_2 is redistributed with C_C and each would be at voltage V_{DD}/8. It is obvious that charge is being pumped in this way from each capacitor to another one higher in the ladder. After a few cycles, all capacitors would asymptotically approach the same voltage V_{DD}, and the output voltage would be 3V_{DD}.

Despite being an old design, this circuit finds applications in today’s electrical devices in its original as well as modified form. One can easily notice that the charge pumping technique of this circuit is extendable to more capacitors. By adding more stages to the ladder, any multiple of the supply voltage may be obtained. However, practically, this multiplier becomes inefficient in its monolithic integrated form because of the relatively large on-chip capacitance. Also, the output impedance of the circuit increases multifold with the addition of each extra stage.

### 2.5.2 Dickson Charge Pump

In an endeavor to eliminate the limitations of the Cockcroft-Walton circuit, Dickson proposed a charge pump in 1976. This voltage multiplier has the advantage of being compatible to monolithic integration. Though being similar to the previous circuit, it displays higher efficiency even in the presence of stray capacitance. Also, its drive capability is independent of the number of stages [6]. The figure below shows the Dickson charge pump.
Figure 14 - Dickson Charge Pump

Adapted from Starzyk et. al. [7]

The Dickson charge pump consists of two antiphase clocks \( \Phi_1 \) and \( \Phi_2 \), each having amplitude of \( V_\Phi \) (For simplicity \( V_\Phi \) is shown equal to \( V_{in} \) in this example, though they can be different). The diodes function as self-timed switches characterized by a forward bias voltage, \( V_d \). The voltage multiplier pumps charge along the diodes while the capacitors are successively charged and discharged during each clock cycle. When clock phase \( \Phi_1 \) goes low, the first diode conducts till the voltage at node 1 is \( V_{in} - V_d \). The next trigger causes \( \Phi_1 \) to switch to voltage \( V_{in} \), which causes the voltage at the first node to become \( V_{in} + (V_{in} - V_d) \). Since \( \Phi_2 \) is at ground potential, the second diode conducts until voltage at the second node becomes \( V_{in} + (V_{in} - V_d) - V_d \). When \( \Phi_1 \) goes low again, and thus \( \Phi_2 \) goes to \( V_{in} \), the potential at node 2 becomes, \( V_{in} + (V_{in} - V_d) - V_d + V_{in} \), i.e. \( V_{in} + 2(V_{in} - V_d) \). Similarly, after \( N \) stages, the output voltage is given by,

\[
V_{out} = V_{in} + N(V_{in} - V_d) - V_d \\
= (N + 1)(V_{in} - V_d)
\]
Thus the idealized voltage gain of the Dickson charge pump is directly proportional to the number to stages. Unfortunately, in practice, this is not the case in the CMOS based circuit. The figure below shows MOSFET’s being used as the switching elements. The body terminals of the MOSFETs are fixed to a constant voltage to ensure stable operation of the converter. Due to the cascaded structure of the MOSFETs they are susceptible to body effect, thus increasing their threshold voltage. Consequently the stage gain reduces - more sharply so for each successive stage. Therefore practically, the output voltage of the Dickson charge pump cannot be a linear function of the number of stages.

\[ V_{\text{out}} = C \frac{V_{\text{in}}}{N} \]

**Figure 15 - Dickson Charge Pump Using Mosfets**

*Adapted from Pylarinos [6]*

The Dickson pump suffers from other drawbacks also. The circuit has stray capacitances present at every node, reducing the effective input voltage. This causes the pumping gain to lessen for lower inputs. Hence this circuit is not preferred for very low voltage supplies. Furthermore, the circuit’s efficiency from current feeding point of view is relatively poor. Application of this device is thus restricted to cases with zero DC power consumption [6].
It is evident from the above discussion that CMOS based switches hinder the optimal functioning of switched capacitor converters. The use of micromachined switches has thus been proposed to overcome the aforementioned problems.
CHAPTER 3
PROTOTYPE CIRCUIT DEVELOPMENT

The previous chapters laid down the need for high voltage generation for MEMS, and discussed common approaches towards high voltage generation. The ultimate aim of this project is to develop a high voltage converter customized to the requirements of micromachined devices. As per the discussions in the first chapter, the need is for a multiplier to convert a standard CMOS driving voltage (around 5 V) to the higher end MEMS requirement of 100 V. Voltage multipliers that have been developed using standard IC based switches have not been able to provide voltage levels greater than a few tens of volts, due to low junction breakdown voltage of today’s CMOS technology. The situation is even worse in the case of bipolar transistors as their threshold voltage, due to its logarithmic dependence on the doping concentrations, has not changed considerably [8]. Thus the only solution to developing a 5 V to 100 V converter is to explore alternate forms of switching.

Valizadeh [8] at University of Michigan is currently developing a micromachined charge pump by replacing standard CMOS switches by micromachined switches. This research is adopting the same principle to build the high voltage converter. Various kinds of electrostatic and thermal switches have already been successfully fabricated and tested at USF. The actual design and fabrication of the micromachined switches, is discussed
elsewhere [15]. The micromachined switches do not rely on an electrical barrier cut-off like their CMOS based counterparts. Since they emulate mechanical switches, they have a very high current limit. Also, they can achieve very high frequency operation without much stray effects. It is interesting to see that MEMS technology thus comes to its own aid, and provides a way of developing a customized voltage supply, which could not be built using conventional methods.

This project goes one step further than to merely build a high voltage converter. A power source needs to be built that is small enough to serve a MEMS device without its own size being a liability. As mentioned in the first chapter, switched capacitor circuits lose their size advantage if numerous stages are used – an outcome of space encroachment by multiple individual capacitors. Thus, micromachined capacitors have been built which are not only small but also fabricated in an array formation so as to minimize their area requirement. This is further discussed in the forthcoming chapters.

The segmented nature of this project required an independent operational verification of its various components. Some form of a test bench was essential for this purpose. Thus a need was felt to construct a prototype of the converter to serve as the validation board for the micromachined parts (switches and capacitors). The prototype also provides the proof of concept to establish the practical feasibility of 5V to 100V conversion. Thus, standard off-the-shelf parts were used to construct first generation prototypes; the parts intending to simulate the working of the corresponding micromachined element. Two different prototypes were built to this effect. The construction of these circuits and results obtained will be discussed here. A third
prototype was built to develop microprocessor based logic control for switched capacitor circuits, and will be discussed later in the chapter.

3.1 Independent Charge Circuit

This is perhaps the simplest form of high voltage conversion logic for achieving such high conversion ratios. It consists of a series bank of capacitors, each capacitor being charged one at a time via the voltage input, while the output is taken across the entire voltage bank.

![Diagram of Independent Charge Circuit]

**Figure 16 - First Two Phases of Independent Charge Circuit**

Figure 16 shows the first two phases of the circuit. Twenty capacitors (C₁ to C₂₀) are permanently connected together in series. During the first phase, the voltage supply (V_in
= 5 V) is connected across the first capacitor C₁, charging it to 5 volts. After the next clock trigger, circuit connections alter, shifting the position of the voltage supply such that it is now connected across C₂. In the third phase it is connected across C₃, and so on. The twentieth phase connects the voltage supply to the last capacitor in the series, after which the cycle repeats from the first phase. Hence one can see each capacitor being charged one at a time to 5V. Since there are 20 capacitors, the ideal unloaded output should be 100 V.

In order to implement the above circuit, off-the-shelf DIP packaged IC’s were used to form the control logic. Mechanical relays were used as the switching elements, along with commercially available 1µF general purpose capacitors. The clock pulse was provided via a 555 timer configured as an Astable multivibrator. This pulse was fed to a counter logic. Two four bit binary counters were cascaded so as to form an eight bit counter. A MOD 20 reset logic was used so as to reset the counter after every nineteenth count, i.e. the counters count 0 to 19, and then are reset to 0 again. The five bit output from the counters was fed to cascaded 4:16 demultiplexers. This meant that only one output line out of the first 20 outputs was active low at any given instant. Outputs 21 to 32 of the demultiplexers were not in use. All of the 20 active outputs were connected to an inverter to convert the active low signal to active high. This signal was connected to an amplifier stage made of a NPN transistor, which serves to provide the adequate triggering voltage to the relay switches. Double pole double throw relays were used as switching elements. The triggering pins of the relays were isolated from the normally open (NO) and normally closed (NC) pins. To ensure perfect isolation between the triggering logic and the capacitor bank, two separate voltage supplies were used for this
circuit. One pole of every relay was connected to the positive of the capacitor charging voltage supply, and another pole to the negative terminal.

At every new pulse generated by the 555 timer, the counter increments, thus setting the next output of the demultiplexer to active low. The output of the corresponding inverter is set to high, thus toggling the switch of the corresponding relay from normally closed pin to normally open pin. This connects the voltage supply across the corresponding

Figure 17 - Block Diagram of Independent Charge Circuit

At every new pulse generated by the 555 timer, the counter increments, thus setting the next output of the demultiplexer to active low. The output of the corresponding inverter is set to high, thus toggling the switch of the corresponding relay from normally closed pin to normally open pin. This connects the voltage supply across the corresponding
capacitor. At the same time, the input to the previous relay is goes from high to low, thus opening the connections of the previous capacitor from the supply. In this way the voltage supply virtually shifts position from one capacitor to next.

The following IC components were used to realize this circuit:

- Timer – NE555P
- Counter – CD40161
- NAND gate (reset logic of counter) – SN74LS30
- Demultiplexer – SN74154
- Inverter – SN74LS04N

### 3.1.1 Timer Connections

![Connection Diagram of 555 Timer Used in Independent Charge Circuit](#)

\[
\begin{align*}
R_2 &= \frac{T_{\text{space}}}{0.7C} \\
R_1 &= \left[\frac{T_{\text{mark}}}{0.7C}\right] - R_2
\end{align*}
\]

Figure 18 - Connection Diagram of 555 Timer Used in Independent Charge Circuit
Figure 18 shows the connection of the 555 timer running in astable mode. The duty cycle and frequency of the timer is regulated via the capacitor marked “C” and two resistors $R_1$ and $R_2$. In the actual circuit “C” was chosen to be $1\mu F$ and potentiometers were used in placed of resistors $R_1$ and $R_2$. This enables real time variation of frequency and duty cycle while the converter is switched on.

### 3.1.2 Cascaded Counter Circuit

![Figure 19 - Pin Diagram of CD40161 Four Bit Programmable Counter](image)

![Figure 20 – Cascade Configuration of Four Bit Counter](image)
The four bit counters are cascaded as shown in Figure 20. Outputs Q1 through Q4 of the first counter serve as the least significant bits of the count signal, while output Q1 of the second counter serves as the most significant bit of the count signal. (The count signal being MOD 20 requires only five bits). Outputs Q2 through Q4 of the second counter are left unconnected. The five bits of the count signal are connected to a NAND gate as shown. Thus the output of the NAND gate goes low when its input is decimal 19 (binary 10011). This signal is fed to the clear line of the two counters. Thus whenever the output of the counter is 19, it is set back to 0. Thus the counter counts up from 0 through 19 (MOD 20 count).

3.1.3 Cascaded Demultiplexer Circuit

The demultiplexing logic is illustrated in Figure 22. The demultiplexer SN74154, can be selectively activated, thus enabling its cascading. When pins 18 and 19 of the multiplexer are set to active low, the multiplexer operates as usual with active low output. When either of them goes high all output pins are set to active high. The most significant bit of the 5 bit count is connected to pin 18 while pin 19 is connected to
ground. Thus, when the MSB of count signal is 0, DEMUX 1 operates and when the MSB is 1, DEMUX 2 operates giving us control of relays 17 through 20.

Figure 22 - Demultiplexer Connections

3.1.4 Results

The circuit was constructed as per the outlined logic on a breadboard with the components mention earlier. Various kinds measurements were taken in order to fully characterize the circuit. The figure below shows a photograph of the implemented circuit.
It was observed that the output of the circuit varied with frequency and duty cycle of the
555 timer output. In an endeavor to maximize the converter output, the two rheostats
were adjusted till the peak voltage was as high as possible. The capacitance “C” related to
the timer was changed too, and the value of 1µF was chosen as it provided the highest
gain. The measurements listed correspond to this frequency. It was observed that the peak
voltage was highest at the maximum possible frequency which allowed reliable switching
of the relays. Beyond an approximate frequency of 100 Hz, the large switching time of
the relays cannot keep up with the short triggering pulses, resulting in false switching.
Hence, the output suddenly drops to zero beyond this point.
Although the circuit did convert voltage to a higher value, the conversion was unsatisfactory in the first attempt as the output obtained was highly rippled. This was corrected in the further attempts as discussed.
Various observations from the output of the first independent charge circuit (Figure 25) are as follows:

- Period – 258.1 ms
- Frequency – 3.874 Hz
- Peak to peak voltage – 55 V
- High peak – 88V
- Low peak – 33 V
- Mean voltage – 66.2 V
- RMS voltage – 67.6 V

Output of 555 timer (Figure 26) corresponding to maximum gain:

- Frequency – 69.3 Hz (equivalent to relay switching freq.)
- Period – 14.43 ms
- Positive pulse width (Tmark) – 10.01 ms
- Negative pulse width (Tspace) – 4.424 ms
- Duty cycle – 69.34 %

![Figure 26 - Output of 555 Timer](image)
Charging time for each capacitor = 5.60 ms

Circuit performance was also validated using capacitors with lower capacitance values of 1nF.
The peak output obtained using 1nF capacitors was only 11 V. Circuit was unsuccessful with 1nF capacitors due to fast discharge times of these capacitors. Switching of the relays was too slow to compete with the discharge times. This is as expected, because high frequencies are essential for switched capacitor converters to work with low capacitance values. Since mechanical relays cannot switch at high frequencies, this prototype circuit thus cannot be validated using lower value capacitances.

The first independent charge circuit gave a mean output of 66V from an input of 5V, as seen in Figure 25. This is high enough for crude validation of the conversion principle, but is still low considering an ideal of 100V. Furthermore the output was highly rippled. The difference between the high peak and the lowest trough was 55V, which is just too high for any practical filtering.

Changes were made in the logic of the original circuit in an attempt to improve the output. As explained earlier, the circuit uses a 5 bit counter being used in a MOD 20 configuration. It was found that the clear function of the counter was synchronous in nature, causing a one pulse delay between charging of the 20th capacitor and the 1st one. After this time lag was removed, the ripple reduced so drastically that it was possible to filter out the remnants by using a filtering capacitor in parallel to the capacitor bank. The filtered output voltage was constant at around 82 V. The total voltage variation was just 400mV as compared to 55 V earlier.
Figure 29 - Unfiltered Output of Improved Independent Charge Circuit

Figure 30 - Filtered Output of the Improved Charge Circuit
The table below illustrates the improvement from the output of the first circuit, to that of the newer version.

Table 1 – Output Comparison between First Converter and the Improved Version

<table>
<thead>
<tr>
<th></th>
<th>OLD CIRCUIT (UNFILTERED OUTPUT)</th>
<th>NEW CIRCUIT (FILTERED OUTPUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean voltage</td>
<td>66.2 V</td>
<td>81.7 V</td>
</tr>
<tr>
<td>RMS Voltage</td>
<td>67.6 V</td>
<td>81.7 V</td>
</tr>
<tr>
<td>High voltage</td>
<td>88 V</td>
<td>82 V</td>
</tr>
<tr>
<td>Low voltage</td>
<td>33 V</td>
<td>81.6 V</td>
</tr>
<tr>
<td>Peak to peak voltage</td>
<td>55 V</td>
<td>400 mV</td>
</tr>
</tbody>
</table>

The successful implementation of this circuit design was significant in that it validated the possibility of obtaining a voltage of around 100V on a breadboard. It also meant that any other topology can also be verified using the same components and a similar approach.

3.2 Parallel Charge Circuit

Though a sufficiently good output was obtained from the independent charge circuit, the need was felt to build a more efficient design which can serve as the final topology of the high voltage converter for MEMS. This project aims at establishing the viability of a high voltage converter consisting of MEMS components and obtaining voltages in the range of 100 V. A highly complex topology is not needed to achieve this goal as the concept can
be extended to any other design. The choice of topology and various efficiency considerations being application specific will need to be addressed individually for each application. A basic two phase converter is chosen to be the demonstration base.

The figure below shows the circuit diagram of the parallel charge circuit. This circuit has already been discussed in the previous chapter. The switches marked 1 and 2 are triggered using opposite phased pulses. During phase 1, all capacitors are connected to the voltage supply in parallel configuration. Thus, all capacitors get charged simultaneously to 5 V. During the next phase, the switches marked 1 open, and switches marked 2 close. It is evident that the capacitors are now connected in series fashion, and discharge across the load. Thus, the configuration of capacitors toggles between parallel and series connection at every triggering pulse. While the circuit diagram shown here shows only four switched capacitors for explanatory purposes, the prototype circuit had twenty capacitors connected in the same fashion. Thus, the ideal unloaded voltage is 100 V for this circuit.

Figure 31 - Parallel Charge Circuit
The circuit was built using the same components as in the previous prototype. The triggering pulse from the 555 timer was fed to a high gain amplifier consisting of a dozen cascaded NPN transistors. This amplifier simultaneously switched same phase relays. The triggering pulse from the timer is also fed through an inverter, whose similarly amplified output toggles the other bank of switches.

![Figure 32 - Photograph of Parallel Charge Prototype Circuit](image)

It is obvious from the circuit diagram of the circuit, that the switched capacitors supply the load only during the discharge cycle, and are isolated from the load during their charge cycle. This is unlike the independent charge design where the capacitors supply the load continuously. In this case, when the ripple filtering capacitor is not connected to
the load, the idealized unloaded output is supposed to be 0V during the charge cycle and 100 V during the discharge cycle.

![Parallel charge-series discharge graph](image)

Figure 33 - Unfiltered Output of Parallel Charge Circuit

It is evident that the unfiltered output (Figure 33) that was obtained closely follows the idealized condition. When the load capacitor was connected, a consistent output voltage of 96.05 V was obtained (Figure 34). This particular design is clearly much more efficient as compared to the previous one.

![Filtered output graph](image)

Figure 34 - Filtered Output of Parallel Charge Circuit
It should be borne in mind that the ideal output is 100 V for the unloaded condition i.e. open circuit across output. In reality, the capacitors discharge via the oscilloscope probes, which are known to have an impedance of 10Mohm. The following table compares the output voltages across various loads connected to the independent charge circuit and the parallel charge circuit. The load resistance shown takes into account the impedance of the probes.

Table 2 - Output Comparison between Independent and Parallel Charge Circuit

<table>
<thead>
<tr>
<th>Load resistance</th>
<th>$V_{OUT}$ Independent charge</th>
<th>$V_{OUT}$ Parallel charge</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MΩ</td>
<td>82 V</td>
<td>96 V</td>
</tr>
<tr>
<td>6.875 MΩ</td>
<td>76 V</td>
<td>93.5 V</td>
</tr>
<tr>
<td>5 MΩ</td>
<td>70V</td>
<td>90.65 V</td>
</tr>
<tr>
<td>0.9 MΩ</td>
<td>30V</td>
<td>60.35V</td>
</tr>
</tbody>
</table>

The variation in output voltage with load is expected. As the load resistance is lowered, the output current increases. This means that more charge is being drained away from the capacitors. It has been explained earlier that once steady state condition of switched capacitor converter is reached, only as much charge needs to be pumped as is lost from the capacitors on every switch cycle. Since more charge needs to be pumped with lowered load resistance, the efficiency of the converter reduces. Furthermore, the periodic charge/discharge causes the capacitor voltages to have an AC ripple component. Energy
is lost on the parasitic elements (capacitor ESR and switch on-resistances) during each charge transfer to or from a capacitor. The energy losses increase with increase in the ac component of voltages.

### 3.3 High Frequency Synchronized Triggering

The test bench developed earlier was successful in converting a 5V input to nearly 100 V ideal output. However the same synchronization logic used in the test bench cannot be used in the final converter design. This is because close inspection of the circuit reveals that the two triggering pulses need a very high degree of synchronization, especially at high frequencies. Even the shortest overlap of the ON times of the two signals will close switches in phase 1 and 2 simultaneously thus shorting the battery across itself, burning it out. The figure below shows the required pulses of the two phases.

Figure 35 - Synchronization Pulses Required for High Voltage Converter
There is a minimum lag time that must be maintained between the high states of the two pulses in order to ensure reliable working of the circuit. This is especially important at high frequency where gate delays become a prominent fraction of the pulse time period. In order to achieve a reliable lag time, the pulse generation needs to be precisely programmed. This was achieved using a Complex Programmable Logic Device (CPLD).

A CPLD is a combination of a fully programmable AND/OR array and a bank of macrocells. The AND/OR array is reprogrammable and can perform a multitude of logic functions. Macrocells are functional blocks that perform combinatorial or sequential logic, and also have the added flexibility for true or complement, along with varied feedback paths. CPLD’s are characterized by an architecture offering high speed, predictable timing, and simple software interface.

The CPLD used for this purpose was XCR 3064XL Coolrunner XPLA3 CPLD from the Xilinx Corporation. It is a low power 3.3V CPLD and can function at
frequencies up to 192 MHz. This CPLD features 64 macrocells and 1500 usable gates, interfaced with 36 I/O pins which are more than enough for the implemented logic.

In order to program the CPLD, the XCRP development board from Digilent Inc was used. This development board can be directly connected to a computer via a parallel port for programming purposes. As seen from the photograph below, it has two seven-segment displays, four de-bounced buttons, eight slide switches, eight LEDs, and also a 40-pin expansion connector. The clock frequency can be varied using an on board rheostat. These features are helpful as they enable visual verification of the logic by feeding the synchronization pulses to the LED’s at low frequency. The logic pulses can be extended to another breadboard via the 40-pin connector.

Figure 37 - DXCRP Development Board
3.3.1 Tunability Logic

Due to the custom programming capabilities obtained by using the CPLD, logic was developed to enable tunability of the high voltage converter. This meant that the user could choose between four different voltage output levels for the same input.

![Tunable High Voltage Converter Diagram](image)

**Figure 38 - Tunable High Voltage Converter**

The circuit remained the same as before with only a few switches added to the circuit. The circuit diagram above explains the tunability logic. Switches 3, 4 and 5 are attached to different stages of the counter. Only one of these tuning switches is closed at any one time. Thus, the number of capacitor stages connected to the load can be controlled, providing variability of the converter output. The actual circuit that was built to test the high frequency CPLD controlled operation, had 20 capacitors connected according to the same topology as the parallel charge circuit. Four tuning switches were added to the
topology which connected the load to 5, 10, 15 and 20 stages respectively. Thus, the user can set the idealized voltage conversion ratio to 5, 10, 15 or 20.

### 3.3.2 Configuring the CPLD

The CPLD was programmed using VHDL. The code was compiled and transferred to the CPLD via the Xilinx design software suite, ISE 6.2i. The CPLD has a non-volatile memory providing permanent storage of designs. ISE (Integrated Software Environment) contains a VHDL compiler, using which program is compiled and then verified for functionality. Using another tool of the same software (Xilinx PACE), package pins of the CPLD are assigned to various inputs and outputs used in the VHDL code. The program is then downloaded onto the CPLD and the logic device functions instantly as per the program.

The XPLA3 board has various components on the board (LED’s, switches etc.) already connected to different pins of the CPLD. These pins are also connected to different terminals of the 40-pin connector. The following table gives us the connection between various pins and board components.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BTN1</td>
<td>12</td>
<td>SW8</td>
<td>23</td>
<td>VCC</td>
<td>34</td>
<td>LED7</td>
</tr>
<tr>
<td>2</td>
<td>MCLK</td>
<td>13</td>
<td>TMS</td>
<td>24</td>
<td>AF</td>
<td>35</td>
<td>VCC</td>
</tr>
<tr>
<td>3</td>
<td>VCC</td>
<td>14</td>
<td>SW7</td>
<td>25</td>
<td>AE</td>
<td>36</td>
<td>LED5</td>
</tr>
<tr>
<td>4</td>
<td>BTN4</td>
<td>15</td>
<td>VCC</td>
<td>26</td>
<td>AD</td>
<td>37</td>
<td>LED4</td>
</tr>
<tr>
<td>5</td>
<td>SW1</td>
<td>16</td>
<td>SW6</td>
<td>27</td>
<td>AC</td>
<td>38</td>
<td>TDO</td>
</tr>
<tr>
<td>6</td>
<td>SW2</td>
<td>17</td>
<td>SW5</td>
<td>28</td>
<td>AB</td>
<td>39</td>
<td>LED3</td>
</tr>
<tr>
<td>7</td>
<td>TDI</td>
<td>18</td>
<td>CAT1</td>
<td>29</td>
<td>AA</td>
<td>40</td>
<td>LED2</td>
</tr>
<tr>
<td>8</td>
<td>SW3</td>
<td>19</td>
<td>CAT2</td>
<td>30</td>
<td>GND</td>
<td>41</td>
<td>LED1</td>
</tr>
<tr>
<td>9</td>
<td>SW4</td>
<td>20</td>
<td>LED9</td>
<td>31</td>
<td>LED8</td>
<td>42</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>PORTEN</td>
<td>21</td>
<td>AG</td>
<td>32</td>
<td>TCK</td>
<td>43</td>
<td>BTN3</td>
</tr>
<tr>
<td>11</td>
<td>IO1</td>
<td>22</td>
<td>GND</td>
<td>33</td>
<td>LED6</td>
<td>44</td>
<td>BNT2</td>
</tr>
</tbody>
</table>

Table 3 - Digilab XCRP Board CPLD Pinout
The two synchronized output signals were attached to pins 40 and 41, i.e. LED 2 and LED 1 respectively. Thus, by the alternate glowing of the LEDs, the program could be visually verified too. The toggle switches SW1 and SW2 on the board were chosen to behave as the binary input to choose the voltage conversion ratio. The following switch assignment was used.

Table 4 - Output Voltage Ratio Settings

<table>
<thead>
<tr>
<th>SW1 POSITION</th>
<th>SW2 POSITION</th>
<th>OUTPUT VOLTAGE RATIO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>15</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>20</td>
</tr>
</tbody>
</table>

Thus the two toggle switches, SW1 and SW2 were used to demultiplex the load position via the four tuning switches explained earlier. Thus four independent outputs from the CPLD controlled the tuning switches. These four outputs were tied to LED’s 5 through 8.

All the I/O pins of the CPLD are also connected to the 40 pin connector via which logic was extended onto another breadboard. The following table gives the pinout connections of various board components the 40 pin parallel connector.
As per the above table, pins 4 and 6 of the connector provided the synchronization pulses and pins 22, 24, 26 and 28 controlled the four tuning switches.

### 3.3.3 VHDL Program

The VHDL program written to implement the CPLD based control is given in the appendix. The logic used is as follows. The VHDL output signals ‘ch’ and ‘disch’ are the two synchronization pulses. At every rising edge of the clock pulse, a VHDL signal ‘wcount’ is incremented. The value of ‘wcount’ determines the value of ‘ch’ and ‘disch’. While ‘wcount’ increments from 0 to 19, ‘disch’ is kept at high while ‘ch’ is low. When ‘wcount’ is exactly 20, both the outputs are kept low. From values 21 to 38 ‘disch’ is kept low while ‘ch’ is kept high. When the value of ‘wcount’ is 39, both the clock pulses are again low. When its value goes above 39, it is reset back to 0. Thus, during one clock cycle between state transitions, both outputs are low, thus setting the lag time between toggling of switches. The tuning process is simple 2:4 demultiplexing logic. ‘sel’ is the

---

**Table 5 - Digilent XCRP Board Expansion Connector Pinout**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>11</td>
<td>SW4</td>
<td>21</td>
<td>AD</td>
<td>31</td>
<td>NC</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>12</td>
<td>LED5</td>
<td>22</td>
<td>BTN2</td>
<td>32</td>
<td>SW5</td>
</tr>
<tr>
<td>3</td>
<td>VCC</td>
<td>13</td>
<td>LED9</td>
<td>23</td>
<td>AC</td>
<td>33</td>
<td>NC</td>
</tr>
<tr>
<td>4</td>
<td>LED1</td>
<td>14</td>
<td>LED6</td>
<td>24</td>
<td>BTN3</td>
<td>34</td>
<td>SW6</td>
</tr>
<tr>
<td>5</td>
<td>SW1</td>
<td>15</td>
<td>AG</td>
<td>25</td>
<td>AB</td>
<td>35</td>
<td>NC</td>
</tr>
<tr>
<td>6</td>
<td>LED2</td>
<td>16</td>
<td>LED7</td>
<td>26</td>
<td>BTN4</td>
<td>36</td>
<td>SW7</td>
</tr>
<tr>
<td>7</td>
<td>SW2</td>
<td>17</td>
<td>AF</td>
<td>27</td>
<td>AA</td>
<td>37</td>
<td>NC</td>
</tr>
<tr>
<td>8</td>
<td>LED3</td>
<td>18</td>
<td>LED8</td>
<td>28</td>
<td>CAT1</td>
<td>38</td>
<td>SW8</td>
</tr>
<tr>
<td>9</td>
<td>SW3</td>
<td>19</td>
<td>AE</td>
<td>29</td>
<td>NC</td>
<td>39</td>
<td>NC</td>
</tr>
<tr>
<td>10</td>
<td>LED4</td>
<td>20</td>
<td>BTN1</td>
<td>30</td>
<td>CAT2</td>
<td>40</td>
<td>IO1</td>
</tr>
</tbody>
</table>
two bit control vector while ‘sw’ is the four bit output vector, only one of whose bits is set at any time.

3.3.4 Testing

Rough verification of the VHDL program can be done at very low frequency by visual inspection of LED switching behavior. This however, confirms only the logical correctness of the program and cannot be accepted as a reliable method of CPLD validation. Thus, high frequency implementation of a voltage converter using the CPLD is essential for complete validation. Again, such a design can serve as the test bench for the high frequency switches. Unfortunately, mechanical switches like relays cannot be used in this prototype due to their low switching speed. The only switches that can function at such high frequencies are FET based switches. As stated earlier, though these switches can simulate the high switching speeds of micromachined switches, they have a low current carrying capability. Nevertheless, the magnification of even a very low input voltage, at high frequencies is enough to validate the CPLD functionality and the tunability logic.

The FET switch that was used for this purpose is the Quadruple bilateral switch SN74HC4066. It is a 14 pin IC which consists of four silicon-gate CMOS analog switches designed to handle analog as well as digital signals which can be transmitted bidirectionally. Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.
The following photograph shows the breadboard circuit built to test the CPLD. Outputs were taken at all different configurations of the tuning switches. Four different output levels were obtained as expected.

Figure 39- Pin Diagram of CMOS Based Quadruple Switch SN74HC4066

Figure 40 - CMOS Switch Based High Voltage Converter
The maximum input voltage that this circuit could handle is 0.3V. As the number of stages used increases, the maximum input voltage handling capability decreases. This is because the discharge current increases as the number of capacitors increase. As voltage converters designed using customized FET switches have not been able to generate voltages beyond few tens of volts, this voltage limitation of the general purpose FET switches is as expected.

The output below shows the synchronization pulses obtained from the CPLD. Note the time lag between the state transitions of each pulse. The next four graphs show the outputs of the circuit tuned at all four different output levels for the same input of 0.3V. The four levels are graded level 1 to 4 from lowest to highest voltage conversion ratio.

![Synchronization pulses](image)

**Figure 41 - Synchronization Output Pulses from the CPLD**
Figure 42 - Converter Output with Load Connected Across 20 Capacitors

Figure 43 - Converter Output with Load Connected Across 15 Capacitors
Figure 44 - Converter Output with Load Connected Across 10 Capacitors

Figure 45 - Converter Output with Load Connected Across 5 Capacitors
The four outputs shown above clearly prove the successful implementation of the tunability logic. Note the similar output waveform obtained in the relay based high voltage converter.

The significance of these results goes beyond the aim of establishing a high frequency switch controller. It shows that the flexibility obtained via programmable logic devices can be used to one’s benefit in various ways. Complex programs can be used alter the functioning of converters as per real time conditional variations. An ‘intelligent’ feedback system that goes beyond old generation analog control can consequently be easily implemented.
4.1 Micromachined Vs. Commercial Capacitors

Capacitor technology has made tremendous progress since their invention. The capacitance to volume ratio of today’s capacitors has increased by orders of magnitudes in the last few decades; and alternate methods are being developed everyday for pushing the limit even further. Micromachined capacitors were first proposed less than a decade back. Since then however, not much research has gone into their fabrication due to their limited applicability in industry. Nevertheless, they offer multiple advantages over their commercially available counterparts, which cannot be ignored. Recent emergence of MEMS as a mainstream technology demands due attention be given to micromachined capacitors. Lehmann et. al. [10] have investigated the advantages of micromachined capacitors over conventional ones. Some of their findings are reported here to establish the clear benefit of using micromachined capacitors.

High value capacitors that are used in industry today commonly employ high dielectric constant materials such as polystyrene or silicon dioxide. However they have the disadvantage of having low surface to volume ratios of electrodes. One might increase the electrode area by etching or sintering techniques, but then has to deal with anodically formed oxides. This is the case in aluminum or tantalum capacitors. Ceramic
dielectrics use alternate dielectric materials to solve this problem. Unfortunately, these materials offer a strong temperature and electric-field dependence of the dielectric constant. The thickness of all state of the art non-anodic capacitor dielectrics is limited by the manufacturing process to about 1 micron. This limits the minimum voltage to be about 25 V. For thinner dielectrics anodic oxides are used. Unfortunately these oxides show a diode-like behavior which leads to destruction of the capacitor if reverse bias is applied.

Micromachined capacitors offer an economical solution to all of the problems mentioned above as well as provide certain other superior properties. They commonly use Oxide-Nitride-Oxide stack dielectric which exhibits non-diode-like operation ranging from very low voltage to above 100 V. They also show remarkable invariability of the capacitance under variation of bias, temperature, frequency, and time of operation. Furthermore, they show negligible voltage dependence of the capacitance. Together with the tantalum capacitor, the micromachined capacitor has the smallest volume for the given capacitance. However, the electric series resistance (ESR) of the tantalum capacitor is very high, thus making it void of any real resonance. Thus the micromachined capacitor has the highest resonance frequency.

The table below (adapted from Lehmann et. al. [10]), compares various commercial capacitors with MEMS based capacitor. Electrolytic capacitor with dielectrics Al₂O₃ or Ta₂O₅ are considered. Polymer based capacitors with dielectrics polyethylene terephthalate (PET) or polystyrene (PS), and ceramic capacitors with a TiO₂ (COG) or BaTiO₃ (Z5U) dielectric layer, are compared with a micromachined capacitor with ONO dielectric.
Table 6 - Comparison of Various Capacitor Types

<table>
<thead>
<tr>
<th>TYPE</th>
<th>ELECTROLYTE</th>
<th>POLYMER</th>
<th>CERAMIC</th>
<th>MEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric</td>
<td>Al₂O₃</td>
<td>PET</td>
<td>COG</td>
<td>Z5U</td>
</tr>
<tr>
<td></td>
<td>Ta₂O₅</td>
<td>PS</td>
<td></td>
<td>ONO</td>
</tr>
<tr>
<td>ε</td>
<td>10</td>
<td>27</td>
<td>3.2</td>
<td>2.6</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>10000</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>Voltage Range (V)</td>
<td>3-700 Polarized</td>
<td>3-125 Polarized</td>
<td>50-1500</td>
<td>50-200</td>
</tr>
<tr>
<td></td>
<td>50-7000</td>
<td>25-100</td>
<td>3-100</td>
<td></td>
</tr>
<tr>
<td>Capcitance Range</td>
<td>0.1 μF-1F</td>
<td>0.1-1000μF</td>
<td>1nF-10μF</td>
<td>2pF-500nF</td>
</tr>
<tr>
<td>Specific Capacitance (μF V mm⁻³)</td>
<td>8</td>
<td>5</td>
<td>0.1</td>
<td>0.003</td>
</tr>
<tr>
<td></td>
<td>0.03</td>
<td>1</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Temperature Range (°C)</td>
<td>-55/+105</td>
<td>-55/+125</td>
<td>-55/+100</td>
<td>-55/70</td>
</tr>
<tr>
<td></td>
<td>-55/-125</td>
<td>-55/+125</td>
<td>-55/125</td>
<td>-55/200</td>
</tr>
<tr>
<td>∆C/C(U) (%)</td>
<td>4</td>
<td>-1</td>
<td>&lt;0.01</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td></td>
<td>&lt;0.1</td>
<td>&lt;0.1</td>
<td>-80</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td>∆C/C(T) (%) (K⁻¹)</td>
<td>+10⁻³</td>
<td>+10⁻³</td>
<td>+5x10⁻⁴</td>
<td>-10⁻⁴</td>
</tr>
<tr>
<td></td>
<td>+3x10⁻⁴</td>
<td>±10⁻²</td>
<td>±3x10⁻⁵</td>
<td>±10⁻²</td>
</tr>
<tr>
<td>∆C/C(f) (%)</td>
<td>20</td>
<td>-8</td>
<td>-4</td>
<td>-0.1</td>
</tr>
<tr>
<td></td>
<td>&lt;0.1</td>
<td>&lt;0.1</td>
<td>-5</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td>∆C/C(t) (%)</td>
<td>±5</td>
<td>+5/-10</td>
<td>±3</td>
<td>&lt;0.2</td>
</tr>
<tr>
<td></td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>-15</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td>tan δ (%)</td>
<td>5 x 10⁻²</td>
<td>5 x 10⁻²</td>
<td>8 x 10⁻⁴</td>
<td>&lt;10⁻⁴</td>
</tr>
<tr>
<td></td>
<td>&lt;10⁻³</td>
<td>3 x 10⁻²</td>
<td>&lt;10⁻⁴</td>
<td></td>
</tr>
<tr>
<td>ESR (m-ohm)</td>
<td>-</td>
<td>~1</td>
<td>70</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
<td>70</td>
<td>60</td>
</tr>
<tr>
<td>Riso(Tₘin/Tₘax) (Mohm)</td>
<td>-</td>
<td>10³/10⁴</td>
<td>10³/10⁴</td>
<td>-</td>
</tr>
<tr>
<td>fres (MHz)</td>
<td>-</td>
<td>&lt;1</td>
<td>7</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
<td>12</td>
<td>15</td>
</tr>
</tbody>
</table>

a ∆C/C(U), a scan from zero bias to the operating voltage; ∆C/C(f), compares the capacitance at 100kHz with the d.c. capacitance; ∆C/C(t), a time interval of 1000 h; tan δ determined at 1 kHz. Since a comparison of the electrical series resistance (ESR), the isolation resistance (Riso), and the resonance frequency (fres) only makes sense for devices of the same capacitance and comparable dimensions these values refer to 100 nF chip capacitors.

Adapted from Lehmann et. al. [10]
4.2 Micromachined Capacitor Structure

Micromachined capacitors can be broadly classified into two categories –

- Tunable capacitors – These allow a continuous variation of the capacitor value over a range of values. Change in capacitance is effected by varying the gap between two metal layers forming the capacitor plates via electrostatic actuation. These capacitors generally find application in RF circuits.

- Fixed capacitors – These have a fixed value of capacitance. They have no moving parts and can be used for most general purpose applications.

Since this particular project needs fixed capacitors, this discussion shall be limited to this type of MEMS capacitors only.

The basic structure of a micromachined capacitor is very simple. Very low resistivity silicon substrate acts as one plate of the capacitor. A dielectric is deposited (or grown) over the silicon. This may be either a single layer dielectric, or a combination of materials stacked together to form a composite dielectric. It is then topped with a conducting layer of metal or polysilicon, which acts as the other plate of the capacitor. Polysilicon is generally preferred due to its conformality over irregular surfaces. In case doped polysilicon is not available, undoped polysilicon is deposited and then diffused with an impurity to lower its resistivity.

The specific capacitance of the capacitor can be increased multifold by taking advantage of the fact that all of the structural layers can be conformally coated over an irregular silicon surface. Very deep holes or trenches can be etched into silicon to increase the effective surface area of the capacitor. The visible surface area of the
electrodes remains small while the capacitance increases exponentially. This is illustrated in the figure below.

Figure 46 - Increased Effective Surface Area of Electrode via Micromachining

The ratio of area increase is larger if the etched holes have smaller pitch and greater depth. There are two common methods of micromachining holes in silicon – Porous silicon and DRIE processing. Both approaches were investigated in this project.

An oxide-nitride-oxide (referred to as ONO hence) stack is used as the dielectric as opposed to only oxide. There are multiple advantages of using a composite dielectric:

- In trenched structures, electric field is concentrated around corners and edges. This field enhancement coupled with oxide thinning at the corners, results in increased current injection thereby reducing the breakdown times. The ONO dielectric locally traps electrons even at very high electric fields. The trapped electrons reduce electric field at the edges and therefore smooth out the current flow across the entire area of the wafer.
This increases the breakdown voltage for the trenched ONO capacitor as compared to the trenched oxide capacitor.

- Reliability of the ONO capacitor is much higher. Breakdown of a thin film capacitor is initiated by the weakest spot in the dielectric; a thickness fluctuation or interface roughness. Having multiple layers reduces this defect density by several orders of magnitude. Defect related as well as intrinsic early failure occurrences are massively reduced in the ONO capacitor [9].

- The lifetime of the ONO capacitor is five to six orders of magnitude higher than the oxide capacitor. Hiergiest et. al. [9] have extrapolated a lifetime of ten years for an oxide capacitor (13.5 nm dielectric) and that of one million years for a similar ONO capacitor.

- Nitride has a higher dielectric constant than oxide. Thus the use of a thick nitride increases the specific capacitance as compared to a similar thickness oxide-only dielectric.

- The first thermal oxide reduces the stress between the silicon substrate and the nitride layer. Similarly the second oxide layer reduces the stress between the nitride and top polysilicon layer.

- The polysilicon layer might need to be doped externally (as in this case), the nitride serves as a diffusion barrier (some unwanted dopant diffusion might be expected in the top oxide).
4.3 Porous Silicon

Porous silicon is a material that is formed by anodic dissolution of silicon in HF solutions. The formation of porous silicon was first reported in the late 1950s in studies on electropolishing of silicon. After the discovery of luminescence in 1990 numerous investigations have been undertaken. They have revealed that porous silicon has extremely rich morphological features with properties that are very different from those of silicon and the formation process of porous silicon is a very complex function of many factors such as HF concentration, type of silicon, current density, and illumination intensity.

Porous silicon can either be formed by anodization in HF-containing solution under an anodic bias or by an electroless process. The formation condition can be illustrated by an I-V curve as shown in the figure below. At small anodic overpotentials the current increases exponentially with the electrode potential. As the potential is increased, the current exhibits a peak and then remains at a relatively constant value. Porous silicon forms in the exponential region but not at potentials higher than that corresponding to the current peak. Electrochemical polishing occurs in this region. At potentials above the exponential region and below the potential of the current peak, porous silicon formation also occurs, but the porous silicon layer does not cover the sample surface completely. The surface coverage of porous silicon decreases as the potential approaches the peak value. Hydrogen evolution simultaneously occurs in the exponential region and its rate decreases with potential and almost ceases above the peak value.
The average dimensions of porous silicon structures cover four orders of magnitude from a few nanometers to tens of micrometers. Such structures can be classified according to size in three different regimes. The microporous regime consists of average dimensions below 2nm. The mesoporous regime shows average dimensions from 2nm to 50nm, and the macroporous regime are above 50nm. This research is concerned with fabrication of pores about 10 microns wide. Thus the discussion here shall be limited to porous silicon etching in the macroporous regime.

Porous silicon formation is a self-adjusting phenomenon. At a specific current density silicon dissolution process in the electrolyte changes from charge transfer limited, to mass transfer limited, thus forming pores. Macropore formation in silicon electrodes is characterized by a depletion of porous region due to space charge effects and a constant
current density at the pore tips indicating a steady state condition between charge transfer and mass transfer. A significant space charge region is only present in n-type semiconductors. Consequently macropore formation in aqueous electrolytes is only observed for n-type silicon electrodes. During dissolution, electrons recombine with the holes present in the surface of the electrode. Energy of 1.1ev higher than the recombination energy is required to start the etching process. The dissolution of holes in HF is restricted by the anodized n-type silicon substrate, since holes are the minority carriers. Hole generation can be enhanced if the substrate is illuminated, thus promoting the dissolution reaction. Illumination from the back-side is found to be superior to front-side illumination, because in the latter case carriers are generated in the pore walls, which leads to further dissolution in this region.

Figure 48 - Porous Silicon Setup
4.3.1 Macroporous Silicon Equations

Lehmann [12] has outlined much of the chemistry that takes place during macroporous silicon formation. For low current densities, the silicon dissolution is limited by charge supply from the electrode and is characterized by an ohmic slope of the I-V curve. For high current densities the reaction is limited by ionic diffusion in the electrolyte near the electrode surface, as indicated by a smaller slope of the I-V curve. For a flat silicon anode the transition from the charge-supply-limited to the ionic-diffusion limited case is characterized by a specific current density, $J_{PS}$. At this current density the dissolution morphology changes fundamentally. For $J>J_{PS}$, holes accumulate at the electrode surface and HF is depleted at the electrode surface. Thus the dissolution is limited by the ionic transfer rate, which is lower in depressions or pits, resulting in electropolishing of the surface. For $J<J_{PS}$, the location dependence of ionic transfer rate is reversed. Thus holes are depleted at the electrode and HF accumulates at the electrode surface. Therefore every depression or pit in the surface initiates pore growth because it focuses the electric field lines of space charge region and thereby enhances the local current density. At $J=J_{PS}$, ionic transfer and charge supply are in a steady state condition.

Lehmann states an Arrhenius-type relationship between $J_{PS}$ (mA cm$^{-2}$) and an activation energy $E_a = 343$ meV. $J_{PS}$ also depends on the concentration of HF (‘c’ wt%) and temperature $T$ (K). The relation is given by the empirical formula –

$$J_{PS} = Cc^{3/2} \exp\left(-\frac{E_a}{kT}\right); \quad \text{where } C = 3300 \text{ mA cm}^{-2}\text{wt.}%^{-3/2}$$
The rate of pore growth can be calculated using the fact that the current density passing through the electrode surface is a measure of the rate of dissolution. Thus, the rate of pore growth \( v \) is calculated by dividing the local current density ‘\( J_{\text{tip}} \)’ at the pore tip by the dissolution valence ‘\( n \)’ (number of charge carriers per dissolved silicon atom), the elementary charge ‘\( e \)’ (1.602 \( \times \) 10\(^{-19} \) C) and the atomic density of silicon, ‘\( N_{\text{Si}} \)’ (5 \( \times \) 10\(^{22} \) cm\(^{-3} \)).

\[
v = \frac{J_{\text{tip}}}{n(-e)N_{\text{Si}}}
\]

In stable condition, at the pore tips \( J_{\text{tip}} = J_{\text{PS}} \). This allows the diameter of the pores to be precisely inferred. All charge transfer occurs via the pore tips and the tip current density is \( J_{\text{PS}} \). Thus the total etching current equals the sum of the cross-sectional areas of all pores, \( A_p \), multiplied by \( J_{\text{PS}} \). At the same time, the total etching current divided by the initial sample surface area \( A_t \) (defined by the sealing ring in the set-up) gives the overall current density \( J \). This allows one to calculate \( A_p \) as,

\[
A_p = A_t \frac{J}{J_{\text{PS}}}
\]

If a homogeneous, orthogonal pattern is used for pore initiation, the spacing \( p \) of pores and the pore diameter \( d \) is same for all pores. Thus \( A_t \) can be replaced by the squared pore spacing \( p^2 \) and \( A_p \) is replaced by cross sectional area of single pore, which can be simply approximated by \( d^2 \).
By substitution one obtains –

\[ d = \rho \left( \frac{J}{J_{PS}} \right)^{1/2} \]

Thus it is seen that all relevant parameters such as location, diameter, depth and growth rate of pores can be controlled by adjusting a few formation parameters such as doping density, applied bias, illumination intensity and HF concentration.

4.3.2 Porous Silicon Fabrication

This research demands macroporous silicon fabrication with pore widths in the range of 5 to 10 microns. It has already been stated the n-type substrate are required for this purpose. To achieve vertical pores without branching <100> silicon is used. The resistivity in ohm-cm should approximately be the square of the required pore size in micron. Hence double side polished 25 ohm-cm, 2” diameter wafers were used for the purpose. The figure below demonstrates the fabrication sequence employed.
Silicon wafers of n-type diffusion, \(<100>\) orientation and 20 – 30 ohm-cm resistivity were used for porous silicon fabrication. First, a wet oxide of 3000 Å thickness is grown to act as a masking layer. Back side lithography is then performed to pattern the contact ring area. This exposes the contact ring area for subsequent n-type diffusion (n-type
diffusion below the electrode ensures an ohmic contact. The oxide on the back side is then stripped via a BOE etch. Next, lithography is done on the front side to define pores. The exposed oxide is etched using BOE. After the photoresist is stripped, KOH etching is performed to form pore tips. The exposed silicon etched in KOH (90 C, 15 min.) to etch inverted pyramids which act as pore initiation sites. A jig is used to protect the back side. Metal deposition is done on backside. Ti (500 Å) is evaporated first to act as the adhesion layer and Al (3000 Å) is evaporated over it to form the backside metal electrode. Lithography is then performed on the backside, and metal is patterned to form the contact ring. The metal ring is the same area in which phosphorus was earlier diffused.

The wafer now is ready for porous silicon etching. The wafer is placed in the porous silicon etching jig such that the backside is illuminated via the lamp. The etching solution is poured into the jig and electrodes are connected in place. The etching is controlled via a labview program into which various parameters like HF concentration, fill factor, etching time, temperature are entered.

The labview program controls the etching by varying the etch current. The required etch current is calculated according to the entered parameters. The lamp intensity is varied till the actual etch current follows the calculated value (Changing the lamp intensity varies the photocurrent and hence the total current through the sample).
4.3.3 Results

All wafers were patterned using a mask containing 6 micron wide pore openings with a pitch of 30 microns. Various wafers were initially etched under 2.5 V bias, with 2% HF solution. The etch results had some favorable aspects; namely continuous and stable etching was observed at a desirable etch rate – 170 micron depth in 24hrs. However some persistent problems plagued the fabrication. The pore dimensions were highly random. Also the cross-section of the pores was star shaped (as opposed to the ideal square pore). Finally, the pore diameter was very huge at around 15 micron, thus resulting in a very thin pore wall.
Figure 51 - Initial Attempts at Porous Silicon Fabrication

The figures above show the SEM images of the cross section of the initially fabricated porous silicon wafers. From the figures it is obvious that the pores obtained were highly
unsatisfactory. Therefore, various improvements were made in the process. Firstly, the setup was fine-tuned to facilitate even more stable etching. A potentiometer was placed in series with the voltage source to enable fine changes in series resistance in order to account for small differences in electrolyte conductivity from run to run. This change in series resistance was recorded in the labview program for appropriate formula adjustments. The most important improvement however, was a change in the etch chemistry. Ethanol was added to the etch solution to form straighter pores. Etching with pure HF solution causes hydrogen masking to take place. This causes uneven etching at the pore bottom, thus resulting in irregular etching. Ethanol supposedly removes this problem. The etch solution was prepared with the following volume ratios - 20.4 ml of 49% HF, 20 ml of Ethanol solution, 459.6 ml of DI water. This ratio results in 2 % wt. solution of HF. Figures below show the pores obtained after a 24 hour etch implemented with these variations.
As seen from the SEM images, exceptional results were obtained. The pores were extremely uniform with respect to all dimensions. They had an excellent depth of 200 microns. Pore sizes were much smaller (9 to 10 microns) as compared to previous
attempts. Also, the cross-sections were square shaped as desired. An important feature of these pores was that the pores did not seem to near pinch-off at the bottom, i.e. the pores walls were straight for the entire depth of the pore. This result is highly significant as it shows that the aspect ratios achieved were limited by the thickness of the wafer (250 micron) and not by process restrictions. Thus, one can practically achieve even deeper pores with this process.

Further tests were done using lower resistivity 500 micron thick wafers. This proved the repeatability of the results obtained from prior successful experiments. Smaller pore widths of 8 to 9 microns were achieved. The pore depths were same at around 200 microns. Extremely uniform features were obtained as before.
4.4 DRIE Processing

Wafers were also processed using Deep Reactive Ion Etching (DRIE). DRIE is a special subclass of the more generic process Reactive Ion Etching (RIE) – a dry etching process.
technique. In RIE the substrate is placed inside a reactor in which several gases are introduced. A plasma is generated in the gas mixture using an RF power source which breaks the gas molecules into ions. Etching takes place via a chemical as well as a physical process. In the chemical part of etching, the ions are accelerated towards the material being etched and react at the surface, forming another gaseous material. The physical part of etching is similar in nature to the sputtering deposition process. If the ions have high enough energy, they can knock atoms out of the material being etched without a chemical reaction. Balancing the chemical and physical etching is a very complex task due to the various parameters in question. However, by changing the balance it is possible to influence the anisotropy of the etching, since the chemical part is isotropic and the physical part is highly anisotropic. Various combinations can form sidewalls that have shapes ranging from rounded to vertical. A schematic of a typical reactive ion etching system is shown in the figure below.

![Figure 54 - Typical Parallel-Plate Reactive Ion Etching System [13]](image-url)
The DRIE process is similar to the process mentioned above, with slight modifications. The primary technology is based on the so-called "Bosch process", named after the German company Robert Bosch which filed the original patent. Two different gas compositions – C$_4$F$_8$ and SF$_6$ are alternated in the reactor. C$_4$F$_8$ composition deposits a polymer on the surface of the substrate, while the SF$_6$ composition etches the substrate. The polymer is immediately sputtered away by the physical nature of the etching, but only on the horizontal surfaces and not the sidewalls. This is due to the directional nature of the accelerated ions. The polymer dissolves very slowly due to the chemical nature of etching. Hence it builds up on the sidewalls, protecting them from etching.

The DRIE process allows for etch depths of hundreds of microns to be achieved with almost vertical sidewalls (angle 90° +/- 2°). Aspect ratios of up to 50 to 1 can be obtained. Very importantly etching is independent of the crystal orientation, and thus provides a high degree of flexibility in process design. The etch rates observed are 3-4 times higher than wet etching and can be over 10µm/min. The surface roughness of the sidewall can be as low as 10nm, and the homogeneity of the etch depth less than +/-3% (on a 4" wafer). However, there always exists a compromise between the etch rate and the surface roughness. Also, the process exhibits high loading effects. A large etched silicon area lowers the etch rate and the inhomogeneity can increase to above +/- 10%.
4.4.1 DRIE Based Fabrication

All DRIE based fabrication was done on 4” <100> wafers. A 2 micron oxide was first deposited via PECVD. Patterning was done to open etch windows of 5 micron wide squares with 20 micron pitch. Pore depth mainly depends on two parameters - the number of Bosch cycles and the gas pressure during the polymer deposition step. Increasing the number of Bosch cycles relates to longer etching and thus greater etch depths. The gas pressure predominantly controls the side wall angle and thus the aspect ratio of etching. A side wall angle of less than 90° would result in earlier pinch-off or closing of pores.

The first batch of wafers was placed for DRIE etching for a 200 bosch cycle process. The gas pressure was kept at 24 mTorr. An etch depth of only 70 to 75 micron was obtained. Thus etching was then tried using a 400 bosch cycle process using the same gas pressure. This time too the etch depths were similar (Figure 55), showing that etch depth for this particular gas pressure had been reached.
Figure 55 - Pores Obtained in Initial Attempts at DRIE Processing
The figures above show that the pores obtained were again only 75 microns deep. The pores are clearly pinching off beyond this depth. For larger capacitance, greater etch depths are naturally required. Therefore the need was felt to obtain larger depths than those obtained in the first few attempt. It was observed that areas on the wafer with very large openings of about 1mm (text on the mask used for reference), were etched to 400 microns. Thus, it was realized that the problem was with the etching parameters and not with the number of cycles. The gas pressures had to be investigated as a variable to obtain high aspect ratios on small features. When the gas pressure during the polymer deposition step was changed from 24 mTorr to 22 mTorr, favorable results were obtained. The figure below shows pore depth of around 140 microns obtained using the new recipe.

Figure 56 - 140 micron Deep Pores using DRIE
4.5 Polysilicon Deposition

Polysilicon was deposited on the wafer for the purpose of testing its conformality. As seen in the figures below, it was observed that a uniform and conformal layer was formed on the top of the pores as well as near the pore bottom. Thickness of the layer is approximately 1.2 micron. The sample served to prove the feasibility of polysilicon deposition in deep narrow pores.

![Figure 57 - Conformal Coating of Polysilicon at Top of Pore](image1)

![Figure 58 - Uniformly Thick Coating of Polysilicon over Entire Pore Wall](image2)
4.6 Porous Silicon Vs. DRIE Capacitor Fabrication

Both methods of capacitor fabrication have their own advantages and disadvantages. This is outlined in the table below. It is evident that the choice of process is highly application and resource dependent. The results obtained as a part of this research reveal an added significance in that they corroborate much of the theoretical advantages and limitations of each process.

Figure 59 - Polysilicon Coating near Bottom of Pore
Table 7 - Comparison of Porous Silicon and DRIE Processes

<table>
<thead>
<tr>
<th>POROUS SILICON</th>
<th>DRIE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Economical process.</td>
<td>Gases and equipment is expensive.</td>
</tr>
<tr>
<td>Very high aspect ratios are possible.</td>
<td>Aspect ratios are limited. Maximum</td>
</tr>
<tr>
<td>Thus potentially very high specific capacitance is possible.</td>
<td>attainable specific capacitance is lower than</td>
</tr>
<tr>
<td></td>
<td>porous silicon process.</td>
</tr>
<tr>
<td>No toxic gas hazard.</td>
<td>Gases used are toxic and corrosive.</td>
</tr>
<tr>
<td>Not a very flexible process. Only pores can be etched.</td>
<td>Different kinds of etch topologies (e.g. trenches) apart from pores are possible.</td>
</tr>
<tr>
<td>Pores necessarily occupy entire wafer.</td>
<td>Selective etching is possible in certain areas as per requirement.</td>
</tr>
<tr>
<td>No space for additional features.</td>
<td></td>
</tr>
<tr>
<td>Slow etch rate. Lengthy wafer preparation steps before etch step.</td>
<td>Etch rate up to 8 times faster than porous silicon. Minimal pre-etch fabrication steps.</td>
</tr>
<tr>
<td>Hazardous acids and solvents need to be handled.</td>
<td>Eliminates handling of dangerous acids and solvents.</td>
</tr>
<tr>
<td>Automation is difficult.</td>
<td>Enjoys ease of automation.</td>
</tr>
<tr>
<td>Only n-type &lt;100&gt; silicon can be used.</td>
<td></td>
</tr>
<tr>
<td>Specific resistivity of wafer is required.</td>
<td></td>
</tr>
<tr>
<td>Substrate doping required after etch.</td>
<td>If low resistivity wafer is used, doping step can be avoided.</td>
</tr>
</tbody>
</table>
CHAPTER 5
CAPACITOR BANK FABRICATION

5.1 Introduction

Conventional microcapacitor fabrication techniques follow an array based process which allow for the fabrication of only individual capacitors, to be used separately. When used in a multi-capacitor bank formation, valuable size and time benefits are compromised due to independent packaging and handling requirements of each capacitor. Though fabrication techniques for individual microcapacitors have long since been established, the development of a capacitor bank in silicon has not been done yet. For this purpose, novel fabrication techniques were developed as a part of this research. They enable on-chip integration of numerous microcapacitors, without losing customized configurability of the capacitor bank. The techniques utilize a polyimide to facilitate lithography on a highly contoured surface. A test capacitor bank was fabricated for evaluation, each capacitor on the bank being similar in structure to microfabricated capacitors described in the previous chapter.

Two different types of capacitor bank designs are explored here. The first design developed is that of a series bank of capacitors. Multiple microfabricated capacitors are fabricated in a line such that each capacitor is in series to the adjacent one. This type of design can be used in the Cockcroft-Walton circuit described in Chapter 2. The second design is that of isolated capacitors. Each capacitor is completely isolated
from others. Both plates of the capacitor have separate contact pads. The capacitors can be connected in any configuration desired by wire bonding them accordingly. This is a more generic capacitor bank and can be used in any of the voltage converters.

5.2 Series Capacitor Bank Fabrication

Figure 60 - Series Capacitor Bank Process Flow
The figure above shows the process flow for series bank of capacitors. The fabrication process utilizes very low resistivity substrates to avoid a diffusion step. Any crystal orientation or doping type might be used, since the process uses DRIE which is largely crystal orientation independent. The wafers are next anodically bonded to a quartz substrate. PECVD oxide (3 micron thick) is then deposited to act as a masking layer. Lithography is performed in order to pattern holes in the oxide. The exposed oxide is then etched using RIE (87 minute etch step). Next, holes are etched in silicon using DRIE process. The same parameters as outlined in the previous chapter are used (400 Bosch cycle; 22 mTorr gas pressure during polymer deposition). Any residual photoresist is then removed in acetone (figure ‘a’). The wafer is then oxidized to grow a 2 micron thick wet oxide. Isolation regions are then patterned via lithography and a subsequent 70 minute RIE etch (figure ‘b’). Isolation trenches are then etched through the wafer using DRIE (700 Bosch cycles; 24 mTorr gas pressure). This isolates the capacitor blocks (figure ‘c’). The residual photoresist is removed and the masking oxide is etched using 6:1 BOE (30 minute etch).

The skeleton of the capacitor bank is now ready and dielectric layer are deposited next. First, a dry oxide film of 10nm is grown. Next, LPCVD Nitride (15 nm) is deposited, followed by a 10nm LPCVD oxide deposition. Over this, a 5000 Å polysilicon film is deposited using LPCVD. Doped Low Temperature Oxide (PSG – 1 micron) is deposited and the wafer is annealed at 1100 °C for 1 hour. This step diffuses the phosphorus into the polysilicon layer reducing its resistivity. The PSG is then removed via a 15 minute etch in 6:1 BOE (figure ‘d’).
The next step primes the wafer surface for the subsequent lithography. Since the surface of the wafer is highly contoured, direct lithography is not possible. Thus PiRL is spun onto the wafer to create a planar surface over which photoresist can be spun. Three to four spins of PiRL are needed to reach sufficient planarity. PiRL is baked at 120 °C for 90 seconds (figure ‘e’). Lithography is then performed over the PiRL layer in order to pattern openings in polysilicon. Since PiRL dissolves in developer, it gets patterned along with photoresist, thus exposing the polysilicon layer, forming the contact pad openings. A 10 second over-develop ensures a reliable etch of the entire PiRL layer (figure ‘f’). The polysilicon is then etched for 2 minutes using the non-Bosch process in DRIE system. This etch step is timed to purposely over-etch the polysilicon. This ensures reliable isolation of the polysilicon layer and the silicon substrate. The ONO stack is etched next in RIE in a single 3 minute etch step; the recipe for oxide and nitride etch being the same (figure ‘g’). Any residual photoresist is removed with acetone and then PiRL is removed in developer.

PiRL is then spun again 3 to 4 times. This again is to prime the wafer for the next lithography. After baking the PiRL, lithography is performed as earlier. Bond pads and dicing lines are patterned in this step. Each adjacent set of capacitors has a bond pad either on polysilicon(top plate of capacitor) or on exposed silicon (bottom plate of capacitor). Titanium (500 Å) and Gold (3000 Å) are sputtered next (figure ‘h’). Lift-off is then done in developer MF-319.

The capacitors blocks are then diced along the metal dicing lines. Finally, wire bonding is done to connect the capacitors in the required fashion (figure ‘i’). It can be seen from the final structure that each capacitor is joined to one adjacent capacitor via the
common substrate and to the other adjacent via the polysilicon. Therefore, each capacitor has the bottom plate common to one capacitor and the top plate common to the other. Hence they are in a series configuration.

5.3 Isolated Capacitor Bank Fabrication

The process flow for the isolated capacitor bank is similar to that of the series capacitor bank except for a few variations. Unlike the previous process flow, one cannot deposit the ONO and polysilicon layer after the isolation trench formation, since adjacent capacitors are not connected at all. Also, trench isolation is present between any two capacitors (unlike the previous case where trench isolation was present after every alternate capacitor). Each capacitor has a metal contact pad on its polysilicon layer and also on silicon substrate.

All the processing parameters are the same as in the previous process unless otherwise mentioned. The processing is done on low resistivity 4” silicon wafers. PECVD oxide of 3 micron thickness is deposited. Trenches are patterned on the oxide using DRIE (400 Bosch cycles; 22 mTorr gas pressure). After stripping the resist the masking oxide removed using a 30 minute 6:1 BOE etch. The first dielectric layer is grown next (10nm dry oxide). LPCVD Nitride (15nm), LPCVD Oxide (10nm) and LPCVD polysilicon (5000 Å) are deposited next. LTO-PSG (1 micron) is deposited and wafer is annealed at 1100 °C for 1 hour. PSG is then removed using a 15 minute 6:1 BOE etch.

Next, a glass wafer (Pyrex 7740) is bonded to the substrate using anodic bonding. Quartz is not necessary as no further high temperature steps are left. A 3 micron PECVD oxide is
deposited, and isolation trenches are patterned over this layer. After an 87 minute RIE etch step, isolation trenches are etched through the silicon wafer via a 700 Bosch cycle DRIE step. The masking oxide is removed using RIE (120 minutes). PirL is then spun a couple of times as in the earlier process. After PiRL bake (120 °C; 90 second), lithography is performed to pattern the bond pad openings on polysilicon. Polysilicon is etched using a 2 minute non-Bosch DRIE etch process. Then the ONO layer is etched in a single 3 minute RIE etch step. Photoresist and PiRL are stripped in acetone and developer MF-319 respectively. PiRL is spun again 3-4 times to planarize the surface. Lithography is done to define contact pads, and also to define dice lines. Ti/Au (500 Å / 3000 Å) are sputtered next. Lift is done in developer. Different blocks of capacitors are diced using the dice lines for reference. Finally, the capacitors are wire bonded in the desired fashion.

5.4 Capacitance Calculations

Before proceeding to mask design, the need was felt to ascertain dimensions to achieve the required capacitance. Dr. Shinzo Onishi at University of South Florida [16] concluded that a capacitance of 20nF from each individual capacitor would be enough to achieve the required voltage conversion at 1 KHz frequency, using the parallel charge voltage converter design. Rough calculations were made by adjusting various parameters like pore width, pore pitch, pore depth, and dielectric thicknesses. Simple parallel plate capacitor model was used for these calculations.
As an example –

Assume, Thickness of ONO stack = 10nm-25nm-10nm respectively.

Pore width = 5 micron.

Pore pitch = 10 micron.

Pore depth = 200 micron.

The net dielectric constant of a composite layer is given by –

\[
\varepsilon_{net} = \frac{t_1 + t_2 + t_3}{\left( \frac{t_1}{\varepsilon_1} + \frac{t_2}{\varepsilon_2} + \frac{t_3}{\varepsilon_3} \right)}
\]

Where, \( t_1, t_2 \) and \( t_3 \) are the dielectric thicknesses and,

\( \varepsilon_1, \varepsilon_2 \) and \( \varepsilon_3 \) are the corresponding dielectric constants.

The dielectric constant of oxide is taken to be 3.9 and that of nitride is taken to be 7.5.

Substituting the values, the net dielectric constant is calculated to be \( \varepsilon_{net} = 5.32 \).

The unit cell of the capacitor is shown below.

Figure 61 - Unit Cell of Capacitor
For ease of calculation, the pores are assumed to be perfectly cuboidal in shape. All calculations are with respect to a single unit cell. There are four quarter pores present in each unit cell. Thus, effectively there is one pore per unit cell.

The effective surface area is the sum of the area of the top surface, the side wall area and the pore bottom area.

Thus,

\[ A_{\text{net}} = A_{\text{top}} + A_{\text{side}} + A_{\text{bottom}} \]

\[ A_{\text{top}} + A_{\text{bottom}} = A_{\text{visible}} \]
\[ = 10 \, \mu m \times 10 \, \mu m \]
\[ = 100 \, \mu m^2 \]

\[ A_{\text{side}} = \text{‘pore width’ x ‘pore depth’ x ‘number of walls’} \]
\[ = 5 \, \mu m \times 200 \, \mu m \times 4 \]
\[ = 4000 \, \mu m^2 \]

Therefore,

\[ A_{\text{net}} = (A_{\text{top}} + A_{\text{bottom}}) + A_{\text{side}} \]
\[ = 100 \, \mu m^2 + 4000 \, \mu m^2 \]
\[ = 4100 \, \mu m^2 \]

Capacitance, \( C = \frac{\varepsilon_0 \varepsilon_r A_{\text{net}}}{d} \)

‘d’ is the total thickness of the dielectric layer \( (t_1 + t_2 + t_3) \)

Substituting the required values, one gets, \( C = 4.29 \, pF \)
Specific capacitance  = Capacitance of unit cell / Visible area of unit cell

= \frac{4.29 \text{ pF}}{(10 \mu m \times 10 \mu m)}

= 42.9 \text{ nF/mm}^2

Similar calculations were made with various dielectric thicknesses and pore sizes. Two sets of calculations were made – One for pore depth 100 micron and one for pore depth 200 micron. The results are demonstrated in the figures below.

Figure 62 - Specific Capacitances ( nF / mm$^2$) for 100 µm Deep Pores
In order to get an idea of the required mask dimensions, the capacitor area needed for the desired 20 nF value was calculated for the various parametric dimensions. These are tabulated below.
### Table 8 - Area Needed for 20 nF Capacitors ( $\text{mm}^2$ ) Using 100 $\mu$m Deep Pores

<table>
<thead>
<tr>
<th></th>
<th>10-25-10 nm</th>
<th>20-40-20 nm</th>
<th>40-100-40 nm</th>
<th>50-200-50 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 um hole 10 um pitch</td>
<td>0.91</td>
<td>1.68</td>
<td>3.64</td>
<td>5.63</td>
</tr>
<tr>
<td>5 um hole 20 um pitch</td>
<td>3.19</td>
<td>5.87</td>
<td>12.74</td>
<td>19.69</td>
</tr>
<tr>
<td>10 um hole 20 um pitch</td>
<td>1.74</td>
<td>3.20</td>
<td>6.95</td>
<td>10.74</td>
</tr>
<tr>
<td>10 um hole 40 um pitch</td>
<td>5.46</td>
<td>10.06</td>
<td>21.84</td>
<td>33.76</td>
</tr>
<tr>
<td>20 um hole 40 um pitch</td>
<td>3.19</td>
<td>5.87</td>
<td>12.74</td>
<td>19.69</td>
</tr>
</tbody>
</table>

### Table 9 - Area Needed for 20 nF Capacitors ( $\text{mm}^2$ ) Using 200 $\mu$m Deep Pores

<table>
<thead>
<tr>
<th></th>
<th>10-25-10 nm</th>
<th>20-40-20 nm</th>
<th>40-100-40 nm</th>
<th>50-200-50 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 um hole 10 um pitch</td>
<td>0.47</td>
<td>0.86</td>
<td>1.86</td>
<td>2.88</td>
</tr>
<tr>
<td>5 um hole 20 um pitch</td>
<td>1.74</td>
<td>3.20</td>
<td>6.95</td>
<td>10.74</td>
</tr>
<tr>
<td>10 um hole 20 um pitch</td>
<td>0.91</td>
<td>1.68</td>
<td>3.64</td>
<td>5.63</td>
</tr>
<tr>
<td>10 um hole 40 um pitch</td>
<td>3.19</td>
<td>5.87</td>
<td>12.74</td>
<td>19.69</td>
</tr>
<tr>
<td>20 um hole 40 um pitch</td>
<td>1.74</td>
<td>3.20</td>
<td>6.95</td>
<td>10.74</td>
</tr>
</tbody>
</table>
It is clear from the above charts and tables that the specific capacitance increases as the dielectric thicknesses decrease, and also as the pore pitch decreases. Also it increases as pore depth increases.

As the etching was done using DRIE, pores could be replaced with trenches. It is easy to visualize that the area ratios of the unit cell remain the same in both cases. Thus the calculated data remains unchanged. Trenches are preferred over pores because they are easier for wet as well as dry chemical to reach a trench rather than a pore, without any clogging. Also, rinses are more effective in purging a trench.

As per the calculated values, a mask was created for the isolated capacitor process flow. The process flow requires four lithography steps. Since, it was a first prototype all four layers were printed onto a single mask, each layer being fitted into one quadrant. Three sets of capacitor types were fitted onto the mask. 5 micron hole with 10 micron pitch, 10 micron hole with 20 micron pitch and 20 micron hole with 40 micron pitch. The figures below show the four quadrants of the mask separately.
Figure 64 - Layer 1 of Mask - Trenches for Increase in Effective Area

Figure 65 - Layer 2 of Mask - Isolation Trenches
Figure 66 - Layer 3 of Mask - Polysilicon Etch Regions

Figure 67 - Layer 4 of Mask - Metal Deposition Areas
The mask design is such that capacitors are fabricated in blocks. Each block consists of nine capacitors. All of the nine capacitors within the block are isolated using DRIE trenches 50 micron wide. Each block is separated by dicing along the metal dice lines. Thus a set of nine capacitors can be packaged in one unit. The figure above shows one such block.
5.5 Fabrication

Wafers were fabricated to test the capacitance of these structures. Firstly, CVD of Oxide – Nitride – Oxide was characterized to obtain reliably uniform films without any pin holes. CVD was done on plain wafers without any preprocessing and analyzed for surface defects, thickness variation etc. Highly uniform and very thin films were obtained. The thicknesses suitable for this project were achieved.

![ONO Film (40nm – 100nm – 30 nm) on a Plain Wafer](image)

Figure 69 - ONO Film (40nm – 100nm – 30 nm) on a Plain Wafer

Very low resistivity (0.001 ohm-cm) <100> n-type wafers were used for capacitor fabrication. Initial capacitors were made on plane wafers without using trenched structures. This was to reliably characterize the furnaces and also test the basic capacitor structure. Each block of capacitors was separated via dicing. The figure below shows the fabricated plain wafer. Testing of the entire block was done for capacitance at various frequencies.
Figure 70 - Plain Capacitor Showing Bond Pads on Polysilicon and Silicon

Figure 71 - Dielectric and Polysilicon Layers of Plain Capacitor
The dielectric layer thicknesses observed are 21nm, 7nm and 8.5nm for the ONO layers. The polysilicon layer was observed to be 391nm.

A significant result is seen in Figure 72. This figure shows the cross section across the edge of a bond pad opening. It is seen that the polysilicon is clearly isolated from the silicon substrate. There is a distinct overhang of the dielectric beyond the edge polysilicon film. It should be kept in mind that the opening in the dielectric and polysilicon is the same on the mask. The polysilicon layer is over-etched (2 minute etch instead of the required 45 seconds) in the non-Bosch DRIE system to ensure electrical isolation seen above.
5.5.1 Plain Capacitor Testing and Analysis

The table shows the values of capacitance and series resistance of one of the various capacitors that were measured.

Table 10 - Capacitance and Series Resistance Measurement of Plain Capacitor

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Series Capacitance $C_s$</th>
<th>Series Resistance $R_s$</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 Hz</td>
<td>59.885 nF</td>
<td>52.069 kΩ</td>
</tr>
<tr>
<td>120 Hz</td>
<td>48.516 nF</td>
<td>47.712 kΩ</td>
</tr>
<tr>
<td>1 KHz</td>
<td>21.225 nF</td>
<td>16.547 kΩ</td>
</tr>
<tr>
<td>10 KHz</td>
<td>4.9662 nF</td>
<td>15.461 kΩ</td>
</tr>
<tr>
<td>100 KHz</td>
<td>280.63 pF</td>
<td>8.534 kΩ</td>
</tr>
</tbody>
</table>

Figure 73 - Capacitance Dependence on Frequency for the Fabricated Capacitors
It is observed that the capacitance values at low frequency are in range of the calculated capacitance of 37\text{nF}. However, the series resistance is too high. An analysis of this result can help explain the frequency variation of capacitance.

Series resistance can arise from various different sources [14]:

- Contact made by the probe wire to the metal pads.
- The resistance of the quasi-neutral bulk silicon and polysilicon.
- An extremely non-uniform doping distribution in the silicon.

Any or all of these reasons might have contributed to the high series resistance obtained.

It should be kept in mind that the polysilicon layer had a resistivity of only 0.02 ohm-cm, and this low doping level would also contribute to the increase the series resistance. Thus, a lower resistivity polysilicon layer and higher doping of silicon are needed to ensure lower ESR’s.

The equivalent diagram of a MOS capacitor is shown in the figure below. The capacitor is in the accumulation region at zero bias. The oxide capacitance is in series with the accumulation layer capacitance $C_A$.

![Equivalent Circuit of the MOS Capacitor in Accumulation](image)

Figure 74 - Equivalent Circuit of the MOS Capacitor in Accumulation
The series resistance of a MOS capacitor is known to vary inversely with frequency, as shown by the equation below.

\[ R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \]

\( G_{ma} \) is the measured equivalent parallel conductance and \( C_{ma} \) is the measured accumulation capacitance. This shows that inverse dependence of the series resistance is as expected.

The accumulation capacitance is given by –

\[ C_{ma} = \frac{C_{ar}}{1 + \omega^2 R_s^2 C_{ar}^2} \]

It is evident from the above equation that a high value of series resistance would drastically bring down the accumulation capacitance at higher frequency. This effect is seen in the above results.

It is emphasized that both capacitance and conductance measurements are highly affected by series resistance, particularly at higher frequencies and thus care should be exercised in both, the preparation of the samples and in the techniques used in measurement [14].
CHAPTER 6
CONCLUSION

This research explored high voltage conversion via switched capacitors with specific relevance to MEMS applications. It has been shown that switched capacitor voltage converters offer unique benefits over conventional magnetic component based converters. The significance of these benefits gets amplified as one scales down in size. For the high voltage demanding micromachined devices, the use of these converters no longer remains a matter of mere convenience or spatial merit. Instead, they become an enabling technology without which the implementation of many a great ideas would be inconceivable.

This technology holds more scope than this thesis has presented. Since, this converter was fathomed for a particular application i.e. MEMS, its design and functionality were developed and discussed singularly for this purpose. However, one can easily envision a broader utilization. Minor alterations can result in a more generic converter. With ever-improving component design (of switches or capacitors) next generation converters can be built to serve non-MEMS based systems as well.

In an endeavor to customize the high voltage converter for MEMS, this research resulted in the innovation of micromachined capacitor banks. This technique of microcapacitor fabrication brings in fresh opportunity for microcapacitors, which so far have been neglected by the industry. Packaging of multiple capacitors together has not
yet been reported. This method can potentially result in a micromachined capacitor bank connected in complex topology, but at the same time equal in size to a single commercial capacitor. The merits of such a capability are enormous. This again is a concept with broader applicability, presented here for a particular one.

MEMS devices utilizing high voltage converters utilizing MEMS devices is a unique case of ‘technology reproduction’ (an enabling technology enabling itself). It is certain that this is just the beginning of a similar trend in micromachining. It is not far that a microsystem would encompass seamless integration of multiple micromachined devices. Lab-on-a-chip is already a common coin word. Factory-on-a-chip would perhaps be the next.
REFERENCES


15. Rajshekhar Popuri, _private communication._

16. Dr. Shinzo Onishi, _private communication._
APPENDIX A: VHDL Coding

The following is the VHDL program that was written to implement the high frequency CPLD control logic.

library IEEE;

use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following lines to use the declarations that are
-- provided for instantiating Xilinx primitive components.

--library UNISIM;
--use UNISIM.VComponents.all;

entity HVC_code is
    Port ( clk : in std_logic;
          sel : in std_logic_vector(1 downto 0);
          disch : out std_logic;
          ch : out std_logic;
          sw : out std_logic_vector(3 downto 0));
end HVC_code;
architecture Behavioral of HVC_code is

signal wcount: std_logic_vector (5 downto 0);

begin

wvform: process (clk) is
begin
if (clk'event and clk='1') then
    wcount <= wcount + 1;
end if;

if (wcount > "100111") then
    wcount <= "000000";
end if;

if (wcount > "100111") then
    wcount <= "000000";
end if;

if (wcount <= "010011") then
    disch <= '1';
    ch <= '0';
elsif (wcount >= "010101" and wcount <= "100110") then
    disch <= '0';
APPENDIX A: (Continued)

ch <= '1';

else

  disch <= '0';
  ch <= '0';

end if;

end process wvform;

tuning: process (sel) is

begin

  case sel is

    when "00" => sw <= "1000";
    when "01" => sw <= "0100";
    when "10" => sw <= "0010";
    when "11" => sw <= "0001";
    when others => sw <= "1000";

  end case;

end process tuning;

end Behavioral;