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CVD Growth of SiC on Novel Si Substrates

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CVD Growth of SiC on Novel Si Substrates

by

Rachael L. Myers

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Chemical Engineering
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Keywords: Cubic Silicon Carbide, Silicon Carbide, Epitaxy, Chemical Vapor Deposition

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## TABLE OF CONTENTS

LIST OF TABLES iii  
LIST OF FIGURES iv  
ABSTRACT vii

### CHAPTER 1 INTRODUCTION 1
1.1 3C-SiC Overview 1  
1.2 Heteroepitaxy of 3C-SiC on Si 4  
1.3 Defect Reduction Using Novel Substrates 7  
1.4 Summary 9

### CHAPTER 2 HETEROEPITAXY OF 3C-SIC 11
2.1 Review of Growth Methods 11  
2.1.1 Liquid Phase Epitaxy (LPE) 11  
2.1.2 Molecular Beam Epitaxy (MBE) 13  
2.1.3 Vapor Phase Epitaxy (VPE) 14  
2.2 USF SiC CVD Reactor 20  
2.3 Lattice Mismatch of 3C-SiC on Si Substrates 25  
2.4 Novel Si Substrates for 3C-SiC Growth 29  
2.4.1 Porous Silicon 29  
2.4.2 Undulant Silicon 31  
2.4.3 Silicon on Insulator (SOI) 35  
2.5 Summary 37

### CHAPTER 3 APCVD PROCESS DEVELOPMENT 38
3.1 Carbonization of Si(001) 38  
3.2 3C-SiC Growth on Si(001) 40  
3.3 3C-SiC Growth on Porous Si 45  
3.4 3C-SiC Growth on Porous 3C-SiC Substrates 52  
3.5 Summary 55

### CHAPTER 4 LPCVD PROCESS DEVELOPMENT 57
4.1 LPCVD Reactor Hardware Development 57  
4.1.1 150 Torr Modification 57  
4.1.2 Gas Jetting Modification 60  
4.2 Carbonization of Si(001) 61  
4.3 3C-SiC Growth on Si(001) 64
4.4 3C-SiC Growth on Porous Si(001)  68
4.5 3C-SiC Growth on SOI Substrates  72
4.6 Summary  80

CHAPTER 5 CONCLUSIONS AND FUTURE WORK  81
5.1 Conclusions  81
5.2 Future Work  83

REFERENCES  87
LIST OF TABLES

Table 1.1 Properties of typical SiC polytypes compared to Si, GaAs, and GaN. 2
LIST OF FIGURES

Figure 1.1  Stacking orders of the three most common polytypes in SiC. 3
Figure 1.2  Illustration of the affect of lattice mismatch in hetero epitaxy. 6
Figure 1.3  Schematic of undulant silicon substrate [12]. 8
Figure 2.1  LPE method by way of vertical dipping [4]. 13
Figure 2.2  Diagram of the growth zone for two types of cold-wall reactors (a) horizontal (b) vertical [15]. 16
Figure 2.3  Schematic diagram describing the CVD process. 17
Figure 2.4  Representation of the tight regime between etching and deposition for Si growth [18]. 19
Figure 2.5  Photograph of the USF 75 mm horizontal cold-wall reactor. 21
Figure 2.6  Side view of quartz reaction tube with the following details: (1) gas inlet, (2) quartz boat, (3) SiC coated susceptor, (4) gas outlet, and (5) cooling water jacket. 22
Figure 2.7  Cross-sectional view of USF CVD reactor. 23
Figure 2.8  Elastic accommodation of a film lattice to the substrate lattice. 27
Figure 2.9  (a) Elements of a dislocation between real crystal and ideal crystal. 28
Figure 2.10 Plan-view SEM image of 3C-SiC growth on porous Si showing large rectangular terraces [11]. 31
Figure 2.11 Illustration of crystal defects in 3C-SiC: (a) twin boundaries, (b) anti-phase boundaries [16]. 32
Figure 2.12 Elimination of twin boundaries using undulant Si substrate. 34
Figure 2.13 SOI substrate for growth of 3C-SiC. 36
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Optical micrograph of etch pits produced from the H$_2$ etch step of the Si substrate.</td>
</tr>
<tr>
<td>3.2</td>
<td>APCVD carbonization process schedule including the initial etch step.</td>
</tr>
<tr>
<td>3.3</td>
<td>APCVD process schedule developed for growth of 3C-SiC on Si(001).</td>
</tr>
<tr>
<td>3.4</td>
<td>Plan view SEM micrographs of 3C-SiC grown on Si(001) for various flow rates.</td>
</tr>
<tr>
<td>3.5</td>
<td>(a) Cross section TEM data of 3C-SiC grown on Si(001), (b) SAD data of 3C-SiC grown on Si(001).</td>
</tr>
<tr>
<td>3.6</td>
<td>XRD data of 3C-SiC grown on Si(001).</td>
</tr>
<tr>
<td>3.7</td>
<td>Plan view SEM micrographs of some porous Si prior to growth.</td>
</tr>
<tr>
<td>3.8</td>
<td>Cross-sectional SEM micrograph after 3C-SiC epi growth on porous Si.</td>
</tr>
<tr>
<td>3.9</td>
<td>Plan-view SEM micrographs of (a) porous Si (Sample ID: PS #7) and (b) 3C-SiC grown on the porous Si shown in part (a) (Sample ID USF-03-033A).</td>
</tr>
<tr>
<td>3.10</td>
<td>LTPL data from USF-03-033A (standard Si), USF-03-033B (porous Si).</td>
</tr>
<tr>
<td>3.11</td>
<td>TEM data from USF-03-033B (porous Si) showing the defect network in the film.</td>
</tr>
<tr>
<td>3.12</td>
<td>Process developed by Hoya Corporation to produce free-standing 3C-SiC from 3C-SiC grown on undulant Si substrates [33].</td>
</tr>
<tr>
<td>3.13</td>
<td>Process flow developed for growth of 3C-SiC on free standing porous 3C-SiC.</td>
</tr>
<tr>
<td>3.14</td>
<td>SEM micrographs of 3C-SiC grown on free-standing porous 3C-SiC (P-3C).</td>
</tr>
<tr>
<td>4.1</td>
<td>Reactor LP hardware implemented in [35] and modified here to achieve proper LPCVD operation.</td>
</tr>
<tr>
<td>4.2</td>
<td>Photo of gas diffuser installed during this research to eliminate gas jetting in the reactor.</td>
</tr>
</tbody>
</table>
Figure 4.3  Carbonization process flow initially used under APCVD conditions.  

Figure 4.4  SEM micrographs after carbonization of Si(001).  

Figure 4.5  Process flow of low-pressure carbonization step used in Figure 4.4.  

Figure 4.6  SEM micrograph of 3C-SiC/Si morphology for growth at low pressure.  

Figure 4.7  Process flow for growth process of 3C-SiC on Si(001) under LPCVD conditions without a separate oxide etch step.  

Figure 4.8  SEM micrograph of 3C-SiC grown on Si(001) at low pressure using the process shown in Figure 4.7.  

Figure 4.9  Process flow for growth of 3C-SiC on porous Si(001) under LPCVD conditions.  

Figure 4.10  SEM micrographs of (a) standard Si(001): USF-03-160G, (b) porous Si(001): USF-03-160B, (c) oxidized and annealed porous Si(001): USF-03-160A.  

Figure 4.11  Graph of thermal expansion coefficient versus temperature comparing Si, 3C-SiC, and Poly 3C-SiC [14].  

Figure 4.12  Step flow process to produce ceramic substrates for growth of 3C-SiC [14].  

Figure 4.13  Step flow of 3C-SiC process on ceramic ‘SOI’ substrate.  

Figure 4.14  3C-SiC on ceramic substrate (3C-SOI) process schedule developed during this thesis research.  

Figure 4.15  Plan view SEM micrographs of 3C-SiC grown on a ceramic substrate; 1 hr growth produced film thickness of 2 µm determined from a standard Si(001) sample via cross-section SEM (not shown).  

Figure 4.16  Rocking curves for USF 3C-SiC epi grown on NRL fabricated 3C-SiC on ceramic substrates.
Silicon Carbide has been a semiconductor material of interest as a high power and temperature replacement for Silicon (Si) in harsh environments due to the higher thermal conductivity and chemical stability of SiC. The cost, however, to produce this material is quite high. There are also defects in the substrate material (SiC) that penetrate into the active devices layers which are known device killers. Silicon is a material that provides a low cost substrate material for epitaxial growth and does not contain the defects that SiC substrates have. However, the large (~22%) lattice mismatch between Si and SiC creates dislocations at the SiC/Si interface and defects in the SiC epitaxial layer. These defects result in high leakage currents in 3C-SiC/Si devices. The main focus of the this research was to reduce or eliminate these defects using novel Si substrates.

First a 3C-SiC on Si baseline process was developed under atmospheric pressure conditions consisting of 3 steps – an in-situ hydrogen etch to remove the native oxide, a carbonization step to convert the Si surface to SiC, and finally a growth step to thicken the SiC layer to the desired value. This process was then modified to establish a high-quality, low-pressure 3C-SiC CVD growth process. This LPCVD process was then used to grow 3C-SiC on numerous novel Si substrates, including porous Si, porous 3C-SiC ‘free-standing’ substrates and SOI substrates which consisted on thin Si films bonded to
poly-crystalline SiC plates. The results of these experiments are presented along with suggestions for future work so that device-grade films of 3C-SiC can be developed for various applications.
CHAPTER 1
INTRODUCTION

1.1 3C-SiC Overview

Silicon carbide (SiC) has long been of interest as a high-power and temperature replacement to silicon (Si) for use in harsh environments. SiC is a robust semiconductor material which is currently used in high-power, high-frequency, and high-temperature device applications [1]. These applications are prominent due to SiC being a wide-band gap material with high thermal conductivity and physical stability. Table 1.1 shows that SiC has a larger band gap and higher thermal conductivity than Si, allowing SiC to operate at higher temperatures for electronic applications.

Initially SiC was used as an abrasive material. The substance can only be found naturally in meteorites. J. A. Lely from Philips Research Labs first initiated the process of growing device-grade SiC in 1955 where he produced randomly sized crystals of hexagonal shape [2]. In 1987, the first single polytype crystal of SiC was made by seeded sublimation growth, a modification of the Lely method. In the same year, the first SiC company, Cree, Inc., was started by a university research group at the North Carolina State University (NCSU) and began commercial production of SiC wafers and blue light emitting diodes (LED’s) [2].

SiC has many different polytypes (~170), or crystal structures, each having different electrical and physical properties. Figure 1.1 shows the most commonly studied
polytypes of SiC; cubic 3C-, and hexagonal 4H- and 6H-SiC [3]. Note that the lettering A, B, and C denotes the positioning of the atoms [4]. The stacking order of the tetrahedrally bonded bilayers differentiates each polytype from the other [5]. One crystallographic orientation is β-SiC, also known as 3C-SiC (cubic). This polytype is the only purely cubic polytype, while the others have both cubic and hexagonal structure (except for 2H-SiC which is the only pure hexagonal polytype [4]). The 3C-SiC polytype has the highest electron mobility of all SiC polytypes, no anisotropy and low temperature stability [6]. The cubic lattice structure allows the electrons to move more freely compared to 4H- and 6H-SiC, since the crystal is not as densely packed as the hexagonal close packed (hcp) structure.

Table 1.1 Properties of typical SiC polytypes compared to Si, GaAs, and GaN [6].

<table>
<thead>
<tr>
<th>Properties</th>
<th>3C-SiC</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
<th>Si</th>
<th>GaAs</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Structure</td>
<td>Indirect</td>
<td>Indirect</td>
<td>Indirect</td>
<td>Indirect</td>
<td>Direct</td>
<td>Direct</td>
</tr>
<tr>
<td>Band Gap [eV]</td>
<td>2.2</td>
<td>3.0</td>
<td>3.3</td>
<td>1.11</td>
<td>1.43</td>
<td>3.5</td>
</tr>
<tr>
<td>Electron Mobility [cm$^2$/V s]</td>
<td>1000</td>
<td>450</td>
<td>900</td>
<td>1500</td>
<td>8500</td>
<td>900</td>
</tr>
<tr>
<td>Hole Mobility [cm$^2$/V s]</td>
<td>50</td>
<td>50</td>
<td>100</td>
<td>600</td>
<td>400</td>
<td>30?</td>
</tr>
<tr>
<td>Breakdown Field [MV/cm]</td>
<td>2</td>
<td>3</td>
<td>3</td>
<td>0.3</td>
<td>0.4</td>
<td>3</td>
</tr>
<tr>
<td>Thermal Conductivity [W/cm K]</td>
<td>4.9</td>
<td>4.9</td>
<td>4.9</td>
<td>1.5</td>
<td>0.5</td>
<td>1.3</td>
</tr>
<tr>
<td>Electron Saturation Velocity [10$^7$ cm/s]</td>
<td>2.7</td>
<td>2</td>
<td>2.7</td>
<td>1</td>
<td>2</td>
<td>2.5</td>
</tr>
</tbody>
</table>
The hexagonal (4H- and 6H-SiC) substrates are commercially available. However, they are not of high quality due to a high density of physical defects. Other problems are the high cost and limited diameter (3” currently available commercially although 4” have been demonstrated). A benefit of 3C-SiC is that large-area, single-crystals can be produced since this polytype can be grown on silicon (Si) substrates, unlike 4H- and 6H- which are homoepitaxially grown on SiC substrates. More importantly, 4H- and 6H-SiC have a high density of defects, such as micropipes and screw dislocations, in the substrates which result in defects in the epitaxial layer. Silicon substrates have no such defects, resulting in an epitaxial layer which does not contain micropipes or screw dislocations, the predominant defects in crystals grown from the hexagonal polytypes.

**Figure 1.1** Stacking orders of the three most common polytypes in SiC. From left to right, 4H-SiC, 6H-SiC, and 3C-SiC. k and h denote crystal symmetry points that are cubic and hexagonal, respectively. Figure courtesy of O. Kordina, Caracal Semiconductor [3].
From Table 1.1, it is noted why SiC is suitable for high power and high temperature devices. The thermal conductivity of SiC is substantially higher than Si allowing both operational use at high temperatures and the devices to dissipate self-generated heat during operation. The large electric breakdown field strength of SiC permits high-power operation. Finally the large saturated drift velocity enables high-speed carrier transport to be supported. 3C-SiC has many practical uses such as in the area of gas sensors [7], fuel cells and biomedical applications [42]. Currently the SiC Group at the University of South Florida (USF) is exploring the use of 3C-SiC for gas sensors to detect hydrogen [7]. Sensors have been fabricated from material grown during this research work (see Chapter’s 3 and 4). Further information can be obtained from reference [7]. SiC is a material that is known to be biocompatible, in that the body does not reject it and cells may easily attach to the surface of SiC material [31]. Therefore, tissue can be grown on this material which may then be inserted into the human body as a ready-made implant. For sensors, it may be that a certain pathogen such as anthrax may bind to the SiC surface, then one may detect whether the pathogen is present or not. Solid-state silicon fuel cells may be replaced with SiC fuel cells in order to increase their output power [8]. Using 3C-SiC instead of 4H- or 6H-SiC might lower the cost of the fuel cells and increase the surface area. Therefore, there are many applications for the use of 3C-SiC provided the challenges of its growth on Si substrates are met.

1.2 Heteroepitaxy of 3C-SiC on Si

Heteroepitaxy of 3C-SiC on Si (denoted as 3C-SiC/Si) is motivated by the use of an economical substrate (Si) that surpasses in size and cost compared to SiC substrates
Currently, the maximum diameter of commercial SiC substrates is 3 inch, whereas Si substrates are available up to 12 inch. Thus, the number of devices per wafer is potentially greater on Si than SiC. This factor, coupled with the isotropic nature of 3C-SiC compared to the hexagonal polytypes, provides the motivation for developing device-grade 3C-SiC/Si technology.

Epitaxy is the growth of a thin layer on a crystal substrate in which the substrate is a template for the growth. Heteroepitaxy is the growth of an epitaxial layer on a seed crystal of a different type. Cubic SiC may be heteroepitaxially grown on Si substrates and, until recently, single crystal, large-area, bulk 3C-SiC crystals did not exist. The growth of 3C-SiC epi layers is micropipe free which is critical since micropipes are known SiC device killers [9]. However, the 22% lattice mismatch between the Si and SiC which causes the epi to not be of device quality. The lattice mismatch results in stress that causes planar defects in the epitaxial layer such as misfit dislocations, microtwins, and stacking faults at the interface of Si and SiC. These defects then propagate into the 3C-SiC layer and result in high leakage currents in 3C-SiC/Si devices. Indeed the problems with this material system have led many groups to abandon 3C-SiC/Si. In this thesis, we aim to use novel patterned substrates to mitigate and/or eliminate these defects with the goal of developing device-quality 3C-SiC/Si layers.
Figure 1.2 Illustration of the affect of lattice mismatch in hetero epitaxy. The \(-\) symbol denotes the location of a missing row of atoms which is known as a line defect. Note the stretched and compressed covalent bonds at the interface resulting from the lattice mismatch between the two crystals.

As seen in the figure, there is a strain in the epi layer from an attempt by the epi layer \((a_{\text{SiC}} = 4.36\text{Å})\) [43] to accommodate the substrate’s lattice constant \((a_{\text{Si}} = 5.43095\text{Å})\). The result of this not only produces defects, but defects in the epitaxial layer having mosaic morphology in the case of the 3C-SiC/Si system. While a carbonization step is normally employed which converts the Si surface to SiC and acts as a buffer layer to reduce this stress, this is not enough to completely accommodate the mismatch. With this buffer layer, there are still a fair amount of dislocations which must be reduced if 3C-SiC is to be suitable for device applications.
1.3 Defect Reduction Using Novel Substrates

Many techniques have been researched to reduce the effects of defects caused by the lattice mismatch at the SiC/Si interface. Some techniques being researched at USF are growth on porous silicon, on nano-patterned (pyramidal) Si and on Si films bonded to ceramic SiC substrates. Researchers have experimented with the growth of 4H- and 6H-SiC on porous SiC substrates with promising results in the area of reduced defect densities [10]. With this idea in mind, it is thought that growth of 3C-SiC on porous Si would give way to similar results. Indeed this is not a new idea and results from research in this area have already been reported in the literature [11]. The mechanism that is believed to result in improved 3C-SiC films on porous Si is that the porous Si may relieve the stress caused by the lattice mismatch. The pores act as a compliant layer which allows the epitaxy of 3C-SiC to form in its ideal bulk lattice constant due to deformation of the underlying Si crystal. However this is just speculation at this time and additional research by the SiC Group at USF is being conducted to shed light on this subject.

Growth of thick 3C-SiC films on undulant Si has been researched by Hoya Corp. in Japan [12]. Undulant silicon consists of specially prepared Si wafers that contain ridges along the [-110] direction, as shown in Figure 1.3 [12]. The undulations are used to eliminate or reduce planar defects caused by the Si/SiC lattice mismatch by canceling each other out from two directions. Looking at Figure 1.3, it can be seen that there are ridges and valleys in the Si undulant surface. In the v-sections (ridges and valleys), there will be defects developing perpendicular to the growth facets. When the defects continue to grow, they will eventually collide and cancel with defects growing from facets in the opposite direction. Therefore, there will be a reduction in the defect density, especially
for extended film growth. That is, the defect density dramatically diminishes for longer
growth times. This is also the case for 3C-SiC growth on standard Si(001) [13]. Once a
thick 3C-SiC layer is grown, the Si substrate may be removed yielding a free standing
3C-SiC substrate which allows growth at higher temperatures. Indeed Hoya has
developed such substrates and has made them available to the University of Pittsburgh
for porous anodization. These samples were then made available to USF for growth on
the porous 3C-SiC buffer layers prepared by University of Pittsburgh. In addition,
growth studies by Saddow and Rao in our laboratory on non-porous (i.e., standard) bulk
3C-SiC Hoya material have been conducted to determine the quality of the resulting
films. These results will be presented in Chapter 4 of this thesis.

Figure 1.3 Schematic of undulant silicon substrate [12].

The final method being studied for defect reduction presented in this thesis is the
growth of 3C-SiC on silicon-on-insulator (SOI) substrates provided by K. Hobart of the
Naval Research Laboratory [14]. For these SOI substrates, a thin layer of silicon (100Å
thick typically) is transferred to a polycrystalline SiC plate and thermally bonded. The samples are then diced and RCA cleaned in preparation for growth in the USF SiC CVD reactor. Due to the ultra-thin nature of the Si film, the standard in-situ hydrogen etch step is not used as we learned that it completely removes the thin Si layer. Instead the silicon surface is immediately converted to SiC via a carbonization step. 3C-SiC growth is then conducted producing a high-quality epitaxial layer of 3C-SiC. Since the layer is supported by a high-temperature poly-crystalline SiC substrate with a high sublimation temperature (greater than 2000 °C), growth can, in principle, be performed at higher temperatures, up to the normal homoepitaxy temperatures of 1580 °C. This is likely to result in lower defect densities and produce better morphology. However this work has just been initiated and this goal has yet to be achieved. Details of this work will also be presented in greater detail in Chapter 4 of this thesis.

1.4 Summary

This thesis will report on research conducted on the growth of 3C-SiC and the methods studied to improve the quality of the epitaxy. 3C-SiC is a promising material for applications of high power, high frequency and high temperature devices. The material is cost effective and may be grown on a larger scale than 4H- and 6H-SiC. The silicon substrate does not contain any defects such as micropipes which allows the epitaxy to be free of these device-killing defects. There are many positive attributes of 3C-SiC on Si, however, there is a 22% lattice mismatch that causes defects at the Si/SiC interface. This limits the resulting material quality for device applications. With developing research and methods, 3C-SiC may become device quality material.
There are four main chapters to this thesis. Chapter Two will begin with a review of the different types of epitaxial growth methods. The reactor used to grow epitaxy (both homoepitaxy and heteroepitaxy) at USF will be described. An in-depth review of each type of defect reduction method will be presented; namely the use of porous Si, undulant Si, and SOI substrates. Chapter Three will discuss the results produced from atmospheric pressure chemical vapor deposition (APCVD) 3C-SiC studies at USF. The types of research performed to improve the quality of the films and methods used at APCVD will be shown. The next chapter describes the research done under low pressure CVD (LPCVD) conditions. Lastly, Chapter 5 will give a summary of the thesis and provide suggestions for future work on 3C topics.
CHAPTER 2
HETEROEPITAXY OF 3C-SIC

2.1 Review of Growth Methods

Epitaxial layers are needed to produce device quality material and are traditionally grown on bulk substrates. There are three main techniques to grow epitaxial layers; liquid phase epitaxy (LPE), vapor phase epitaxy (VPE), and molecular beam epitaxy (MBE). The two methods that were initially used for growing SiC epilayers are LPE and VPE [4]. However, vapor phase techniques, and more specifically chemical vapor deposition (CVD), have become the method of choice due to some difficulties with the LPE technique. The other technique for epitaxial growth that will be discussed in this chapter is molecular beam epitaxy although it has found limited use in SiC due to the extremely low growth rates of the films.

2.1.1 Liquid Phase Epitaxy (LPE)

Liquid phase epitaxy is a technique used to deposit many different epitaxial layers onto a substrate [15]. Epitaxial layers from this technique can be grown at low temperatures (350 to 900°C), resulting in high growth rates, such as 0.1 mm/min. The method is relatively inexpensive and produces a low concentration of point defects; however, the surface morphology is difficult to control which makes CVD favorable [15]. There are two principle approaches to LPE which are from a melt and by vertical dipping.
In the LPE technique, by way of a melt, there is a melt of supersaturated components which cool on the substrate and form a solid [4]. The phase diagram of Si-C determines the maximum amount of growth from a Si-C melt solution [4]. The components, for example, Si and C, are in a solvent melt and when the process cools, the Si and C will form a solid on the SiC substrate. The growth will result in an epi layer of the same crystal orientation as the substrate. In the early 1970’s, a single-crystal layer, with the same polytype as the substrate, was produced from a carbon-saturated Si solution by LPE [4]. In the 1980’s, SiC was made from a Si melt in which the substrate was placed on the bottom of a graphite crucible that was filled with solid Si pieces. The process was brought to 1800°C and then cooled slowly so the substrate would not crack; this resulted in a growth rate of 1 µm/min [4]. The main difficulty with the LPE process is damage to the SiC epilayer from the stress caused by the melt solidification [4]. A method used to solve this is vertical dipping, where the substrate is applied to a graphite holder and dipped into melted Si for a period of 5 hours. Figure 2.1 gives an illustration of this process. The growth temperature from this experiment was between 1500 and 1750°C and a growth rate of 4 – 10 µm/hr resulted [4].
The poor morphological outcome of LPE growth is one of the main reasons CVD is preferred (CVD will be discussed in section 2.1.2) over the LPE method. Epitaxial layers are grown on substrates that are in a step-like (i.e. vicinal) orientation. The growth occurs by the attachment of atomic species on the steps and propagates parallel to the surface [15]. With thicker growth, step bunching results from the coalescence of terraces (steps) in the epilayer. If the step growth is too large, step bunching is likely to occur. However, to reduce this, the misorientation of the substrate must be less than 0.1° (as in the case of GaAs) [15]. For surfaces that have such small misorientations, the step height is extremely small and polytype control is nearly impossible.

2.1.2 Molecular Beam Epitaxy (MBE)

MBE is the process in which molecular beams of constituents react with a crystalline surface in an ultrahigh vacuum (UHV) chamber to produce epitaxial layers [15]. The MBE system is commonly referred to as an evaporation apparatus. The MBE
process is conducted at low temperatures (800-1000°C), and, as a result, extremely low growth rates are achieved (6.2 nm/hr) [44]. Molecular beam epitaxy is unlike any other epitaxial process due to the high quality of the films produced. In addition, MBE has the benefit of in-situ diagnostics which are able to monitor the growth surface during deposition by means of reflection high-energy electron diffraction-(RHEED). Many different chemical sources can placed in crucibles in the MBE system where shutters control the flux of the molecular beams from these sources. The crucibles are heated to a desired temperature that is controlled within ±1°C of the set temperature. With the temperature set, the shutters are actuated to allow changes in the film composition and doping of the layers. A substrate is placed in the MBE chamber and the molecular beams impinge the surface, in which atomic species are absorbed and migrate to the surface of the substrate to produce a film. While MBE is the preferred method for high-quality growth of heterostructures in III-V technology, the higher growth temperatures required for SiC MBE has limited this approach.

2.1.3 Vapor Phase Epitaxy (VPE)

Vapor phase epitaxy, in which chemical vapor deposition (CVD) is a subset of, is a process were a reaction between a gas and a crystalline surface occurs resulting in deposition of a solid on the substrate surface. There are different types of reactors for CVD; cold-wall, horizontal, atmospheric-pressure reactors; cold-wall, vertical (and horizontal), low-pressure reactors; and hot-wall, horizontal, low-pressure reactors. Figure 2.2 shows diagrams of both a horizontal reactor and a vertical reactor. Hot-wall reactors are basically isothermal furnaces, in which the temperature uniformity is
optimal. The growth of SiC is extremely uniform due to the uniformity of the susceptor and substrate temperature. Cold-wall reactors maintain a cool reaction chamber envelope except for the area surrounding the susceptor. In this type of design, the reactants are deposited in the highest temperature area (the susceptor, which supports the substrate). This is meant to keep the deposition mainly on the wafer; however, deposition on the walls of the reactor still occurs. Commercial reactors are available for SiC growth that can handle up to seven 2” wafers [16]. Low-pressure reactors are used to ensure laminar flow, which results in improved uniformity in the grown layers. The thermal energy needed for these types of systems are obtained from resistive or radio frequency (rf) induction heating [4].

Susceptors used in CVD reactors are normally made of graphite and are usually coated with either SiC or another ceramic, such as TaC. There have been studies conducted to compare the contaminants produced from these two types of susceptors. Bare graphite susceptors result in a high level of aluminum, boron and nitrogen contaminants in the epitaxial layer, while the SiC (100 to 120 μm thick) coated graphite susceptors reduce the levels of these contaminants [4]. One study conducted to reduce the contaminants from the graphite susceptor was to use a vertical low-pressure reactor with the substrate undergoing high-speed rotation allowing the gas flow to be in a favorable pattern [4].
To grow SiC epilayers, a carrier gas of ultra-high purity (UHP) hydrogen is needed as well as precursors which serve as the carbon source and silicon source. The carbon source comes from hydrocarbons, such as $\text{C}_2\text{H}_2$, $\text{CH}_3\text{Cl}$, $\text{CH}_4$, $\text{C}_7\text{H}_8$, and most commonly, $\text{C}_3\text{H}_8$ (propane). The silicon source most commonly used is $\text{SiH}_4$ (silane), but others have been used such as $\text{Si}_2\text{H}_6$ and $\text{SiCl}_4$. The precursors crack at high temperatures to produce the Si and C species needed for growth. Experimental studies have shown that in the case of $\text{H}_2$, $\text{SiH}_4$, and $\text{C}_3\text{H}_8$ gas sources, an intermediate species ($\text{SiH}_2$) may also play a role in the development of the SiC epitaxial film [4].

A specific sequence of events must occur in order to grow SiC epilayers on a substrate via CVD, as shown in Figure 2.3. Initially, the reactant gases enter the reactor by forced flow. Then, the gases diffuse through a boundary layer that is above the susceptor and substrate. The reactant gases are then adsorbed on the surface of the substrate where the reaction takes place. The desorption of the by-products away from the substrate takes place and then the gases diffuse back through the boundary layer into
the main gas stream. The gas flow of the system is ideally laminar, which means that the gas velocity at the walls is zero.

A boundary layer is produced and is essentially a gradient of velocity starting at zero on the walls, and increasing to the velocity of the main gas flow in the center of the reaction tube. The boundary layer starts at the inlet of the tube and increases until the flow becomes stabilized [17]. The reactants must diffuse through this layer to reach the surface of the substrate. When the velocity of the gases increases, the boundary layer becomes thinner because the flow stabilizes faster at the higher velocities. Like-wise, when the velocity of the reactant gases decreases, the boundary layer becomes thicker. The concentration of the reactant gases plays an important role in the deposition in that the gases will eventually become depleted as they react to form the deposit.

![Figure 2.3](image-url)  
**Figure 2.3** Schematic diagram describing the CVD process. Step (1) Diffusion of reactants through boundary layer, (2) Adsorption of reactants to substrate surface, (3) Surface reaction, (4) Desorption of by-products away from substrate surface, (5) Diffusion through boundary layer into main reactant stream [17].
Rate limiting steps determine the rate of deposition of the epitaxial layer. A rate limiting step is one that controls the process, i.e. it is the slowest step and thus the growth rate is limited by this process. In the CVD process, the rate limiting step can be from surface reaction kinetics or mass transport. For surface reaction kinetics limited growth, the rate of deposition is dependent on the surface reaction (it is the slowest step). The reactants are diffusing fast enough to the surface because the boundary layer is thin due to high gas velocity (i.e. low pressure); however, the reaction can not occur as quickly as the reactants are getting to the surface. The reaction may be slow due to the temperature at the substrate surface not being high enough as well as other reasons. A mass transport limited process occurs when the reactant gases are not diffusing fast enough to the surface of the substrate to support the surface reaction. This may be caused by the boundary layer being too large as is the case typically for high pressure CVD. In practical CVD systems, both rate limiting phenomena are in play and the resulting process is a delicate balance between the two.

Another factor with chemical vapor deposition is that there is a fine line between etching of the substrate surface and growing of the film. Factors involved in this tight regime are reaction temperature and partial pressures of the reactant gases. Figure 2.4 presents a graph that depicts the regime of etching/deposition for Si growth via SiCl₄ in H₂ CVD. If the temperature of the reaction is too high, etching may occur, when in fact, one has intended deposition of a layer. When the partial pressure of the reactant species is large, the same principle can occur. As one can see, the process of growing epitaxial layers by the method of CVD is not trivial. There are many factors that need to be researched and experimented with to establish the optimum growth process.
Epitaxial growth is one of the most important factors for producing high quality devices. Using the CVD process, doping of the material is easily achieved by changing precursor flows and introducing gases that result in p-type or n-type doping. Doping of the material is used to change the electrical properties for different device applications. In the case of SiC, a p-type dopant (called acceptors because they accept electrons) is Al. When aluminum is incorporated into the reaction, the aluminum competes with the Si and then occupies a Si lattice site. With Al atoms in the material in the place of Si, the material becomes a p-type epilayer. Nitrogen is the predominant n-type dopant (called donors because they donate electrons). It behaves similarly to Al, only it competes with carbon. Site competition epitaxy is used as a precise means of doping control [19]. This method uses the control of the Si/C ratio to achieve the level type of doping needed. Since the dopants compete with the Si and C atoms for a place in the SiC lattice, precise control of Si/C enables doping control. Chemical vapor deposition provides the simplest way to dope epilayers. The material grown also results in high quality material which is
needed for devices. CVD reactors are commercially available and can produce high-quality material over large areas. The SiC CVD reactor used during this thesis research was constructed in-house and is now described in some detail.

2.2 USF SiC CVD Reactor

The reactor used for the experiments conducted in this thesis is a 75mm horizontal, cold-wall, low to atmospheric pressure chemical vapor deposition reactor. A similar reactor was previously built at Mississippi State University by Dr. Stephen Saddow and his former student Thomas Schattner [20]. At the University of South Florida (USF), a similar atmospheric pressure reactor was built by our group to accommodate wafers up to 75 mm in diameter. However, the susceptor design limits the maximum size wafer to 2” (50 mm) in diameter. Figure 2.5 shows a photograph of the reactor at USF and Figure 2.6 shows a sketch of the side view of reaction tube itself. A cooling jacket surrounds the inside diameter of the tube to keep the reactor cool (i.e. “cold wall”). The susceptor is heated by a radio frequency (rf) generator via the rf induction coil shown, which wraps around the reaction tube. The graphite susceptor is placed in the reactor on a quartz support (boat) in the center of the rf coil, upon which is placed the substrate.
Figure 2.5 Photograph of the USF 75 mm horizontal cold-wall reactor. Gases enter the reactor through a ¼” stainless steel gas line to the left and exit out of the system through the 2” exhaust, as shown. The quartz susceptor support (i.e. boat) and a susceptor are shown in the bottom of the photo for scale reference.
Figure 2.6 Side view of quartz reaction tube with the following details: (1) gas inlet, (2) quartz boat, (3) SiC coated susceptor, (4) gas outlet, and (5) cooling water jacket.

The mirror above the reactor in Figure 2.5 is used to aid in Si melt tests that are routinely conducted. Melt tests are used to determine the actual temperature on the susceptor surface compared to the reading from an infrared (IR) pyrometer; which reads the temperature on the back of the susceptor. This is performed by placing Si on the susceptor (or on a SiC wafer that is placed on top of the susceptor) and heating the susceptor until the silicon melts. At atmospheric pressure, the silicon melts at 1410°C. If the Si melts at a reading from the pyrometer of, say, 1390°C, then the appropriate adjustments to the set point temperature can be made to ensure the proper growth temperature is realized (in this case growth at 1580°C requires a set point temperature of 1560°C). The pyrometer is focused to the backside of the susceptor where a small indention is placed so accurate repeatable measurements are made. A cross-sectional view of the reaction tube is presented in Figure 2.7. The susceptor is placed on a quartz boat, which in turn is placed into the reactor. The quartz ribs shown in the picture are what support the susceptor.
Along with the reactor, there is a gas handling system and a process control system that are extremely important to the growth process. The process control system deals with controlling the process and ensuring proper safety precautions are applied which are needed for reactor operation. Reactor control is essential because repeatability is critical. Details of the control system are outlined in the thesis by Thomas Schattner [20].

There are three main functions to performing a growth run in the CVD reactor; reactor start-up, growth mode, and shut-down. The start-up and shut-down can be controlled automatically or manually. Start-up begins with an initial vacuum test to ensure that there are no leaks in the system. This test is done by checking to see if the pressure reaches below 500 mTorr. If this pressure is reached, then the start-up process can continue. This step is very important in that SiH$_4$ is pyrophoric, meaning it ignites spontaneously when in contact with air. Once the vacuum seal test has been conducted, a pump and purge cycle is initiated, either manually or automated. This cycle starts with a

Figure 2.7 Cross-sectional view of USF CVD reactor.
5 minute purge of Ar, followed by a sequence of pumping down the reaction tube, and then slowly back filling with $H_2$ until the tube reaches atmospheric pressure, and then repeats itself. The pump and purge cycle helps to eliminate contaminants, such as nitrogen, that are in the reaction tube and in the gas lines. Once the pump and purge cycle has finished, growth may be initiated. The details of the growth process in this thesis will be described in Chapters 3 and 4. The shut-down process may also be performed manually or automatically. The automatic process consists of a 30 second $H_2$ purge at the growth temperature, which purges the process gases from the reactor, followed by a 2 minute Ar purge, also at growth temperature, which anneals the sample. Then the rf generator is turned off to allow the sample to cool under Ar purge for 30 minutes. Both the start-up and shut-down are controlled by a programmable logic controller (PLC) which controls the gas valves directly. The growth mode, however, is manually controlled with the personal computer (PC). Labview is the program used to set the desired flow rates needed for growth. Switches on the control panel open and close the valves for the various process gases and mass flow controllers (MFC); meter the flow based on the labview settings. The rf generator is also controlled in this manner.

There are many sensors incorporated into the reactor and fed into the control system which ensure system safety during the growth process. When the sensors are activated, the system shuts down all gases and the heating source and Ar is purged through the reaction tube. The sensors for the control system include a hydrogen gas sensor, door sensor, and cold water jacket flow sensor. The fault of any of these sensors results in immediate system shutdown as noted above.
The gas handling system enables the gases to reach the reactor with high purity. A diagram of the overall system is given in reference [20]. Each gas has a separate welded stainless-steel line leading to a single gas manifold. This is a dual manifold system containing a vent and a process side. The vent side allows the gases to be vented without flow through the reaction tube, which allows the user to establish steady-state gas flow prior to growth. On the control panel, there are two different actuators for the gases, the “vent” gas actuators and the “process” gas actuators. The silane gas feed and hydrogen feed have additional features. The silane is connected to a separate purge system where Ar is used to purge the line to ensure that there is not any unwanted air in the line. The hydrogen line is connected to a palladium purifier, to purify the hydrogen above the VLSI grade. The purifier is kept at a temperature around 400°C, which allows the hydrogen atoms to diffuse through a Pd membrane and then on to the process. All of the items described in this section are necessary to have good quality control for epitaxial growth with the CVD method.

2.3 Lattice Mismatch of 3C-SiC on Si Substrates

As stated previously, the growth of 3C-SiC on silicon substrates does not presently result in device-quality epi because of the large lattice mismatch between SiC and Si. The problem with this type of growth is the film critical thickness, which is too thin for most applications. Since the lattice constant of the 3C-Si film does not match that of the Si substrate, strain in the layer occurs. When the growth exceeds a certain thickness, called the critical thickness, \( h_C \), defects are generated in the layer to relax the stress. In the extreme case the film may crack and peel off of the substrate. However the
usual case is that dislocations are generated which accommodate the strain energy in the film, but the films do not crack. Buffer layers are therefore used to provide closer lattice spacing for the epitaxial layer that is to be deposited. In some material systems, alloys can be formed which have the property that their lattice constant is a function of the alloy composition. In this way a buffer layer can be formed between two mis-matched crystals and the lattice constant graded accordingly. Unfortunately 3C-SiC does not alloy and this approach cannot be used to match the lattice constants of 3C-SiC and Si. Fortunately intermediate buffer layers may be used to grow 3C-SiC on Si substrates which, while they do not completely eliminate the stress in the film, reduce it somewhat.

There are two types of strain associated with lattice mismatch: tension and compression. Figure 2.8 shows examples of both tension and compression in an epilayer grown on a substrate of different lattice constant [21]. Compression occurs when the lattice of the epitaxial layer is larger than that of the substrate lattice - the epilayer tries to adjust to the size of the substrate lattice and must effectively shrink to do so. This causes the lattice of the deposited layer to be in compression in the growth plane while the lattice becomes elongated in the vertical direction and is thus in tension. When the film is in tension, the epitaxial layer lattice constant is smaller than the substrate lattice constant, causing the lattice of the deposited layer to expand horizontally (i.e. be in tension). The result is the lattice constant is reduced in the vertical dimension, as shown in the figure, and is thus in compression.
The lattice mismatch can be calculated by the following equation:

$$f = \frac{a - a_o}{a_o}$$  \hspace{1cm} (2.3.1)

where $a$ is the lattice constant of the film and $a_o$ is the lattice constant of the substrate [21].

The elastic strain energy is given by:

$$E_H = 2G \left(1 + \frac{?}{1 - ?} \right)hf^2$$  \hspace{1cm} (2.3.2)

where $G$ is the shear modulus (slope of the linear elastic region of the shear stress, shear strain curve), $?$ is Poission’s ratio (ductility), $h$ is the film thickness, and $f$ is the lattice mismatch given by (2.3.1). Note that the only controlled variable in this equation is the thickness of the film [21].

When the elastic strain energy exceeds the dislocation energy density, dislocations form. Therefore, when the critical thickness is exceeded, dislocations will
occur. In order to compute the critical thickness, the elastic strain energy must be set equal to the dislocation energy density. The dislocation energy density is as follows [21]:

\[ E_D = Gb^2/(8p\nu(2a)) \cdot \ln(h/b) \]

Where \( b \) is the Burger’s vector of the slip distance, \( a \) is the lattice constant, and \( h \) is the film thickness.

The equations can then be simplified to give an estimate of the critical film thickness, \( h_c \) [21]:

\[ h_c = a/2f \]

An example of a real crystal and that of an ideal crystal is given in Figure 2.9. As seen in the figure, the real crystal has an extra lattice site from the dislocation where the ideal crystal has no dislocation. The burgers vector for the real crystal is 1 because it has one more lattice point to travel in order to make a circuit about the dislocation (compared to the real crystal).

**Figure 2.9** (a) Elements of a dislocation between a real crystal (left) and ideal crystal (right). (b) Plot of critical thickness vs. lattice mismatch [21].
The graph of the critical thickness versus the lattice mismatch shows that the higher the lattice mismatch, the lower the critical thickness. This means that when the lattice mismatch is relatively high, as in the case of 3C-SiC on Si, the critical thickness is less which makes the dislocations more prominent. This is the main reason why novel substrates are needed for the growth of 3C-SiC on Si, which will be discussed in the next section.

2.4 Novel Si Substrates for 3C-SiC Growth

Growth of 3C-SiC on silicon produces defective material due to the large lattice mismatch (>20%) between Si and SiC as noted in the last section. However, this type of growth is very promising because of the properties of SiC, the high electron mobility and the inexpensive cost of the substrate material with large diameter size. In order for the material to be of device quality, methods were researched to reduce the planar defects caused by the Si/SiC interface mismatch. The methods in particular that this thesis focuses on are growth on porous Si, on undulant Si, and on silicon on insulator (SOI). This section of the thesis will discuss these techniques that many researchers have studied in an attempt to improve the 3C-SiC/Si growth system.

2.4.1 Porous Silicon

Porous Si as a compliant substrate has been investigated by researchers to produce high quality 3C-SiC material [11]. Silicon is made porous by an anodization process using hydrofluoric acid (HF) were the current, time and HF concentration controls the porosity and thickness of the pores [23]. Experiments described in the literature have
been conducted for the growth of 3C-SiC on porous Si with atmospheric pressure CVD using propane and silane as the precursors. The growth temperature was in the range of 1330 to 1350 °C resulting in a growth rate of 2 µm/hour. The compliant substrate was ~50% porous p-type silicon. A standard silicon substrate and a SIMOX substrate were included in the growth for comparison [11]. The experiment resulted in an improvement of the full width half maximum (FWHM) of the {200} reflection of SiC and {400} reflection of Si [11]. The authors of this paper believe that the reason for this improvement was that the pores acted like a dislocation filter, giving about a 50% improvement [11]. Scanning electron microscopy (SEM) was performed on the samples to give an overview of the morphology. The SEM images showed large rectangular terraces on the 3C-SiC grown on porous Si, but not on the 3C-SiC/SIMOX [11]; shown in Figure 2.10. They believe this is from the carbonization process of the initial porous layer. Micro-Raman spectra were also performed on these samples which concluded that there was approximately a 50% improvement in the interface relaxation comparing the porous Si substrate to that of the bulk Si substrate. Therefore, the experiments performed in this reference conclude that porous Si substrates give rise to an overall improvement in the epilayer quality compared to that of bulk Si substrates.
Another paper discusses the results from 3C-SiC growth on porous Si by way of a single precursor source with low-pressure CVD with a growth temperature of 1050 °C [24]. Transmission electron microscopy (TEM) diffraction patterns indicated a fully relaxed single crystalline 3C-SiC layer on Si. However, X-ray diffraction (XRD) showed the presence of a minute amount of different phases in the samples, which they believe is caused from the impurities of the precursor [24]. Atomic force microscopy (AFM) was also performed and indicated the surface morphology to be a rough surface caused by the surface roughness of the porous Si substrate [24]. Although the morphology is not of the highest quality, the relaxation of the 3C-SiC on the porous Si shows very promising results which could lead to device quality material.

2.4.2 Undulant Silicon

The Hoya Corporation developed a novel technique to reduce planar defects in 3C-SiC epitaxial layers on Si substrates [25]. The method strives to eliminate planar defects in the 3C-SiC layer on Si (001) substrates. Two types of planar defects result
from the mismatch of the SiC/Si interface, namely anti-phase boundaries (APB) and twin boundaries (TB). An APB is where there are two C atoms next to each other in the lattice structure when, in fact, there should be a carbon atom next to a Si atom. Twin boundaries are different stacking sequences of Si-C pairs. These defects usually propagate through the (111) planes when Si(001) substrates are used to minimize the defect propagation, however, planar defects still arise in the epilayers. Figure 2.11 show both twin boundaries and anti-phase boundaries. As seen from the figure (b), the APB’s propagate in the (1 1 1) plane. These may eventually be annihilated with continued growth as seen in the figure. The TB’s give way to different stacking sequences which are offset by roughly 60º from Figure 2.11(a). It has been determined that APB’s may also be eliminated by step flow epitaxy on misoriented Si(001) substrates, therefore, the main goal is to eliminate the twin boundaries [25].

![Figure 2.11 Illustration of crystal defects in 3C-SiC: (a) twin boundaries, (b) anti-phase boundaries [16]. These are the two dominant defect types in 3C-SiC grown on Si substrates.](image)
To eliminate the twin boundaries that propagate in the (111) plane, Hoya made Si (001) substrate surfaces to form countered slopes oriented in the [110] and [-1 -1 0] directions which they call “Undulant-Si” [25]. The entire surface of the substrate is covered with these oriented undulations, where the ridges are aligned in the [-1 1 0] direction as shown in Figure 1.3.

Experiments were performed by Hoya on misoriented (4º towards the [110] direction), well-oriented Si and undulant Si for comparison. The undulant Si was prepared by scraping 15 µm diameter diamond slurry across the surface in the [-1 1 0] direction resulting in continuous ridges in the [1- 1 0] direction [25]. The surface was then oxidized with a 200 nm oxidized layer in dry oxygen to remove any crystal defects caused by the scraping process. The oxide was then removed with a 5% solution of HF. The ridges developed in this process had a ridge to ridge spacing between 400 and 700 nm with ridge to valley heights of 7 to 26 nm which were determined from atomic force microscopy (AFM) [25]. Once the undulations were created, epitaxial growth of 3C-SiC was performed which took place in a cold-wall low-pressure CVD reactor. First, a carbonization step took place to convert the Si surface into SiC using 10 sccm of C₂H₂ and 100 sccm of H₂ for 5 minutes. Growth then proceeded at 1350ºC and 100 mTorr for 5 hours with flow rates of 50 sccm of SiH₂Cl₂, 10 sccm of C₂H₂, and 100 sccm of H₂, which resulted in 200 µm epitaxial 3C-SiC layer [25].

Before examining the growth of the epitaxial layers, the Si substrate was removed from under the 3C-SiC layer by a HF+HNO₃ solution. Optical micrographs of the growth of 3C-SiC on the well-oriented Si substrates showed a mosaic like morphology that had adjoining structures rotated 90º from each other, suggesting a high APB density.
As for the 3C-SiC grown on off-oriented Si substrates, scale-like steps oriented at an obtuse angle in the [110] direction were seen, demonstrating APB elimination [25]. However, to determine if the TB’s were eliminated, the 3C-SiC was etched in molten KOH for 5 min. After the etching process, the surface of the epilayer had a high density of etch-pits which were similar to the scale-like stepped morphology after growth. This led to the conclusion that there were still twin boundaries in the epitaxial layer. Unlike the well-oriented and misoriented Si substrates, the undulant Si substrate 3C-SiC morphology had a mirror-like surface in which the undulations were observed on the backside of the sample. The undulant Si resulted in elimination of both anit-phase boundary and twin boundary defects. The surface of the 3C-SiC grown on undulant Si was etched in molten KOH and resulted in no etch-pits [25]. Figure 2.12 demonstrates how the undulating substrate eliminates both planar defects.

![Figure 2.12](image)

**Figure 2.12** Elimination of twin boundaries using undulant Si technology. Cross-sectional structure of 3C-SiC changes from (a) to (c) as growth proceeds [25].
The anti-phase boundaries are eliminated due to the slope of the undulant surface. The twin boundaries continue to propagate as shown in Figure 2.11(b). However, with continued 3C-SiC growth and increasing film thickness, the defects eventually eliminate each other. Hoya Corporation has developed a method that eliminates both types of planar defects caused by the SiC/Si interface mismatch. With this technique, high quality, free standing 3C-SiC material has been produced from low-cost, large area, Si substrates.

2.4.3 Silicon on Insulator (SOI)

The growth of 3C-SiC on SOI, or ceramic, substrates is very promising due to the possibility of high temperature growth which should result in superior epi quality. Not only is there a lattice mismatch between Si and SiC, there is a thermal expansion mismatch (~8%) which also results in dislocations [14]. The ceramic substrate matches the lattice constant of the 3C-SiC film grown from the thin Si layer, which enables the thermal stresses to be negligible [26]. These substrates are also low cost and have large surface areas (>4”) which may be polished to a fine finish. The polycrystalline substrates were grown by a bulk commercial CVD process. A Si film of about 175 Å thickness was then bonded to the surface at the Naval Research Laboratory. Unfortunately, silicon voids resulted from the bonding procedure. Figure 2.13 shows a sketch of the cross section of the SOI substrates studied here.
Figure 2.13 SOI substrate for growth of 3C-SiC. 175 Å of Si bonded to polycrystalline SiC [14].

Once the SOI substrates had been diced and RCA cleaned, an initial carbonization step preceded at 740 Torr, 1230°C for 20 seconds in a 10 sccm propane flow (3% in hydrogen) [26]. Growth from 5 – 60 minutes then took place at temperatures between 1380 and 1400 °C at flows of 15 sccm of propane (20% in hydrogen) and 50 sccm of silane (5% in hydrogen) at a pressure of 200 Torr. Once there was an initial SiC film, high temperature growth took place up to 1550°C. During the carbonization step, if the temperature was too high, the silicon layer would be completely etched and the growth would produce polycrystalline films. When the temperature was increased to the growth temperature, the propane was introduced to prevent etching of the thin SiC layer, which was produced during the carbonization step. RHEED was conducted during growth and suggested that the 3C-SiC material grown was single crystal. SEM micrographs showed island-like structures that may be caused by anti-phase boundaries which may be eliminated by growth on off-axis Si substrates [26]. The growth process of 3C-SiC may be conducted from SOI substrates giving way to single crystal SiC. This process is favorable due to the high growth temperatures which may be achieved to produce high quality material. It should be emphasized that this reported work was performed on on-
axis oriented Si films; the work performed in this thesis, and presented in Chapter 4, is of a similar nature but on off-axis (i.e., vicinal) Si films.

### 2.5 Summary

Many different growth techniques may be used to produce epitaxial layers of silicon carbide. However, the most useful and effective is chemical vapor deposition (CVD). CVD gives way to ease in doping which is needed for different applications of the material. The experiments performed in this thesis use a cold-wall horizontal low to atmospheric pressure CVD reactor to grow 3C-SiC films on Si (001) substrates. Processes were developed during this thesis research to enable the growth of reasonable quality 3C-SiC on Si at both atmospheric pressure (Chapter 3) and low pressure (Chapter 4). With the lattice mismatch between Si and SiC being so high, the use of novel substrates is needed to produce device quality 3C-SiC material. There are many novel substrates which may result in higher quality grown films of 3C-SiC than bulk Si substrates. These types of substrates are important for the improvement of 3C-SiC in order for the material to someday be of device quality. Now that the motivation for these novel substrates has been provided, results from experiments performed during this research on novel Si and SOI substrates will be presented in Chapters 3 and 4.
CHAPTER 3
APCVD PROCESS DEVELOPMENT

3.1 Carbonization of Si(001)

The traditional growth of 3C-SiC on bulk Si consists of three main steps: (1) a native oxide etch using H₂, (2) a carbonization step which converts the Si surface to SiC, and (3) growth of 3C-SiC. The native oxide etch has been shown in the literature to be a necessary step prior to carbonization in order to grow 3C-SiC [1]. The carbonization step to convert the Si surface into SiC has also been shown to be a key step to produce good morphology in the final 3C-SiC film. The surface of the silicon substrate has dangling Si bonds where the carbon can attach to form SiC. This layer acts like a buffer layer to aid in stress reduction for the growth at the SiC/Si interface, however, defects still occur from the large lattice mismatch as discussed in Chapter 2. The first carbonization process performed for the work presented in this thesis was taken from the literature [13]. Based on this, the process was optimized for our reactor until the best morphology was produced. This was performed by changing the propane flows and the temperature at which the carbonization step took place. Before the carbonization took place, a hydrogen etch step was performed to remove any native oxides that developed on the Si substrate. The etch process is sensitive to temperature and time of etching, especially when the temperature is very close to the Si melting point of 1410°C. An example of what can go wrong with too aggressive an etch step is the formation of etch pits as shown
in Figure 3.1. Notice how the pits are square and they are oriented in the [111] direction of the cubic structure.

![Figure 3.1](image1.png)

**Figure 3.1** Optical micrograph of etch pits produced from the H\(_2\) etch step of the Si substrate. Sample No. USF-02-111. T = 1050°C for 10 minutes, P = 760 Torr.

To perform carbonization of the Si substrate, a Si(001) wafer was initially cleaned using the RCA process and then set on top of a SiC coated graphite susceptor, which was placed into the CVD reaction tube. The carrier flow was then set to 4.5 slm of H\(_2\) in which the temperature was brought to 1050°C for 10 minutes with rf induction heating with a process pressure of 760 Torr. This temperature did not produce any etch pits and was the temperature adopted for the H\(_2\) etching process at atmospheric pressure. After 10 minutes of H\(_2\) etching, the rf generator was turned off to let the sample cool for 5 minutes. Propane was then added to the carrier gas flow for 1 minute, at which time the temperature was ramped up to the carbonization temperature of 1050°C. Carbonization then took place for two minutes after which the rf generator was shut off and the sample was cooled for 25 minutes under an Ar purge. The flow of propane for the carbonization
step was initially set for 20 sccm (3% in hydrogen), but changes were needed to improve the morphology. A flow of 50 sccm of C\textsubscript{3}H\textsubscript{8} (3% in hydrogen) resulted in the best morphology and was used for the rest of the AP experiments. The morphology of the samples were viewed to determine which carbonization flows gave the best morphology by way of optical microscopy. Figure 3.2 shows the APCVD process flow for the carbonization of Si developed during this thesis research.

![APCVD carbonization process flow](image)

**Figure 3.2** APCVD carbonization process schedule including the initial etch step. A propane flow of 50 sccm (3% in hydrogen) was determined to yield the optimum buffer layer morphology. The H\textsubscript{2} carrier flow was 4.5 slm.

Once the carbonization step was optimized, growth of 3C-SiC could be initiated. This is discussed in the next section.

### 3.2 3C-SiC Growth on Si(001)

The growth of 3C-SiC on Si(001) could proceed once the carbonization step had been used to convert the Si surface to SiC. After the carbonization step, the temperature was directly raised to the growth temperature. As with the etch step and carbonization
step, the flow rate and temperature determine the quality of the film. Many experiments were conducted to achieve the best 3C-SiC film morphology. The APCVD growth process schedule developed during this phase of research is shown in Figure 3.3. As shown in the diagram, the temperature is ramped to the growth temperature after carbonization has been performed. One minute after reaching the growth temperature, the silicon precursor, 3% silane in hydrogen, was introduced into the gas flow and the propane was reduced to the designated growth flow rate; 3C-SiC growth now occurs. After growth, all gases were shut off except $H_2$ for 30 seconds. Ar was then introduced and, after 2 minutes of an anneal at the growth temperature, the rf heating was terminated and the sample cooled under Ar purge.

![Figure 3.3](image)

**Figure 3.3** APCVD process schedule developed for growth of 3C-SiC on Si(001). The flow rates during growth are as follows: $H_2$: 4.5 slm, $C_3H_8$: 20 sccm, $SiH_4$: 20 sccm.

Experiments were conducted and the morphology was studied from observations under the SEM. The first experiments used flow rates of propane and silane of 15 and 15 sccm (both 3% in hydrogen), respectively. A series of runs were performed at different flows during growth for silane and propane which were: 15 and 15, 20 and 20, and 25...
and 25 sccm. Figure 3.4 shows SEM results of the morphology for each set of flows. As seen in the figures, the middle micrograph (b) has the best morphology. Compared to the other two samples, the surface is much smoother in between the mosaic structures that were observed on all of our films. Not only were the flows varied, but the growth temperature was also changed to produce the best morphology. The experimental growth temperatures ranged from 1350 - 1370°C. It was determined that 1350°C was the optimum growth temperature for 3C-SiC on Si(001) at atmospheric pressure in our cold-wall reactor.

**Figure 3.4** Plan view SEM micrographs of 3C-SiC grown on Si(001) for various flow rates. Sample ID’s are USF-02-122, USF-03-031, USF-03-026 respectively. Note USF-03-031 has the best morphology. The top corner numbers represents the carbonization flow rate: growth flow rates for silane/propane. The film thickness is also indicated, as determined by cross-section SEM investigation (not shown).

The samples were not only characterized by scanning electron microscopy (SEM), but also via XRD and TEM (including selective area diffraction (SAD)). These studies were performed by Dr. V. Krishnamoorthy of UOE and Dr. T.S. Kuan of SUNY-Albany, respectively. Figure 3.5 shows some of the TEM and SAD data on a 3C-SiC
sample grown on Si(001). Notice in the TEM image that, at the interface of the 3C-SiC and Si, there are a substantial amount of defects. This is the direct result of the stress caused by the lattice mismatch between Si and SiC. As the growth proceeds and thicker and thicker films are grown, these defects become less prominent. If further growth had occurred, then there theoretically would be even less defects at the surface of the film.

Looking at the SAD data shown in Figure 3.5, the spots shown are a clear indication that a good single-crystal film has been grown. The diffraction spots corresponding to 3C-SiC and Si are as indicated. SAD gives an inverse spacing of the diffraction spots from each lattice, with the larger lattice constant having spots closer spaced together. The SAD data also shows that the Si(001) is parallel to the SiC(001) and the SiC<110> is parallel to the Si<110>. There is also nearly a 25% relaxation of the misfit strain. All data analysis performed by Dr. Kuan.

![Figure 3.5](image)

**Figure 3.5** (a) Cross-section TEM data of 3C-SiC grown on Si(001), (b) SAD data of 3C-SiC grown on Si(001). Sample ID USF-03-031A. Film thickness is 4.3 µm.
XRD was performed on sample USF-03-031A which is shown in Figure 3.6. This sample was grown by the process depicted in Figure 3.3 with the precursor flows of 20 sccm (3% in hydrogen) for both silane and propane. The omega-2-theta scan confirms the TEM data shown in Figure 3.5. The film is single crystal with some mosaic structure. The peaks are narrow and sharp indicating good quality and the SiC(400) is parallel to the Si(400) indicating the film was epitaxially grown.

**Figure 3.6** XRD data of 3C-SiC grown on Si (001). Sample ID USF-03-031A, a 4.3 µm film grown in 2 hours. The equipment used was a Phillips MRD System, CuKa source, Dumond Monochromator.

The first 3C-SiC process development steps were conducted on TaC coated graphite susceptors. This was done since TaC coated graphite has a longer useful time than SiC coated parts (tens of hours for TaC vs. 10 hours maximum for SiC). Hence the development of a 3C-SiC/Si process on TaC would have long-term process stability and cost advantages of SiC. Unfortunately, when the process temperature was raised to
around 1200°C, the sample reacted with the TaC. While Si and TaC do not react, residual Ta on the surface of the TaC coated part does. As a result, a eutectic formed between the Ta and Si at this temperature. The Si reacted with the Ta and an alloy was formed that was not removable. Therefore, the SiC coated susceptor could only be used for the growth of 3C-SiC on Si if the Si substrate is to be placed directly onto the susceptor. In the future work section of this thesis (Chapter 5), plans for safely growing 3C-SiC on TaC coated graphite will be discussed. Simply stated, an intermediate material, such as poly-crystalline SiC plate, must be placed between these two materials to prevent a reaction from occurring. From the results shown in this section, a stable APCVD 3C-SiC/Si process was developed with acceptable film morphology. However, more experiments were conducted in order to reduce the dislocations created by the lattice mismatch at the interface between the SiC and Si. The next section describes a process developed for 3C-SiC growth on porous Si substrates.

3.3 3C-SiC Growth on Porous Si

Silicon substrates may be made porous by an anodization process [27]. A silicon p-type wafer is placed in an electrochemical cell containing an aqueous hydrofluoric acid (HF) solution in which the Si wafer is the anode and a Pt wire is the cathode [27]. One process reported in the literature involves a solution of DI wafer which contains ethanol and 100% hydrofluoric acid with a ratio of 1:2:1 [27]. Current is applied to the cell and the HF ensures the dissolution process of crystalline Si while the ethanol improves the penetration of the etchant into the pores [27]. Many parameters may be adjusted to provide different types of pores such as: anodization time, current density, etching
solution composition, wafer type, doping level, and exposed area [27]. For p-type wafers, since there is an abundance of holes present, the anodization takes place in the dark and is performed with a constant current source. Many types of pores result from the anodization process depending on the anodization conditions.

The University of Pittsburgh provided porous Si samples for this research under the ONR DURINT program [28]. Some examples of the pores experimented on during this thesis are shown in Figure 3.7. Notice that in Fig. 3.7(a) the surface contains pores that are both square and circular in nature. In Fig. 3.7 (b), all of the pores are circular in shape. Fig. 3.7 (c) shows that there may be two different types of porous morphologies on one sample. The top portion of the micrograph shows a porous structure that appears to be sporadic in structure as though it has 3D features. However, the bottom portion of the micrograph shows square pores imbedded in a pattern with large circles. Indeed this is an example of a star-like porous morphology which is typical for high current anodization processing in Si [29]. Clearly different types of pore morphology may produce different morphologies of 3C-SiC films during growth. Exactly which structure will yield the optimum film requires experimental investigation, which we have only begun to carry out during this thesis research and are continuing under LPCVD conditions.
Figure 3.7 Plan view SEM micrographs of some porous Si prior to growth. (a) Sample ID: PS #14, (b) Sample ID: PS #16 and (c) Sample ID: PS #8. Porous Si samples provided by Prof. W. J. Choyke, University of Pittsburgh.

The pores are not only at the surface of the silicon wafer, but the pores penetrate about 10 - 15 µm into the substrate. Figure 3.8 shows a cross-sectional SEM micrograph of the porous material. A 3C-SiC film (USF-03-067E) was grown on the substrate which is on top of the porous Si substrate. As shown in the figure, the pores penetrate into the bulk of the Si to a depth of ~ 12 µm.
Figure 3.8 Cross-sectional SEM micrograph after 3C-SiC epi growth on porous Si. Note the pores have penetrated into the Si bulk approximately 12 µm. A 3C-SiC film of ~16 µm was grown on this Si(001) substrate and contains a very sharp interface with the porous Si surface. Sample ID USF-03-067E.

Once the porous Si had been made, growth of 3C-SiC growth studies were conducted. The growth procedure for porous Si was basically identical to that of standard Si, however, the H$_2$ etch step process time was reduced to two minutes from ten minutes which is standard for bulk Si substrates. The etch was only performed for two minutes to reduce etching of the porous network. However, there is believed to be significant pore modification during the entire growth process as has been the case in porous SiC [30]. When the pores are heated, they begin to modify and enlarge. This might be because larger pores are at a lower energy state than the smaller pores [31]. Further investigation of pore modification of porous Si during growth is being conducted in our laboratory and will be reported at a later date.

The etch and carbonization steps were conducted in the same manner for all of the experiments performed in atmospheric pressure for growth of 3C-SiC on porous Si. That is, the hydrogen flow rate was 4.5 slm for 2 minutes while the carbonization step
introduced propane at 50 sccm (3% in hydrogen). However, for the precursor flow rates during growth, all of the experiments were the same except one. The flow rates of the precursors of propane and silane were both 20 sccm (3% in hydrogen). The one experiment that was changed was for precursor flow rates of 25 sccm (3% in hydrogen) for both silane and propane. This was done to determine if the growth rate would increase and/or the growth would result in a better film morphology. The sample had a rough morphology and was not believed to be single crystal, as determined from SEM study. Therefore, the rest of the experiments conducted for atmospheric pressure on porous Si had precursor flow rates of 20 sccm (3% in hydrogen).

One type of porous Si substrate not presented in Figure 3.7 had two different morphologies which are shown in Figure 3.9(a). As shown in the top high-magnification micrograph, the surface has a pore structure of a cross-hatched ‘star pattern’ nature while the bottom high-magnification micrograph shows that the structure inside the circular region contains square pores. 3C-SiC was grown on this sample and the corresponding SEM micrographs are presented in Figure 3.9(b). The morphology of the growth performed on the square pores is substantially better than that grown on the cross-hatched pores. Unfortunately, only the small spot shown in Figure 3.9(b) contained the square pores for the entire 1cm² sample. As a direct result of this experiment the University of Pittsburgh has been working to develop a porous Si process to produce the square pore structure over the entire wafer.
Figure 3.9  Plan-view SEM micrographs of (a) porous Si prior to growth (Sample ID: PS #7) and (b) 3C-SiC grown on the porous Si shown in part (a) (Sample ID USF-03-033A). Note the superior film morphology grown in the circular region of (a) containing square pores.

Low temperature photoluminescence (LTPL) and TEM were performed on the sample shown in Figure 3.9 at the University of Pittsburgh and the State University of New York at Albany (SUNY-Albany), respectively. These data are presented in Figures 3.10 and 3.11. Originally, it was thought that this sample showed a reduced defect density by an order of magnitude (i.e., X10) compared with a Si(001) control sample. However, it was later found that no such assessment may be made due to differences in the epi layer thickness. In addition, while the LTPL investigation indicated the 3C-SiC was of reasonable quality, the doping density was too high to make any quantitative assessments. One reason for these somewhat disappointing results may be that the small spot of the sample with good morphology is so minute compared to the rest of the sample that the TEM and LTPL data were most likely from the surrounding ‘poor’
morphological regions. If more porous Si of the square type were produced, the results might indicate a high quality film of 3C-SiC with superior properties to the Si(001) control.

Figure 3.10 LTPL data from USF-03-033A (standard Si), USF-03-033B (porous Si).

Figure 3.11 TEM data from USF-03-033B (porous Si) showing the defect network in the film. Note the defect density improves as the film thickness increases.
The main focus for future experiments on porous Si are to reproduce the square porous Si structure shown in Figure 3.9(a) within the circular region, lower the doping of the grown films via an adjustment of the Si/C ratio, and to grow thicker films to permit more accurate LTPL assessment of the film quality with minimum influence of the interface region. More work completed is described in Chapter 4 along these lines.

3.4 3C-SiC Growth on Porous 3C-SiC Substrates

The final set of novel samples studied during this thesis under APCVD conditions involved free-standing 3C-SiC substrates provided by Professor Choyke from the Hoya Corporation [32]. These novel substrates were made using two separate processes. First, thick (>200 µm) 3C-SiC was grown on undulant Si substrates which have been described in Chapter 2, section 2.3.2. After the growth was performed, the Si substrate was removed and the backside polished, leaving a free-standing 3C-SiC substrate which is yellow in color. The substrate was then etched in a solution of HF+HNO₃ to prepare it for epitaxial growth [32]. Figure 3.12 shows the process flow developed by Hoya to produce free standing 3C-SiC substrates.
Figure 3.12 Process developed by Hoya Corporation to produce free-standing 3C-SiC from 3C-SiC grown on undulant Si substrates [33]. Image courtesy of Dr. H. Nagasawa.

The University of Pittsburgh received some of these samples from Hoya and provided both bulk and porous versions to our group for 3C-SiC epitaxial growth studies. For the porous layers developed at Pittsburgh, anodization took place to make the free-standing 3C-SiC porous.

The free-standing porous 3C-SiC was then RCA cleaned and loaded into the CVD reactor on a SiC-coated graphite susceptor. Since the goal was to grow a homo-epitaxial film, there was no need for the etch and carbonization steps. Instead, the growth proceeded more along the lines of homo-epitaxy of SiC [34]. A process flow for the growth is shown in Figure 3.13. After the sample was loaded into the reactor, hydrogen
and propane flows of 4.5 slm and 20 sccm (3% in hydrogen), respectively, were initiated. The temperature was ramped until the growth temperature of 1350°C was achieved. After 1.5 minutes at the growth temperature, silane was introduced at a flow rate of 20 sccm (3% in hydrogen). Growth occurred for 5 hours at which time an Ar purge was started and the rf heating turned off.

![Figure 3.13](image)

**Figure 3.13** Process flow developed for growth of 3C-SiC on free standing porous 3C-SiC. The flow rates during growth are as follows: $\text{H}_2$: 4.5 slm, $\text{C}_3\text{H}_8$: 20 sccm, $\text{SiH}_4$: 20 sccm.

The samples were examined under the SEM to determine the morphology of the resulting epi film. Figure 3.14 presents a SEM micrograph of 3C-SiC grown on free standing porous 3C-SiC. Part (a) of the micrographs shows a plan view image where the center portion may be a portion of the porous substrate where either film growth did not occur, or it may be a polycrystalline film in nature. Part (b) of the figure is the same image, only with a sample tilt to give a better view of the film depth. Note that the film surrounding the center appears to be of reasonable morphology.
Figure 3.14  SEM micrographs of 3C-SiC grown on free-standing porous 3C-SiC (P-3C). (a) Plan view image of sample. (b) SEM image with sample tilted. Sample ID: USF-03-040B. Center region appears to be where a single crystal 3C-SiC film did not grown properly and is likely polycrystalline.

The growth of 3C-SiC on free-standing porous 3C-SiC substrates is one method that may produce device-quality 3C-SiC films. Since the growth is homoepitaxy, the 3C-SiC film should have less defects and, with longer growth runs, even fewer epi defects should be in the film. However, more experiments need to be performed in order to determine whether this process actually produces such film quality. Indeed this work has been continued by Shailaja Rao of our group since it involves homo-epitaxy and not hetero-epitaxy, which is the focus of the research described here.

3.5 Summary

There are many different processes that have been developed during this thesis research in an attempt to reduce defects in 3C-SiC films grown on Si substrates. The different processes are all attempting to solve the same problem, namely reducing defects
in the epi layer by altering the 3C-SiC/Si interface. However, all of these methods attempt to solve this problem in a different manner. The growth of 3C-SiC on standard Si has been studied and a process has been developed to produce reasonable quality epi during this thesis. Growth on porous Si was also initiated to determine if there is any chance to reduce planar defects using this approach. While the result of these preliminary experiments is promising, more studies need to be conducted in order to produce solid evidence of high quality films. The main outcome of this early work has been the discovery that square porous structure seems to yield the best epi morphology. This work is continuing under low-pressure CVD (LPCVD) conditions, the subject of the next chapter. Growth on free-standing porous 3C-SiC fabricated using undulant Si technology was also researched. These findings indicate as well that more process development is needed to produce device quality films. This latter research, being homo-epitaxial in nature, has been transitioned to the homo-epitaxial growth team led by Dr. Saddow. In all, many experiments were performed to give a baseline atmospheric process for these types of substrates which prove to be promising materials. Once LPCVD was available, all efforts switched to this superior growth environment, which is now discussed in the next chapter.
CHAPTER 4

LPCVD PROCESS DEVELOPMENT

4.1 LPCVD Reactor Hardware Development

The horizontal cold wall reactor at the University of South Florida, as stated in Chapter 2, was originally designed for atmospheric-pressure (AP) operation. The system was later upgraded so that CVD growth could be conducted in the low pressure (LP) regime (50-150 Torr). The design of the low pressure system is described in detail in reference [35] and the reader is referred to the reference for more details. While the initial LPCVD hardware was implemented beyond the scope of this work, a viable LPCVD process was not developed. Therefore some important LP system adjustments were made to the system in order to produce a suitable operating pressure for CVD growth of SiC, both on SiC substrates and on Si, the later being the focus of this thesis. These critical LP system adjustments will be discussed in the following subsections followed by the experimental results that were accomplished with the modified LPCVD system during this thesis research.

4.1.1 150 Torr Modification

The first set of experiments with the low pressure system were homo-epitaxy growths on 4H-SiC. The pressure could not be established above 50 Torr for these experiments which resulted in large temperature gradients on the growth surface, as
determined from the epi samples having huge thickness non-uniformities [31]. After consultation with Dr. Olle Kordina of Caracal Semiconductor, the pressure was increased to 150 Torr by introducing Ar into the vacuum system downstream of the process, but upstream of the pressure control throttle valve. A photograph of the LP hardware, including the gas inlet implemented to increase the system pressure, is shown in Figure 4.1. Initially Ar from a class A cylinder was used as the inlet gas, but due to excessive gas consumption, the Ar feed was replaced by house N\textsubscript{2} to save cost and reduce bottle swapping. The N\textsubscript{2} flow is metered by a ball valve which must be manually set to allow the desired operating pressure to be controlled for the process gases used. By controlling the amount of nitrogen flow into the vacuum system, the pressure may be controlled properly. In addition to the nitrogen gas inlet, a second modification was made as shown in the figure. A constriction in the vacuum line, implemented via a 6” length of 3/8” stainless steel flex tubing, further reduced the pumping throughput and aides in increasing the system pressure. This constriction was placed in-line with the poppet valve but not between the rough valve (used to perform pump and purge pre-growth processing) and the pump. Hence process time for the pump and purge step was not affected, only process pressure during growth under LP conditions, as desired.
**Figure 4.1** Reactor LP hardware implemented in [35] and modified here to achieve proper LPCVD operation. The tube exhaust is shown along with the location of all changes made during this thesis research.

A 150 Torr CVD process for homoepitaxy was developed during the summer of 2003 by Dr. Saddow, therefore, the LPCVD 3C-SiC on Si process was developed at 150 Torr. The flow rate used for the growth was initially 4.5 slm as for the atmospheric pressure process; however, the pressure did not reach 150 Torr if the nitrogen ball valve was left in the position established for homo-epitaxial growth. Therefore the flow rate for the 3C-SiC/Si process was increased to 9 slm of carrier gas (H₂) to ensure the 150 Torr pressure could be controlled without constant re-adjustment of the nitrogen flow when the system was used for homo-epi or hetero-epi (i.e., 3C-SiC/Si) growth.
4.1.2 Gas Jetting Modification

It had long been suspected that the gas inlet to the AP reactor was ‘jetting’ and this problem needed to be addressed. Gas jetting is a situation whereby laminar flow is not possible due to a non-uniform injection of the process gases into the growth vessel. This can be detected in several ways, but the most obvious is the pattern of SiC deposit on the reaction tube walls. For a symmetrical input/output to the tube, the flow pattern on the tube walls should be symmetrical. Clearly it was not, even under APCVD conditions, and this problem became intolerable when LPCVD process development was initiated. A simple fix to this was to install a diffuser to force the gas to quickly expand in the tube and allow laminar flow to be established. Figure 4.2 shows the diffuser implemented during this work to correct the gas jetting problem. It is a thin stainless-steel plate consisting of 750 µm holes uniformly distributed across the face of the plate. The diffuser was installed so that it was approximately 2 cm from the gas inlet. The process gases then can flow through the holes but also around the plate near the tube walls. Once the diffuser was installed immediate and dramatic improvement in both the epi layer thickness uniformity and the tube wall deposit were observed. This represented the last reactor modification that was needed to establish a LPCVD process for 3C-SiC/Si growth. Now the development of various processes on novel Si substrates will be discussed.
Figure 4.2 Photo of gas diffuser installed during this research to eliminate gas jetting in the reactor. The diffuser is a thin stainless steel plate with 750 µm holes across the surface.

4.2 Carbonization of Si(001)

As with atmospheric pressure process development, low pressure process development of 3C-SiC on Si substrates first began with studying the carbonization step before growth could proceed. This was to ensure that each step of the growth process was developed properly. Initially, a hydrogen etch was performed to give the best looking morphology. The samples were viewed under the optical microscope to see if etch pits existed on the sample. When there were no longer any etch pits, then the hydrogen step was declared to be optimized. The hydrogen etch took place under atmospheric pressure since there was already an etch step developed for the AP process. However, pits still were produced on the surface. The etch step experiments were performed between 1015 – 1050 °C and between 2.5 – 10 minutes, all with a hydrogen flow of 4.5 slm. The flow was later increased to 9 slm of hydrogen so that the nitrogen line into the vacuum system did not have to be adjusted for the homo-epitaxial runs.
performed by the SiC group. The hydrogen etch step that produced the best results were a flow of hydrogen of 9 slm at 1000°C for 10 minutes.

Once the hydrogen etch process step was established, the carbonization step was studied to produce the best looking morphology. Many experiments were performed using different temperatures for the carbonization step. The initial carbonizations were conducted with the flow of hydrogen being 4.5 slm. The temperatures tested varied between 1000 – 1050°C with a flow of propane at 50 sccm (3% in hydrogen). When the hydrogen flow was increased to 9 slm, the propane flow was doubled to give a flow rate of 100 sccm (3% in hydrogen). The carbonization step that provided the best morphology was at a temperature of 1050°C, in which the carbonization step took place for 2 minutes. A process flow for the carbonization process described above is shown in Figure 4.3. The pressure for the hydrogen etch was 760 Torr, while the carbonization took place at 150 Torr.

![Figure 4.3 Carbonization process flow initially used under APCVD conditions. The H₂ etch and carbonization steps were performed at a pressure of 760 and 150 Torr, respectively.](image-url)
It was later discovered that the carbonization step could be performed by introducing the propane and directly increasing the temperature to the growth temperature (i.e., skipping the temperature step at the lower temperature for 2 minutes prior to heating up to the growth temperature). During carbonization process development, samples were observed under the SEM to determine the resulting morphology. Figure 4.4 shows an SEM image after carbonization in which there was an initial 10 minute hydrogen etch at 9 slm. After cooling, propane was introduced for one minute before raising the temperature to the growth temperature of 1380°C. The resulting morphology may be showing the initial SiC layer that has a mosaic structure (shown in the higher magnification image). The pressure was set for 150 Torr for the entire process and the carbonization took place only while increasing the temperature to the growth temperature. The process flow diagram is shown in Figure 4.5.

Figure 4.4 SEM micrographs after carbonization of Si(001). Sample ID: USF -03-166. The resulting morphology is mosaic in nature indicating that the surface may be converted to 3C-SiC, as expected. Process pressure = 150Torr, $H_2 = 9$ slm and $C_3H_8 = 50$ sccm (3% in hydrogen).
The process flow shown in Figure 4.5 gave way to the best results for the carbonization step and was therefore used for the rest of the 3C-SiC/Si growth experiments. This was not discovered until late in the research, so the initial growth processes under LPCVD used the carbonization process shown in Fig. 4.3. Once this was discovered, the only changes from this process were temperature changes resulting from the melt tests and flow changes to yield the best morphology. The next section will describe the growth step completed after the carbonization step had been performed.

4.3 3C-SiC Growth on Si(001)

As stated previously, the carbonization step that directly proceeded to the growth temperature was not discovered until late in the research. Initially, the growth process started with a hydrogen etch step for 2.5 minutes because, at the time, this did not produce any etch pits. This was followed by a carbonization step for 2 minutes, then the growth step was conducted. The first growth experiments were conducted to determine which flows resulted in SiC deposition on the reactor walls. When deposition was
observed, the actual flow rates were adjusted until 3C-SiC films were observed under the SEM. The flows that gave way to deposition during growth were 70 sccm (3% in hydrogen), for both propane and silane. With this knowledge, experiments were conducted with propane and silane flows being 10 sccm below this value to determine which produced the best morphology and the highest growth rate; the best was 70 sccm (3% in hydrogen) for silane and propane giving a growth rate of ~2 µm/hr. The morphology of this experiment is shown in Figure 4.6. As seen in the micrograph, white spots cover the entire sample. These are 3-D SiC features or ‘towers’ which may be nucleation sites related to pits in the original carbonized surface (see Fig. 4.4). However, the film morphology in between these 3-D towers is excellent. Therefore, the next step was to reduce and/or eliminate these towers. For this sample, the hydrogen etch step took place for 2.5 minutes with a flow rate of 9 slm under AP conditions. The carbonization step took place for 2 minutes with propane at a flow rate of 100 sccm (3% in hydrogen) occurring at LP conditions.

Figure 4.6  SEM micrograph of 3C-SiC/Si morphology for growth at low pressure. Sample ID: USF-03-139. Growth for 1 hour produced a 2 µm film as determined by cross-section SEM (not shown). White dots are 3-D SiC features (towers) on the surface.
Experiments were conducted to reduce the amount of 3-D features on the 3C-SiC surface grown on Si(001) under LPCVD conditions. First, the hydrogen etch step was increased in time to 10 minutes instead of 2.5 minutes (which is the original 3C-SiC/Si process) to ensure the native oxide was indeed removed. This gave way to a lower density of towers, but still more experiments were needed to reduce them further. The carbonization step described in section 4.2 was used, were the carbonization took place while raising the temperature directly to the growth temperature after sample cooling which was after the hydrogen etch step. This too resulted in lower 3-D features, but was not satisfactory. During this time, growth on 3C-SiC on SOI substrates was being experimented with and great results were produced by skipping the hydrogen etch step (SOI will be discussed in section 4.5). Therefore, experiments were conducted in which the hydrogen etch step was not performed. Figure 4.7 shows the process flow for these experiments.

![Process flow for growth process of 3C-SiC on Si(001) under LPCVD conditions without a separate oxide etch step.](image)

**Figure 4.7** Process flow for growth process of 3C-SiC on Si(001) under LPCVD conditions without a separate oxide etch step.
The hydrogen and propane were introduced initially at atmospheric pressure with flow rates of 1 slm and 100 sccm (3% in hydrogen), respectively. At this time, the temperature was then raised to the growth temperature of 1380°C. After one minute, the pressure was reduced to 150 Torr and the hydrogen flow increased to 9 slm. After another minute, the propane was reduced to 70 sccm (3% in hydrogen) and at the same time, silane was introduced with a flow rate of 70 sccm (3% in hydrogen). The growth then proceeded as long as desired followed by an Ar purge. The results of these experiments were very promising as it gave the best morphology of all the runs conducted so far on bulk Si(001). However, one more adjustment was made to reduce the doping. The propane flow during growth was set to 75 sccm (3% in hydrogen) instead of 70 sccm to reduce the Si/C ratio from 0.33 to 0.31 [19]. This process produced an excellent morphology for 3C-SiC on Si(001) at low pressure as shown in Figure 4.8. As shown in the micrograph, there are just a few 3D towers and the morphology is excellent.

Figure 4.8 SEM micrograph of 3C-SiC grown on Si(001) at low pressure using the process shown in Figure 4.7. Sample ID: USF-03-187. Note reduction in 3D SiC tower density.
A 3C-SiC on Si(001) process at low pressure has been demonstrated. The film morphology produced using an optimized process schedule developed during this phase of the research was found to be of excellent quality as determined by plan-view SEM. The 3-D features noticed in the early experiments were drastically reduced and nearly eliminated. The growth on porous Si at low pressure was then experimented on and is discussed in the following section.

4.4 3C-SiC Growth on Porous Si(001)

The growth of 3C-SiC on porous Si(001) was also conducted under both atmospheric and low pressure conditions. The porous Si(001) samples were provided by Dr. Choyke of the University of Pittsburgh. The first set of experiments involved the growth of 3C-SiC on porous Si under APCVD conditions. LTPL experiments conducted by the University of Pittsburgh indicated that there was no observable difference in epi quality between 3C-SiC grown on porous Si and standard bulk Si. This result was partly due to the high doping level in the reactor at that time (indeed, Dr. Choyke noted we probably had a leak and after leak-checking the propane line we found 3 leaks that were repaired immediately. LTPL is certainly a sensitive technique to measure epi layer doping density!). That no difference was detected in epi quality between porous and standard Si substrates was substantiated by TEM experiments performed by Dr. T. S. Kuan at SUNY-Albany where, again, no quantitative difference in film quality was observed. However, a high degree of pore modification during these initial experiments was observed. A review of the literature was conducted to determine what, if anything, has been done in the Si community to solve this problem.
It was discovered by the Si community that the porous network could be stabilized prior to epi growth such that the resulting Si films were of the highest quality. The problem is that porous structure modification at process temperature can cause large voids to form in the porous layer, adding stress to the film and reducing epi quality. Hence we employed porous stabilization in an attempt to reduce this effect during growth using the following procedure:

After the porous Si samples were RCA cleaned, they were cleaved in two parts so that the affect of pore stabilization on epi growth could be observed. For the treated samples an oxide layer of approximately 500 Å was thermally grown in dry oxygen for 180 minutes [40]. The sample was then annealed for 2 minutes at 950 °C in an Ar ambient in a rapid thermal annealing system and cooled to room temperature [39]. The oxide was then stripped off prior to epi growth by immersing the sample in buffered oxide etch (BOE / 10:1). The treated and the non-treated samples were then loaded into the reactor for epi growth under identical conditions so as to compare the resulting 3C-SiC epi film quality.

The process flow for 3C-SiC on the porous samples is shown in Figure 4.9. As described, a 10 minute hydrogen etch at low pressure was conducted prior to sample carbonization. This hydrogen etch most likely modified the pores since part of the surface was etched away (indeed this etch step was mistakenly used, which is unfortunate due to the limited and special nature of this one-shot experiment). Carbonization took place after the sample was cooled after the hydrogen etch step. Propane was introduced at 60 sccm (3% in hydrogen) at which time the temperature was increased to the growth temperature of 1380°C. After 1.5 minutes, the propane was increased to 70 sccm (3% in
hydrogen) and, at the same time, silane was introduced with a flow rate of 70 sccm (3% in hydrogen) as well. Growth occurred for 5 hours where an Ar purge was used to cool the sample.

![Process flow for growth of 3C-SiC on porous Si(001) under LPCVD conditions. Both pore stabilized and un-stabilized porous Si were used for growth during this experiment. USF ID USF-03-160.](image)

**Figure 4.9** Process flow for growth of 3C-SiC on porous Si(001) under LPCVD conditions. Both pore stabilized and un-stabilized porous Si were used for growth during this experiment. USF ID USF-03-160.

A standard Si(001) sample was also included in this growth run to compare all three samples. SEM study was performed on theses samples and is shown in Figure 4.10. In part (a) of the figure, the standard is of good quality morphology as seen by the texture between the 3-D boulders. As shown in parts (b) and (c), the porous without the pore stabilization process has a better morphology than that with the pore stabilization. However, it is not fair to conclude that the pore stabilization process used here produces such morphologies consistently since only one such study was performed due to limited sample availability. It is obvious that other pore stabilization conditions must be experimented with to optimize this process (more will be said of this in Chapter 5).
Figure 4.10  SEM micrographs of (a) standard Si(001): USF-03-160G, (b) porous Si(001): USF-03-160B, (c) oxidized and annealed porous Si(001): USF-03-160A. Note the superior morphology on standard Si(001). The boundary in (b) and (c) represents the standard Si and porous Si boundary (porous area on right side of micrographs).

Not only was SEM characterization performed, but also LTPL by Dr. Choyke’s group at the University of Pittsburgh. The LTPL data indicated that there is an approximately -1.0 Å peak shift in the No peak position for the 3C-SiC grown on porous Si, while there is approximately a -5 Å peak shift in the No peak position for the 3C-SiC grown on pore stabilized porous Si. Unfortunately quantitative assessment of the defect structure of these films is difficult due to the relatively high doping density in the films (estimated by Dr. Choyke to be in the mid $10^{18}$ cm$^{-3}$ range) which broadens the peaks and makes precise peak position assessment difficult.

Initial growth studies of 3C-SiC on porous Si(001) have been conducted, however, much more research is needed in the area of low pressure growth on porous Si as well as pore stabilized Si before the potential benefits of this approach to defect reduction can be realized. The growth on porous Si may be a promising growth technique to produce high quality films. One last method researched during this thesis
for growth of 3C-SiC on novel substrates will be discussed in the next section; growth of
3C-SiC on SOI substrates.

4.5 3C-SiC Growth on SOI Substrates

As stated previously in Chapter 2, growth on ceramic substrates is one possible
approach to produce high quality 3C-SiC material due to the ability to exceed the melting
temperature of Si and therefore perform high temperature growth. In addition, the
thermal expansion coefficient mismatch between Si and SiC at higher temperatures is
large, which causes dislocations to form in the epitaxial layer. However polycrystalline
3C-SiC (which is essentially a ceramic) has a very similar thermal expansion coefficient
compared to 3C-SiC as shown in Figure 4.11. If growth of 3C-SiC can be made on
polycrystalline 3C-SiC, the result would be less stress in the epilayer. The substrate,
being of polycrystalline SiC and not Si, allows the growth temperature to exceed 1410°C;
which has been demonstrated in our laboratory to be superior to low-temperature growth
[31]. Hence development of a 3C-SiC ‘SOI’ like process should result in improved
epitaxial layers for device applications.
Preliminary growth studies of 3C-SiC on SOI ceramic substrates were conducted during this thesis research. The substrates were provided by Dr. Karl Hobart at the Naval Research Laboratory, Washington, DC. The commercial polycrystalline material was produced by bulk CVD in which 75 mm wafers were machined [14]. Thin Si layers were then bonded to the polycrystalline substrates, diced into 1 cm squares, and provided to our group for 3C-SiC growth. Figure 4.12 shows the step-by-step procedure used to produce the Si bonded to polycrystalline 3C-SiC (i.e. ‘SOI’) samples. Thin layers of Si and Si_{0.7}Ge_{0.3} were epitaxially grown on host Si(001) wafers via low pressure CVD producing thicknesses of 12 and 30 nm, respectively [14]. H_2^+ was then implanted into these films using the so-called ‘smart-cut process’ [14]. The two wafers (polycrystalline SiC and the epitaxially grown Si and SiGe) were brought into contact by force, and then heated to 225 °C for several hours to increase the bond strength [14]. The hydrogen was exfoliated from the wafers by heating to 550 °C, where the host Si was also cleaved at the
peak depth of the hydrogen implant [14]. The remaining host Si was removed with
KOH, along with the SiGe layer which was removed in another solution [14]. The SiGe
layer serves as an etch stop so that the thin Si film is protected during this process.

![Diagram](image)

**Figure 4.12** Step flow process to produce ceramic substrates for growth of 3C-SiC [14].

Once the Si has been bonded to the polycrystalline 3C-SiC, growth of 3C-SiC/Si
can proceed. As stated previously in this thesis, the carbonization step converts the Si
surface into SiC and also serves as a buffer layer for the growth. At this point, growth
can proceed. Figure 4.13 displays a diagram of the cross section of the sample as each
step in the process is performed. Part (a) shows the starting substrate on which the 3C-
SiC is to be grown on. Part (b) shows the carbonization step where the top layer of the Si
is converted to SiC. The final step, part (c), displays the growth of 3C-SiC on the
carbonized 3C-SiC layer. Note that the oxide etch step was not used since the thin Si
film could be completely removed prior to carbonization.
Figure 4.13 Step flow of 3C-SiC process on ceramic ‘SOI’ substrates. (a) starting SOI substrate; (b) sample after carbonization step and ; (c) after growth of 3C-SiC on carbonized layer.

The first set of 3C-SiC on ceramic substrate growth experiments performed during this thesis research contained both a hydrogen etch and carbonization step under APCVD conditions. If the surface quality after carbonization was not smooth, then there is no need to continue the experiment with the growth step. Hence the carbonization step was the end point in the first experiments so that the morphology could be studied. This led to change in the 3C-SiC/Si growth process which will now be described. Initially, the sample was placed in the reactor with a hydrogen flow of 4.5 slm, and the temperature was raised to 1050 °C, at atmospheric pressure. After 10 minutes of $H_2$ etching, the temperature was reduced to room temperature to allow the sample cool for 5 minutes.

Propane was then introduced at a flow of 20 sccm (3% in hydrogen) for one minute before increasing the temperature to 1050 °C. The sample was held at this temperature for 2 minutes in which the temperature was raised to the growth temperature of 1350 °C. The rf heating was turned off and the sample was cooled under an Ar purge. The sample was characterized by optical microscopy and showed a smooth surface. The propane flow was varied for different experiments to see if any changes resulted in the
morphology, which it did not. Growth was then performed with the same process, only adding SiH$_4$ to the gas flow one and a half minutes after reaching growth temperature. The morphology for the growths conducted produced a polycrystalline film. Many experiments were conducted by changing the gas flows of the precursors and the amount of etch time, all resulting in polycrystalline films. Finally, it became apparent that the Si was being etched away during the etch step, exposing the polycrystalline surface in which growth produced the same material. Once this was discovered, growth experiments were conducted without the etch step, in which both C$_3$H$_8$ and H$_2$ were the gases flowing in the reactor prior to the rf generator being switched on. The temperature was increased, via a controlled thermal ramp, directly to the growth temperature. While the temperature was increasing, carbonization of the Si was taking place so as not to have a separate step for the carbonization. The SiH$_4$ was then introduced 1.5 minutes after reaching the growth temperature of 1380 ºC. This too resulted in polycrystalline films, which meant the Si was still being consumed (etched) before the Si could be converted to SiC.

The literature was reviewed and it had been reported that the growth took place at low pressure and the carbonization took place at atmospheric pressure [14] with very low flow of H$_2$ [36]. Therefore, experiments were conducted under nearly the same conditions. The final process flow developed in this work, which resulted in single-crystal 3C-SiC, is shown in Figure 4.14. The reactor was initially at atmospheric pressure and both H$_2$ and C$_3$H$_8$ were introduced at 1 slm and 100 sccm, respectively. The temperature was then raised to 1380ºC and maintained at this value for one minute. The pressure was then brought down to 150 Torr, after which the H$_2$ flow was increased to 9 slm. The measured temperature difference between 760 and 150 Torr had to be compensated for to ensure that the actual temperature was held constant at 1380 ºC.
Once the pressure and temperature reached steady-state, silane was introduced at a flow of 70 sccm (3% in hydrogen) while at the same time, the propane flow was reduced to 70 sccm (3% in hydrogen). At this time, growth proceeded for however long was required. After the growth, all gases were ceased from flowing except $\text{H}_2$ for 30 seconds. Then $\text{H}_2$ was turned off and Ar was introduced for 2 minutes at which time the rf heating source was turned off. Then the sample cooled under Ar purge for 25 minutes.

Figure 4.14  3C-SiC on ceramic substrate (3C-SOI) process schedule developed during this thesis research. Results of this work were recently reported at the International Conference on SiC and Related Materials (ICSCRM) [38].
The above process produced the best 3C-SiC morphology on the ceramic substrate. The epi morphology was studied using the SEM and was found to be excellent, as shown in Figure 4.15. As can be seen in the 40x magnification micrograph (left image), there are small areas of polycrystalline film. These are regions where Si voids were present prior to growth from the bonding procedure (see left corner of micrograph). When the silicon was bonded to the polycrystalline 3C-SiC, voids were produced. When 3C-SiC growth occurs, the areas of the Si voids produce a 3C-SiC epi film that is polycrystalline in structure. However, growth on the Si film results in a good morphological film of 3C-SiC. The plan-view SEM micrograph of Figure 4.15 (b) shows that the surface morphology is of a mosaic structure, which is common in the growth of 3C-SiC on Si substrates.

**Figure 4.15** Plan view SEM micrographs of 3C-SiC grown on a ceramic substrate; 1 hr growth produced film thickness of 2 µm determined from a standard Si(001) sample via cross-section SEM (not shown). (a) Magnification of 40x; (b) Magnification of 10,000x. Sample ID: USF-03-177B.
XRD evaluation of the film was then conducted at the Naval Research Laboratory. Figure 4.16 shows the measured rocking curve from the (002) reflection for two films where the growth was conducted for 30 min and 1 hour, (Sample No. USF-03-176B and USF-03-177B, respectively). The full width at half maximum (FWHM) is approximately 800 arc-sec which is comparable to the best films grown on Si(001) [37]. The XRD results show that the grown films are indeed 3C-SiC and are aligned with the original Si(100) film.

![Figure 4.16](image)

**Figure 4.16** Rocking curves for USF 3C-SiC epi grown on NRL fabricated 3C-SiC on ceramic substrates. Sample USF-03-176B was produced from a growth of 30 minutes, while USF-03-177B was for a growth of 60 minutes. The FWHM of sample 177 is 800 arc-sec, which is comparable with 3C-SiC grown on bulk Si(001).

As shown from these preliminary experiments, growth on ceramic substrates can result in good quality 3C-SiC films. This process is still being investigated to further characterize these films via TEM study of the 3C-SiC/Si interface. An important question that needs to be answered is if the entire thin Si bonded layer has been
consumed during growth. This is important since one of the main attractions of this process is that the growth temperature can exceed 1410 °C, which should result in better quality films. This research is on-going and results will be reported at a later date [38].

4.6 Summary

Many experiments were conducted on the growth of 3C-SiC on novel substrates at low pressure. A 3C-SiC process on standard Si(001) under LPCVD conditions was performed and the results are quite promising with high quality morphology achieved. The growth on porous Si needs to be looked into much further and many more experiments need to be performed in order to determine if the process will yield device quality morphology. The research during this thesis in this regard was only a starting point for the growth on porous Si at low pressure. Fortunately preliminary growth studies of 3C-SiC on SOI substrates proved to be very promising as the resulting morphology produced was excellent. More studies need to be conducted for this process also, however, especially in the area of increased growth temperature since growth is not limited by the silicon melting point.
CHAPTER 5
CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

The development of several growth processes for 3C-SiC on novel silicon substrates were completed during this thesis research. The main reason such substrates are needed is that dislocations occur from the lattice and thermal mismatch between the silicon substrate and the grown SiC epitaxial layer. The growth for all processes took place via atmospheric and low pressure chemical vapor deposition. The APCVD process for 3C-SiC grown on standard Si was presented along with XRD, TEM and SAD data. The TEM data showed that there were dislocations at the interface of the SiC/Si interface, as expected, and that the dislocations reduced in density with increasing film thickness. The SAD data provided information that the grown films were oriented parallel to the Si(001) substrate, while the XRD data proved that the 3C-SiC grown on standard Si(001) was single crystal. The process developed for the growth of 3C-SiC on various porous Si substrates also resulted in a mosaic morphology film, however, some of the films had excellent morphology which might prove to be of high quality. The final process conducted during this research at atmospheric pressure was growth of 3C-SiC on free standing 3C-SiC made from undulant Si substrates. The morphology determined by SEM was of reasonable quality; however, more studies are needed to assess the quality of these films.
The other processes developed during this research were for low pressure (150 Torr) CVD, which was implemented to produce higher growth rates and superior films due to the suppression of Si clusters in the gas phase under these operating conditions. The first set of experiments were conducted for 3C-SiC grown on standard Si(001). SEM was used as the primary tool to determine the quality of the grown films. Initially, the film contained 3D towers, which were eventually reduced in density by adjusting the growth process. The morphology of films from the resulting process was shown to be of excellent quality. Growth at low pressure was also conducted on porous Si(001) substrates. Unfortunately, there was only one sample available for this purpose. This sample was cleaved into two pieces and one of the pieces oxidized and annealed in an attempt to stabilize the pores during subsequent thermal processing (i.e., CVD growth). Both sets were grown on at low pressure to determine which gave way to the highest quality. SEM data was obtained for these samples and indicated that the non-oxidized porous sample had the better morphology compared with the oxidized porous substrate. However, more data must be taken to determine which is indeed of higher quality, and in particular LTPL is needed to truly assess the material quality. These samples have been sent to Prof. Choyke’s group at the University of Pittsburgh for just this purpose and results are pending. The final growth experiments were conducted on SOI substrates. These are highly beneficial substrates as the growth temperature may well exceed the melt temperature of Si. SEM study of the grown films indicates good quality morphology for these films once a suitable growth process had been developed. Indeed, a significant number of growth runs were conducted before the right combination of process steps, temperature and pressure were discovered. The LPCVD process was
critical for growth on SOI substrates. At APCVD conditions, the films grown on the SOI substrates were not single-crystal 3C-SiC, however, they were single crystal at LP conditions. XRD investigation of these samples were also conducted and indicated that the film was indeed 3C-SiC and was aligned with the original Si(001) film. These experiments are on going and will be published at a later date.

5.2 Future Work

The first task to be completed is the transfer of the 3C-SiC cold-wall growth process to the hot wall epi reactor configuration. Since the hot wall susceptor consists of TaC coated graphite, this will involve using a poly-crystalline plate to place the Si samples on top of. The same procedure as described here, starting with carbonization and expanding the process to include growth, will be conducted. The advantage of the hot wall geometry is the reduction of quartz reactor parts in contact with the boat (there is no boat). In addition, tube change out is much reduced so more runs can be conducted in the same amount of time. Finally, and most importantly, the lower thermal temperature gradient above the growth surface results in a much higher growth rate. For example, on 4H-SiC, an 8 µm film was grown in 30 min in the hot wall configuration and it takes over 4 hours to growth the same film in the cold wall configuration. Once a hot wall 3C-SiC process has been developed growth of 3C-SiC on porous Si, stabilized porous Si and SOI material will be repeated in the same manner as described in this thesis.

In the near future, extensive pore stabilization studies will be conducted on porous Si substrates in a effort to limit the thermal migration of the pores during growth. Preliminary work for the stabilization process has been conducted by Shailaja Rao, and
will be expanded so that a suitable process is developed. The pore stabilization will be beneficial not only for the growth process of 3C-SiC grown on porous Si but for all SiC epi growth experiments on porous templates (porous 4H, 6H, 3C, etc.). Therefore the investment of time and resources to fully and properly conduct this task is strongly recommended.

Continued research is needed for the growth of 3C-SiC on SOI substrates to achieve device-quality. Higher temperature growths will be conducted in order to produce the highest quality film since it is known from growth of 3C-SiC on bulk 3C-SiC that higher growth temperatures produce the best epi [31]. TEM will be employed to determine if the Si film is completely consumed. Many different temperatures, along with other parameters, will be experimented with to determine which gives the best results. This research is very important as temperatures beyond the Si melt point may be explored to produce optimum epi.

Research on the different types of porous Si will also need to be continued. As stated in this thesis, there are many different possible pore structures. These porous layers need to be examined to determine which porous structure gives way to the best film quality. XRD, LTPL, and TEM should again be used to determine the material quality. Maximum use of the new USF XRD in the Nanomaterials and Nanomanufacturing Research Center (NNRC) should be made to increase experimental throughput by greatly reducing analytical feedback time, which has hampered efforts till now.

The preliminary work aimed at pore stabilization must be continued until the best porous structure for 3C-SiC epi growth on porous Si is determined. For starters a repeat
of USF-03-160, where the former in-situ hydrogen etch step was inadvertently used, needs to be repeated with the latest LPCVD 3C-SiC process. In parallel various porous layers should be treated in differing ways, based on a thorough literature survey, to optimize the probability of uncovering the optimum process. This includes various oxidation times, methods, etc. and annealing times and ambient gas compositions. This work already has been shown to have some benefits on epi quality, with a shift in the No PL line observed for oxidized (i.e., stabilized) porous Si compared with standard Si(001). Thus the necessary investment to produce a systematic series of experiments to properly assess the parameter space is warranted and suggested.

As shown during this thesis, more research is needed to produce high quality films that may later be used for devices. Indeed one such device, a hydrogen gas sensor, has already been demonstrated and a 5-fold increase in sensor output signal has been achieved merely by switching from APCVD grown 3C to LPCVD grown 3C. It is hoped that similar benefits will be observed for other devices. Ohmic contact research on LPCVD grown 3C-SiC films from this thesis is on-going in preparation for eventual 3C-SiC electronic device research. In addition, maximum use of the novel oxidation system implemented by Dr. A. M. Hoff in our laboratory [41] will be made so that the USF 3C-SiC electronic device program benefits from the best material available, all of which will be generated in-house. In summary, the research undertaken during this thesis period has shown a potential pathway to many applications of high value and pay-off to not only the SiC community but for sensors and systems on a chip as well. What is needed now is a more thorough and systematic study of each of the promising techniques discussed here
and it is the intent of the author to do just that while pursuing a doctorate in Electrical Engineering at USF.
REFERENCES


Thomas Schattner, Homoeipitaxial Growth of 4H and 6H-SiC in a 75mm Reactor, Master’s Thesis, Mississippi State University, Starkville, MS, May 2000.

“Lattice mismatch and its implication on critical thickness and interface structure,” http://www.iht.uni-stuttgart.de/lehre/QuanElekTech/Kap2_Zusatzmaterial.pdf

J.T. Wolan, ECH 6515, Advanced Reacting Systems, USF.

M.-A. Hasan, et. al, “Heteroepitaxy of cubic SiC (3C-SiC) on Si(100) using porous Si as a compliant seed crystal,” ICSCRM, 2001.


[29] Private conversation with S. Bhansali, USF.


[31] Private conversation with S. E. Saddow, USF.


[33] Private conversation with H. Nagasawa, Hoya Corp.


[37] Private conversation with Hobart, NRL.


